

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4027B **flip-flops** Dual JK flip-flop

Product specification
File under Integrated Circuits, IC04

January 1995

Dual JK flip-flop

HEF4027B flip-flops

DESCRIPTION

The HEF4027B is a dual JK flip-flop which is edge-triggered and features independent set direct (S_D), clear direct (C_D), clock (CP) inputs and outputs (O, \bar{O}). Data is accepted when CP is LOW, and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the J, K, and CP inputs. The outputs are buffered for best system performance. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

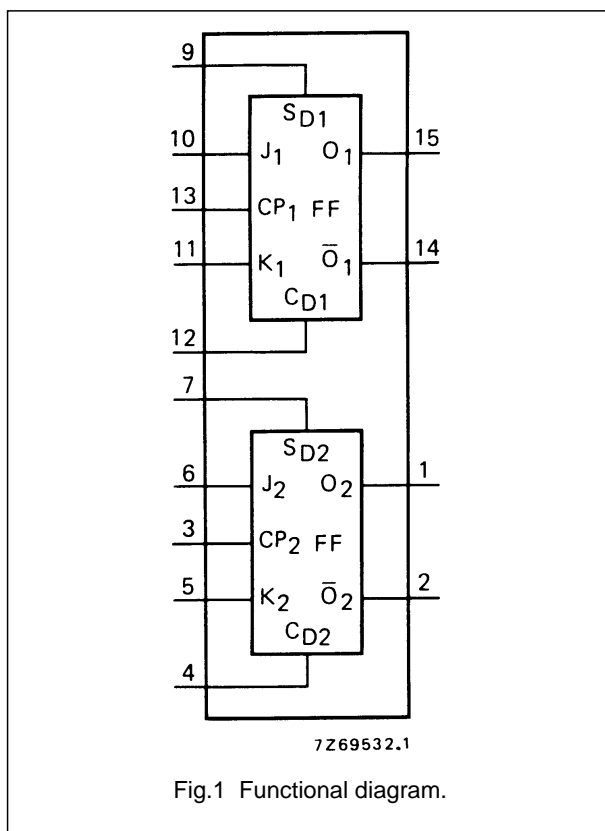


Fig.1 Functional diagram.

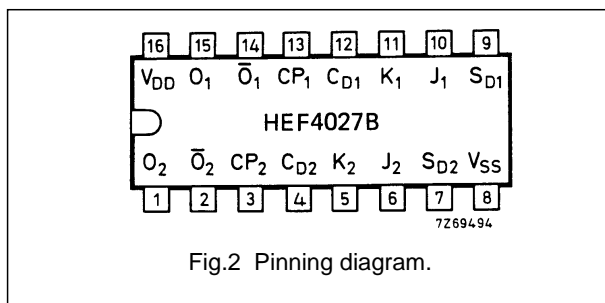


Fig.2 Pinning diagram.

FUNCTION TABLES

| INPUTS | | | | | OUTPUTS | |
|--------|-------|----|---|---|---------|-----------|
| S_D | C_D | CP | J | K | O | \bar{O} |
| H | L | X | X | X | H | L |
| L | H | X | X | X | L | H |
| H | H | X | X | X | H | H |

| INPUTS | | | | | OUTPUTS | |
|--------|-------|------------|---|---|-------------|-----------------|
| S_D | C_D | CP | J | K | O_{n+1} | \bar{O}_{n+1} |
| L | L | \nearrow | L | L | no change | |
| L | L | \nearrow | H | L | H | L |
| L | L | \nearrow | L | H | L | H |
| L | L | \nearrow | H | H | \bar{O}_n | O_n |

Notes

- H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
 \nearrow = positive-going transition
 O_{n+1} = state after clock positive transition

PINNING

- J,K synchronous inputs
- CP clock input (L to H edge-triggered)
- S_D asynchronous set-direct input (active HIGH)
- C_D asynchronous clear-direct input (active HIGH)
- O true output
- \bar{O} complement output

- HEF4027BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4027BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4027BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category FLIP-FLOPS

See Family Specifications

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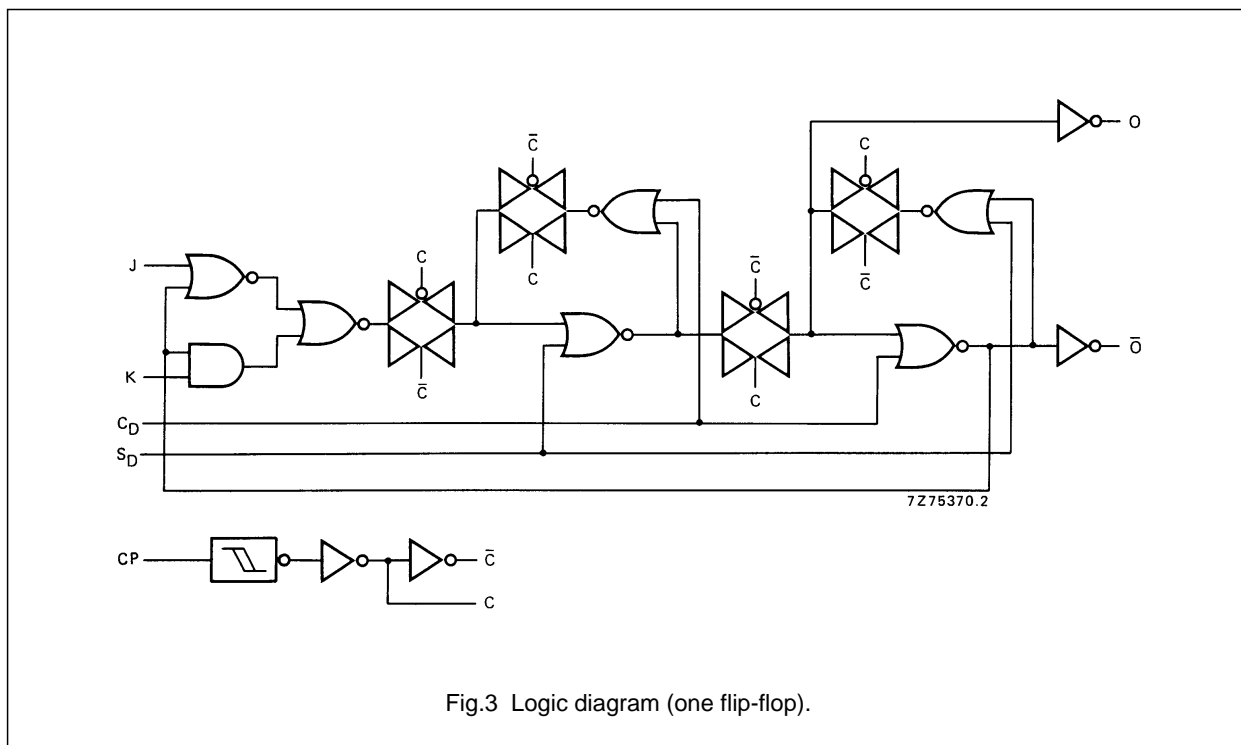


Fig.3 Logic diagram (one flip-flop).

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

| | V _{DD} V | SYMBOL | MIN. | TYP. | MAX. | TYPICAL EXTRAPOLATION FORMULA |
|----------------------------|----------------------|------------------|------|------|--------|--------------------------------------|
| Propagation delays | | | | | | |
| CP → O, \bar{O} | 5 | | | 105 | 210 ns | 78 ns + (0,55 ns/pF) C _L |
| HIGH to LOW | 10 | t _{PHL} | 40 | 80 | ns | 29 ns + (0,23 ns/pF) C _L |
| | 15 | | 30 | 60 | ns | 22 ns + (0,16 ns/pF) C _L |
| LOW to HIGH | 5 | t _{PLH} | | 85 | 170 ns | 58 ns + (0,55 ns/pF) C _L |
| | 10 | | 35 | 70 | ns | 27 ns + (0,23 ns/pF) C _L |
| | 15 | | 30 | 60 | ns | 22 ns + (0,16 ns/pF) C _L |
| S _D → O | 5 | | | 70 | 140 ns | 43 ns + (0,55 ns/pF) C _L |
| LOW to HIGH | 10 | t _{PLH} | 30 | 60 | ns | 19 ns + (0,23 ns/pF) C _L |
| | 15 | | 25 | 50 | ns | 17 ns + (0,16 ns/pF) C _L |
| C _D → O | 5 | | | 120 | 240 ns | 93 ns + (0,55 ns/pF) C _L |
| HIGH to LOW | 10 | t _{PHL} | 45 | 90 | ns | 33 ns + (0,23 ns/pF) C _L |
| | 15 | | 35 | 70 | ns | 27 ns + (0,16 ns/pF) C _L |
| S _D → \bar{O} | 5 | | | 140 | 280 ns | 113 ns + (0,55 ns/pF) C _L |
| HIGH to LOW | 10 | t _{PHL} | 55 | 110 | ns | 44 ns + (0,23 ns/pF) C _L |
| | 15 | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) C _L |

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| | V_{DD} V | SYMBOL | MIN. | TYP. | MAX. | TYPICAL EXTRAPOLATION FORMULA | |
|--|---------------|----------------------------|------|------|------|----------------------------------|--|
| $C_D \rightarrow \bar{O}$ LOW to HIGH | 5 | t_{PLH} | | 75 | 150 | ns | $48 \text{ ns} + (0,55 \text{ ns/pF}) C_L$ |
| | 10 | | | 35 | 70 | ns | $24 \text{ ns} + (0,23 \text{ ns/pF}) C_L$ |
| | 15 | | | 25 | 50 | ns | $17 \text{ ns} + (0,16 \text{ ns/pF}) C_L$ |
| Output transition times HIGH to LOW | 5 | t_{THL} | | 60 | 120 | ns | $10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$ |
| | 10 | | | 30 | 60 | ns | $9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$ |
| | 15 | | | 20 | 40 | ns | $6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$ |
| LOW to HIGH | 5 | t_{TLH} | | 60 | 120 | ns | $10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$ |
| | 10 | | | 30 | 60 | ns | $9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$ |
| | 15 | | | 20 | 40 | ns | $6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$ |
| Set-up time J,K \rightarrow CP | 5 | t_{su} | | 50 | 25 | ns | see also waveforms Figs 4 and 5 |
| | 10 | | | 30 | 10 | ns | |
| | 15 | | | 20 | 5 | ns | |
| Hold time J,K \rightarrow CP | 5 | t_{hold} | | 25 | 0 | ns | |
| | 10 | | | 20 | 0 | ns | |
| | 15 | | | 15 | 5 | ns | |
| Minimum clock pulse width; LOW | 5 | t_{WCPL} | | 80 | 40 | ns | |
| | 10 | | | 30 | 15 | ns | |
| | 15 | | | 24 | 12 | ns | |
| Minimum S_D , C_D pulse width; HIGH | 5 | t_{WSDH} , t_{WCDH} | | 90 | 45 | ns | |
| | 10 | | | 40 | 20 | ns | |
| | 15 | | | 30 | 15 | ns | |
| Recovery time for S_D , C_D | 5 | t_{RSD} , t_{RCD} | | 20 | -15 | ns | |
| | 10 | | | 15 | -10 | ns | |
| | 15 | | | 10 | -5 | ns | |
| Maximum clock pulse frequency J = K = HIGH | 5 | f_{max} | | 4 | 8 | MHz | see also waveforms Fig.4 |
| | 10 | | | 12 | 25 | MHz | |
| | 15 | | | 15 | 30 | MHz | |

| | V_{DD} V | TYPICAL FORMULA FOR P (μ W) | |
|---|---------------|--|---|
| Dynamic power dissipation per package (P) | 5 | $900 f_i + \sum (f_o C_L) \times V_{DD}^2$ | where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V) |
| | 10 | $4\,500 f_i + \sum (f_o C_L) \times V_{DD}^2$ | |
| | 15 | $13\,200 f_i + \sum (f_o C_L) \times V_{DD}^2$ | |

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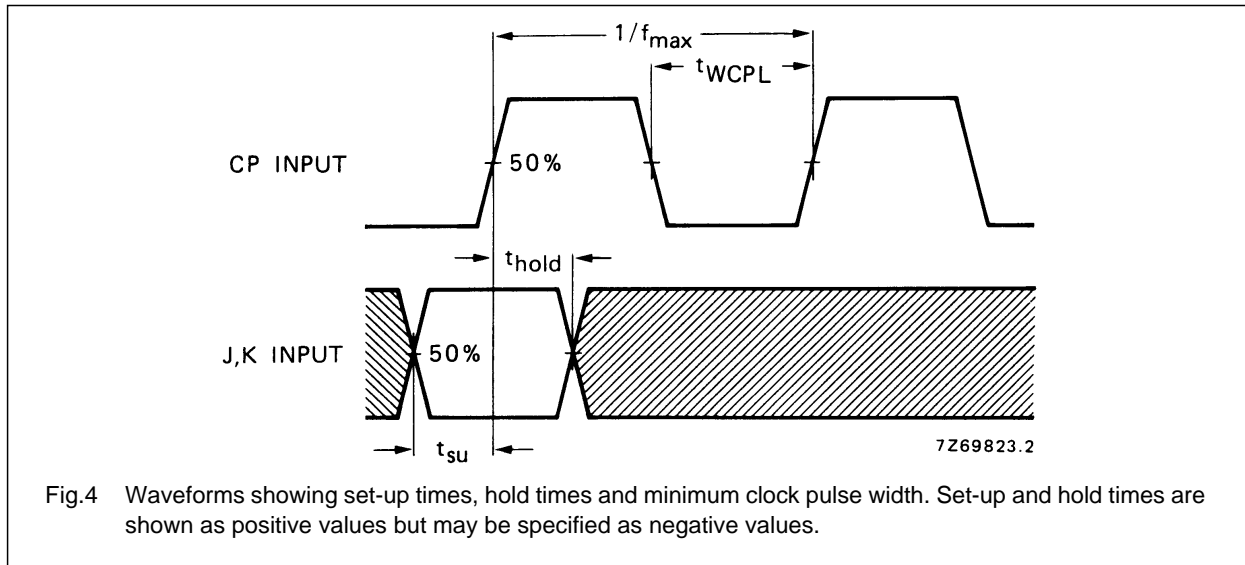
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Fig.4 Waveforms showing set-up times, hold times and minimum clock pulse width. Set-up and hold times are shown as positive values but may be specified as negative values.

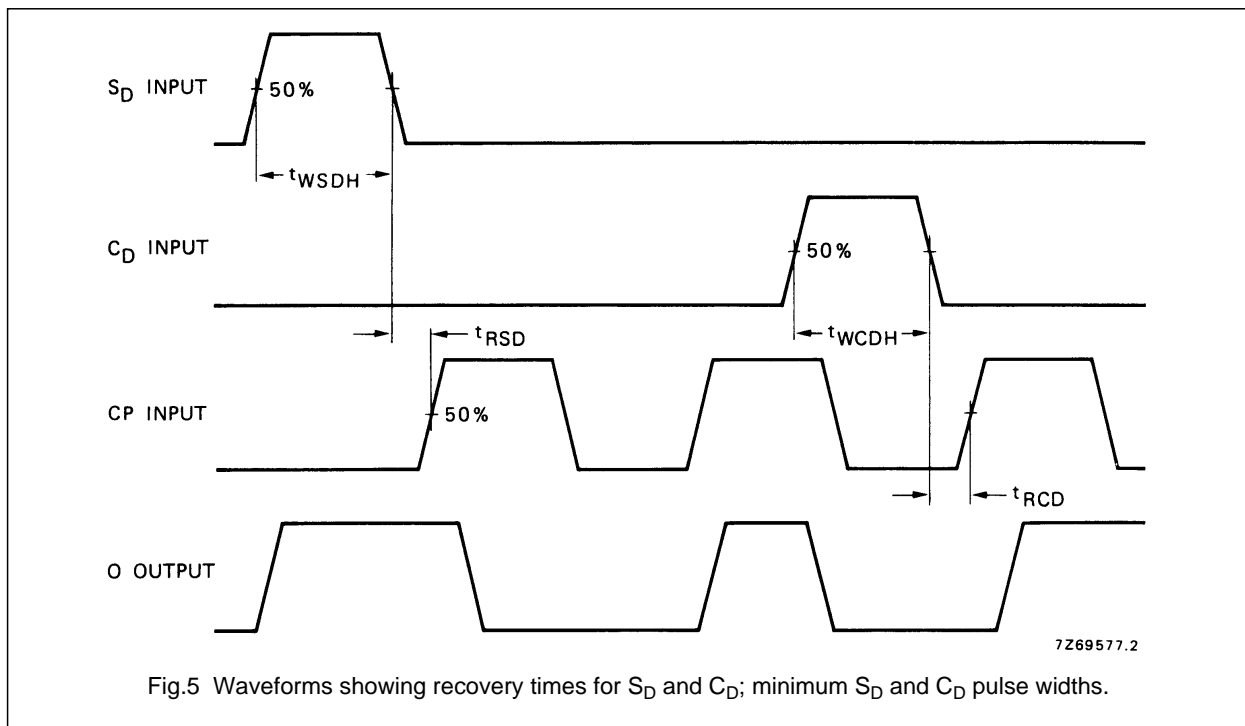


Fig.5 Waveforms showing recovery times for S_D and C_D ; minimum S_D and C_D pulse widths.

APPLICATION INFORMATION

Some examples of applications for the HEF4027B are:

- Registers
- Counters
- Control circuits