

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF40240B**

### **buffers**

Octal inverting buffers with 3-state outputs

Product specification  
File under Integrated Circuits, IC04

January 1995

# Octal inverting buffers with 3-state outputs

# HEF40240B buffers

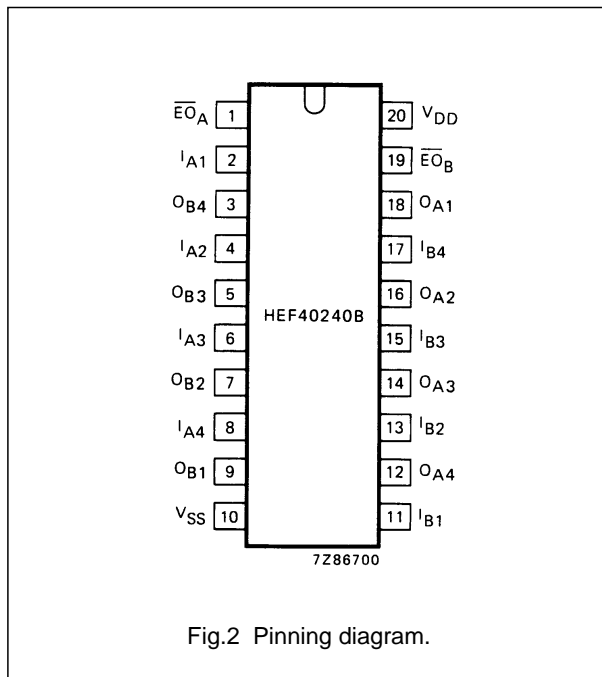
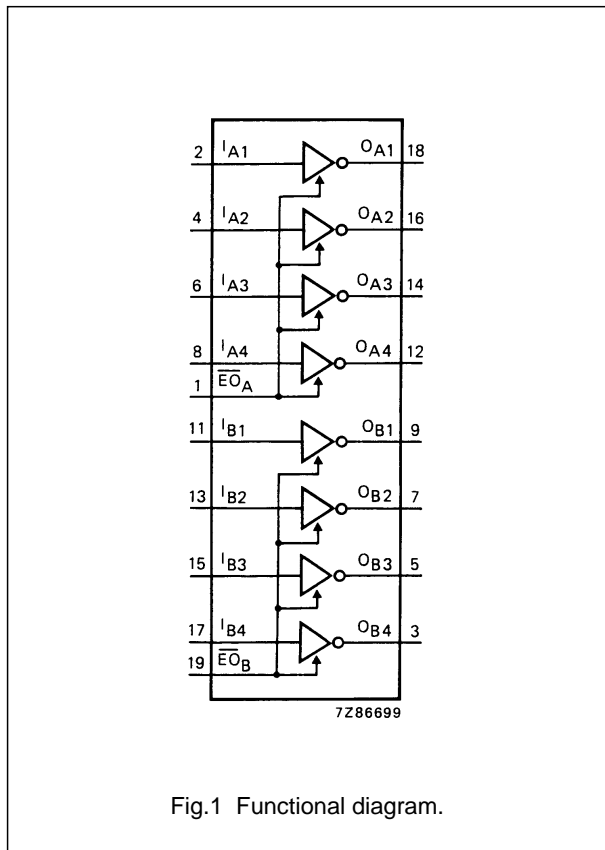
### DESCRIPTION

The HEF40240B is an octal inverting buffer with 3-state outputs. It features output stages with high current output capability suitable for driving highly capacitive loads.

The 3-state outputs are controlled by the output enable inputs  $\overline{EO}_A$  and  $\overline{EO}_B$ . A HIGH on  $\overline{EO}$  causes the outputs to assume a high impedance OFF-state. The device also features hysteresis on all inputs to improve noise immunity.

Schmitt-trigger action in the inputs makes the circuit highly tolerant to slower input rise and fall times.

The HEF40240B is pin and functionally compatible with the TTL '240' device.



- HEF40240BP(N): 20-lead DIL; plastic (SOT146-1)
- HEF40240BD(F): 20-lead DIL; ceramic (cerdip) (SOT152)
- HEF40240BT(D): 20-lead SO; plastic (SOT163-1)
- ( ): Package Designator North America

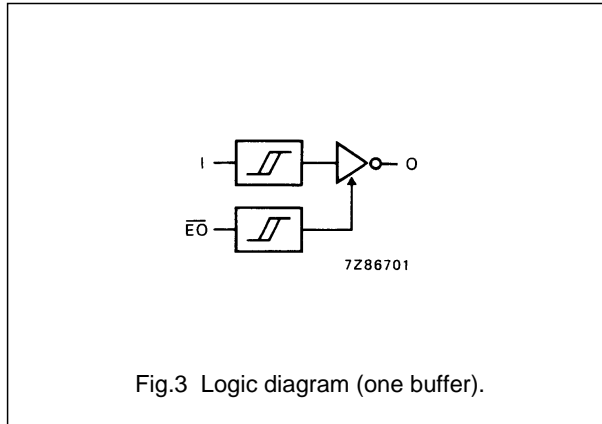
### PINNING

- $I_{A1}$  to  $I_{A4}$  inputs
- $I_{B1}$  to  $I_{B4}$  inputs
- $O_{A1}$  to  $O_{A4}$  bus outputs
- $O_{B1}$  to  $O_{B4}$  bus outputs
- $\overline{EO}_A, \overline{EO}_B$  output enable inputs (active LOW)

### FAMILY DATA, $I_{DD}$ LIMITS category buffers

See Family Specifications

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## TRUTH TABLE

INPUTS		OUTPUT
$I_n$	$\overline{EO}$	$O_n$
H	L	L
L	L	H
X	H	Z

## Notes

- H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)  
X = state is immaterial  
Z = high impedance off state

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

See Family Specifications except for:

D.C. current into any input	$\pm I_I$	max.	10 mA
D.C. source or sink current into any output	$\pm I_O$	max.	25 mA
D.C. current into the supply terminals	$\pm I$	max.	100 mA

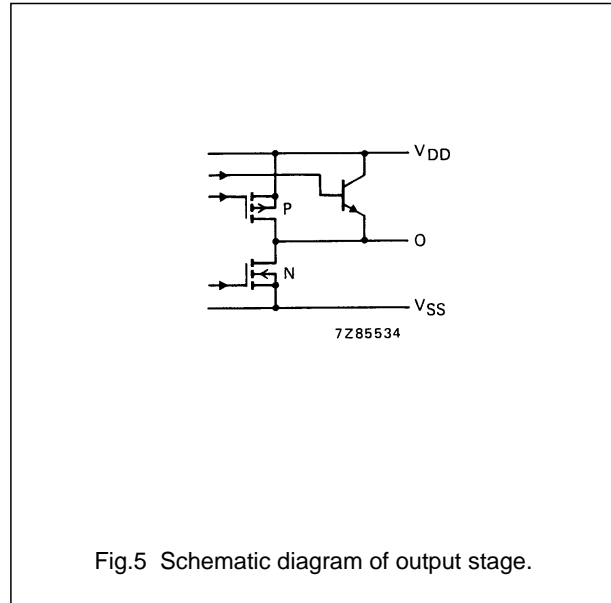
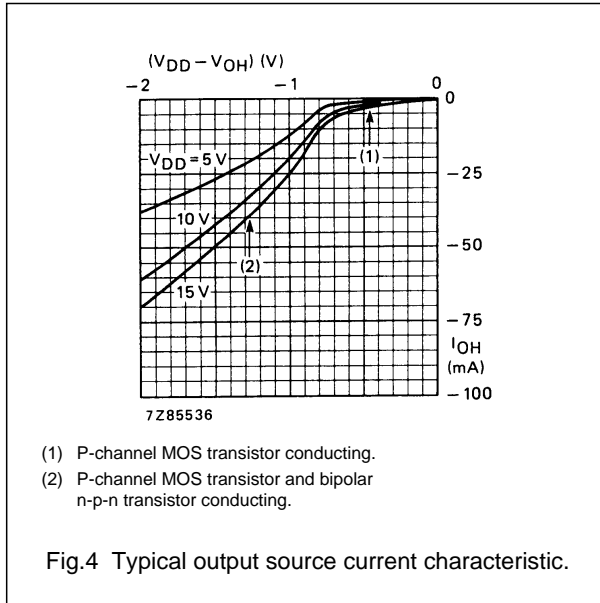
## DC CHARACTERISTICS

$V_{SS} = 0 V$

PARAMETER	$V_{DD}$	$V_{OH}$	$V_{OL}$	SYMBOL	$T_{amb} (^\circ C)$						UNIT
					-40		+25		+85		
					MIN.	TYP.	MIN.	TYP.	MIN.	TYP.	
Output current HIGH	5	3,6	-	$-I_{OH}$	9,3	-	10,0	24,0	10,7	-	mA
	10	8,4	-	$-I_{OH}$	14,4	-	15,0	46,0	15,0	-	mA
	15	13,2	-	$-I_{OH}$	19,5	-	20,0	62,0	19,8	-	mA
Output current HIGH	5	4,6	-	$-I_{OH}$	0,75	-	0,6	1,2	0,45	-	mA
	10	9,5	-	$-I_{OH}$	1,85	-	1,5	3,0	1,1	-	mA
	15	13,5	-	$-I_{OH}$	14,5	-	15,0	50,0	15,5	-	mA
Output current LOW	5	-	0,4	$I_{OL}$	2,9	-	2,3	5,4	1,75	-	mA
	10	-	0,5	$I_{OL}$	9,5	-	7,6	17,0	5,50	-	mA
	15	-	1,5	$I_{OL}$	30,0	-	25,0	45,0	19,0	-	mA
Hysteresis voltage (any input)	5	-	-	$V_H$	-	-	-	220,0	-	-	mV
	10	-	-	$V_H$	-	-	-	250,0	-	-	mV
	15	-	-	$V_H$	-	-	-	320,0	-	-	mV

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AC CHARACTERISTICS

VSS = 0 V; Tamb = 25 °C; input transition times ≤ 20 ns

ALL BUFFERS SWITCHING	V <sub>DD</sub> V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	4 250 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	where f <sub>i</sub> = input freq. (MHz) f <sub>o</sub> = output freq. (MHz) C <sub>L</sub> = load capacitance (pF) ∑ (f <sub>o</sub> C <sub>L</sub> ) = sum of outputs V <sub>DD</sub> = supply voltage (V)
dissipation per	10	17 000 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	
package (P)	15	46 000 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	

## Octal inverting buffers with 3-state outputs

HEF40240B  
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PARAMETER	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	UNIT	TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
$I_{An/Bn} \rightarrow O_{An/Bn}$ HIGH to LOW	5	$t_{PHL}$		95	190	ns	$83\text{ ns} + (0,24\text{ ns/pF}) C_L$
	10			40	80	ns	$35\text{ ns} + (0,10\text{ ns/pF}) C_L$
	15			30	60	ns	$26\text{ ns} + (0,07\text{ ns/pF}) C_L$
$I_{An/Bn} \rightarrow O_{An/Bn}$ LOW to HIGH	5	$t_{PLH}$		85	170	ns	$82\text{ ns} + (0,06\text{ ns/pF}) C_L$
	10			40	80	ns	$38\text{ ns} + (0,03\text{ ns/pF}) C_L$
	15			30	60	ns	$29\text{ ns} + (0,02\text{ ns/pF}) C_L$
Output transition times	5	$t_{THL}$		40	80	ns	see Fig.6
HIGH to LOW	10			20	40	ns	
	15			15	30	ns	
LOW to HIGH	5	$t_{TLH}$		30	60	ns	
	10			20	40	ns	
	15			15	30	ns	
3-state propagation delays							
Output disable times							
$\overline{EO} \rightarrow O_{An/Bn}$ HIGH	5	$t_{PHZ}$		70	140	ns	
	10			35	70	ns	
	15			30	60	ns	
LOW	5	$t_{PLZ}$		75	150	ns	
	10			40	80	ns	
	15			30	60	ns	
Output enable times							
$\overline{EO} \rightarrow O_{An/Bn}$ HIGH	5	$t_{pZH}$		80	160	ns	
	10			35	70	ns	
	15			30	60	ns	
LOW	5	$t_{pZL}$		90	180	ns	
	10			40	80	ns	
	15			30	60	ns	

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