INTEGRATED CIRCUITS

DATA SHEET

74HC2G02; 74HCT2G02
Dual 2-input NOR gate

Product specification
Supersedes data of 2003 Feb 03

2003 May 14

Philips
Semiconductors

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FEATURES

- Wide supply voltage range from 2.0 to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Very small 8 pins package
- Output capability is standard
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74HC2G/HCT2G02 is a high-speed Si-gate CMOS device.

The 74HC2G/HCT2G02 provides the 2-input NOR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 6.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC2G02	HCT2G02	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	9	12	ns
C_I	input capacitance		1.5	1.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	10	10	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. For 74HC2G02 the condition is V_I = GND to V_{CC}.
   For 74HCT2G02 the condition is V_I = GND to V_{CC} – 1.5 V.

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC2G02DP	–40 to +125 °C	8	TSSOP8	plastic	SOT505-2	H02
74HCT2G02DP	–40 to +125 °C	8	TSSOP8	plastic	SOT505-2	T02
74HC2G02DC	–40 to +125 °C	8	VSSOP8	plastic	SOT765-1	H02
74HCT2G02DC	–40 to +125 °C	8	VSSOP8	plastic	SOT765-1	T02

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	2Y	data output
4	GND	ground (0 V)
5	2A	data input
6	2B	data input
7	1Y	data output
8	V_{CC}	supply voltage

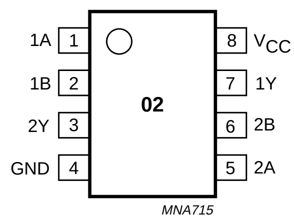


Fig.1 Pin configuration.

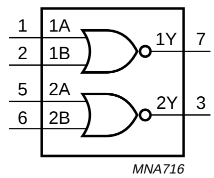


Fig.2 Logic symbol.

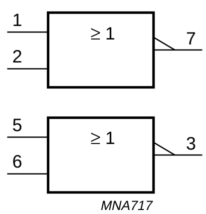


Fig.3 IEC logic symbol.

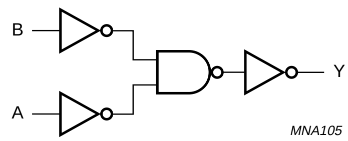


Fig.4 Logic diagram (one driver).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC2G02			74HCT2G02			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	–	–	1000	–	–	–	ns
		V_{CC} = 4.5 V	–	6.0	500	–	6.0	500	ns
		V_{CC} = 6.0 V	–	–	400	–	–	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	V_I < –0.5 V or V_I > V_{CC} + 0.5 V; note 1	–	±20	mA
I_{OK}	output diode current	V_O < –0.5 V or V_O > V_{CC} + 0.5 V; note 1	–	±20	mA
I_O	output source or sink current	–0.5 V < V_O < V_{CC} + 0.5 V; note 1	–	25	mA
I_{CC}, I_{GND}	V_{CC} or GND current	note 1	–	50	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation	T_{amb} = –40 to +125 °C; note 2	–	300	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 110 °C the value of P_D derates linearly with 8 mW/K.

DC CHARACTERISTICS

Type 74HC2G02

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V_{IL}	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = −20 μA	2.0	1.9	2.0	–	V
		I_O = −20 μA	4.5	4.4	4.5	–	V
		I_O = −20 μA	6.0	5.9	6.0	–	V
		I_O = −4.0 mA	4.5	4.13	4.32	–	V
		I_O = −5.2 mA	6.0	5.63	5.81	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 20 μA	2.0	–	0	0.1	V
		I_O = 20 μA	4.5	–	0	0.1	V
		I_O = 20 μA	6.0	–	0	0.1	V
		I_O = 4.0 mA	4.5	–	0.15	0.33	V
		I_O = 5.2 mA	6.0	–	0.16	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	6.0	–	–	±1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	6.0	–	–	10	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = −20 μA	2.0	1.9	–	–	V
		I_O = −20 μA	4.5	4.4	–	–	V
		I_O = −20 μA	6.0	5.9	–	–	V
		I_O = −4.0 mA	4.5	3.7	–	–	V
		I_O = −5.2 mA	6.0	5.2	–	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 20 μA	2.0	–	–	0.1	V
		I_O = 20 μA	4.5	–	–	0.1	V
		I_O = 20 μA	6.0	–	–	0.1	V
		I_O = 4.0 mA	4.5	–	–	0.4	V
		I_O = 5.2 mA	6.0	–	–	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	6.0	–	–	±1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	6.0	–	–	20	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

Type 74HCT2G02

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = −20 μA	4.5	4.4	4.5	–	V
		I_O = −4.0 μA	4.5	4.13	4.32	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 20 μA	4.5	–	0	0.1	V
		I_O = 4.0 μA	4.5	–	0.15	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	±1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	10	μA
ΔI_{CC}	additional supply current per input	$V_I = V_{CC} - 2.1$ V; $I_O = 0$	4.5 to 5.5	–	–	375	μA
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = −20 μA	4.5	4.4	–	–	V
		I_O = −4.0 μA	4.5	3.7	–	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 20 μA	4.5	–	–	0.1	V
		I_O = 4.0 μA	4.5	–	–	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	±1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	20	μA
ΔI_{CC}	additional supply current per input	$V_I = V_{CC} - 2.1$ V; $I_O = 0$	4.5 to 5.5	–	–	410	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

AC CHARACTERISTICS

Type 74HC2G02

GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = –40 to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 5 and 6	2.0	–	26	95	ns
			4.5	–	9	19	ns
			6.0	–	8	16	ns
t_{THL}/t_{TLH}	output transition time	see Figs 5 and 6	2.0	–	19	95	ns
			4.5	–	7	19	ns
			6.0	–	5	16	ns
T_{amb} = –40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 5 and 6	2.0	–	–	110	ns
			4.5	–	–	22	ns
			6.0	–	–	20	ns
t_{THL}/t_{TLH}	output transition time	see Figs 5 and 6	2.0	–	–	125	ns
			4.5	–	–	25	ns
			6.0	–	–	20	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

Type 74HCT2G02

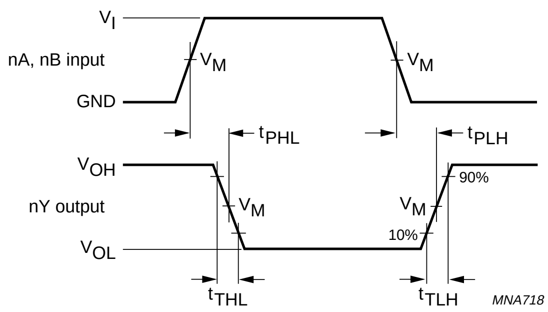
GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = –40 to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 5 and 6	4.5	–	12	24	ns
t_{THL}/t_{TLH}	output transition time	see Figs 5 and 6	4.5	–	6	19	ns
T_{amb} = –40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 5 and 6	4.5	–	–	29	ns
t_{THL}/t_{TLH}	output transition time	see Figs 5 and 6	4.5	–	–	22	ns

Note

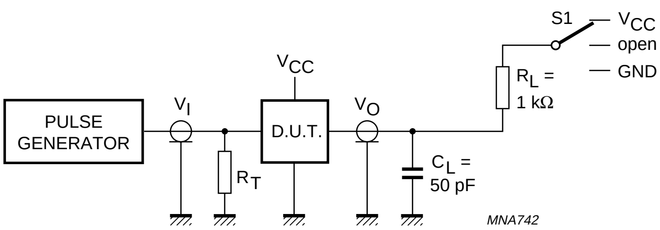
1. All typical values are measured at T_{amb} = 25 °C.

AC WAVEFORMS



For 74HC2G02: V_M = 50%; V_I = GND to V_{CC}.
For 74HCT2G02: V_M = 1.3 V; V_I = GND to 3.0 V.

Fig.5 The input (nA, nB) to output (nY) propagation delays and transition times.



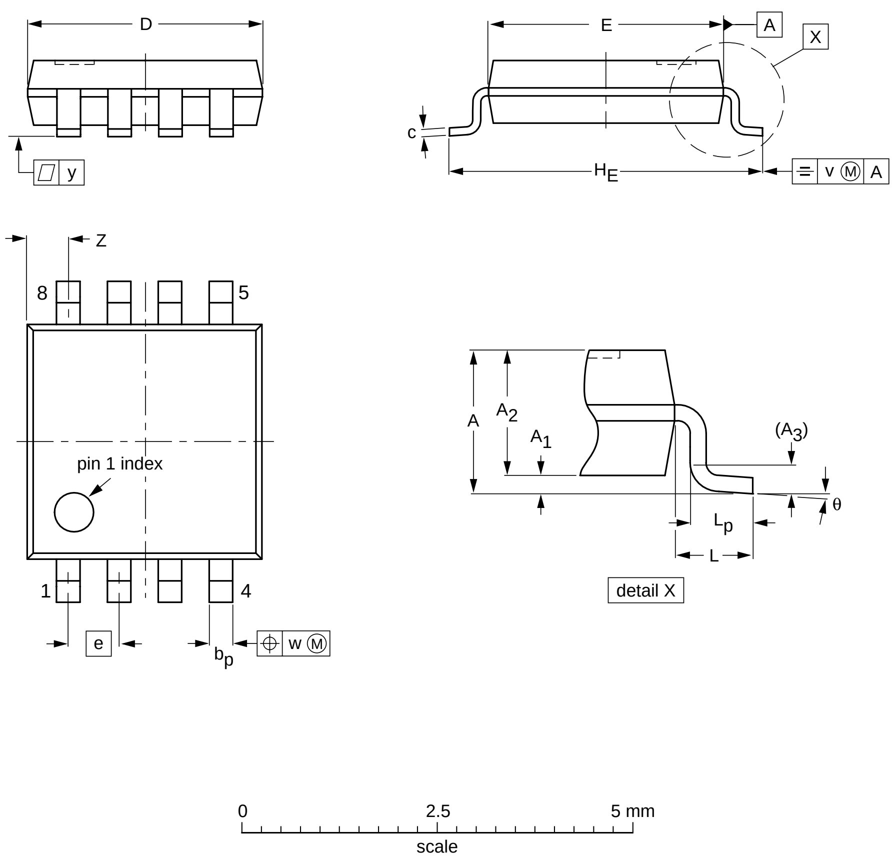
TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.6 Load circuitry for switching times.

PACKAGE OUTLINES

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

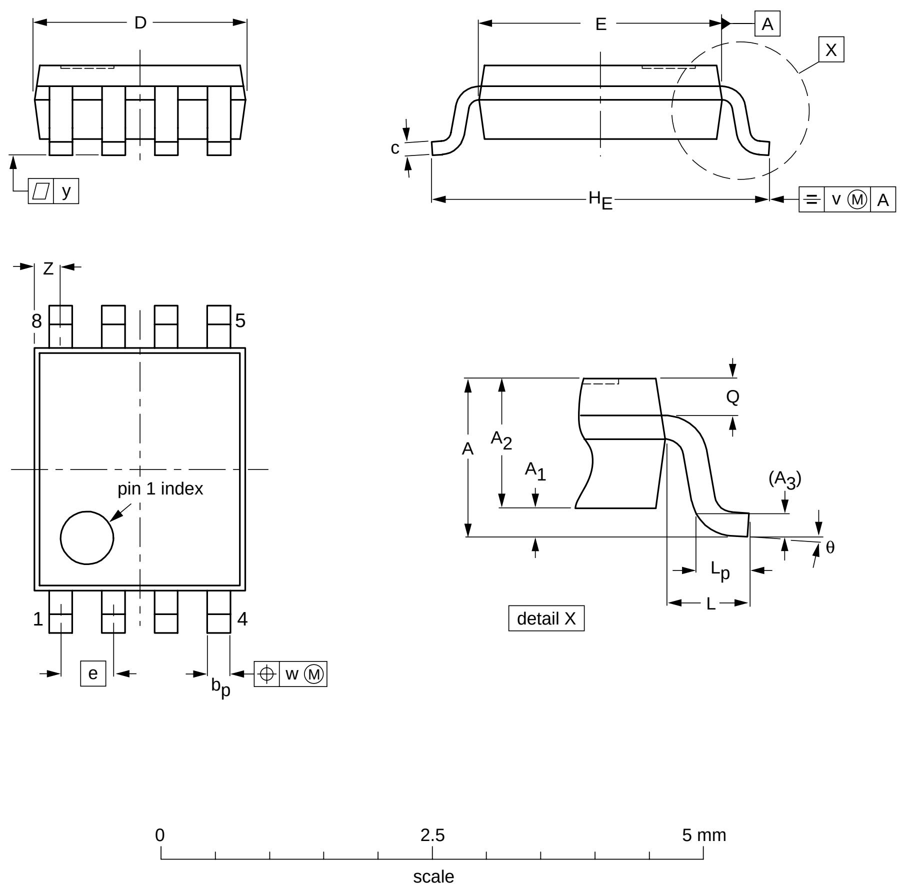
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	v	w	y	Z(1)	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE(1)	SOLDERING METHOD	
	WAVE	**REFLOW(2)**
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable(3)	suitable
PLCC(4), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(4)(5)	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended(6)	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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