

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF40175B** **MSI** Quadruple D-type flip-flop

Product specification  
File under Integrated Circuits, IC04

January 1995

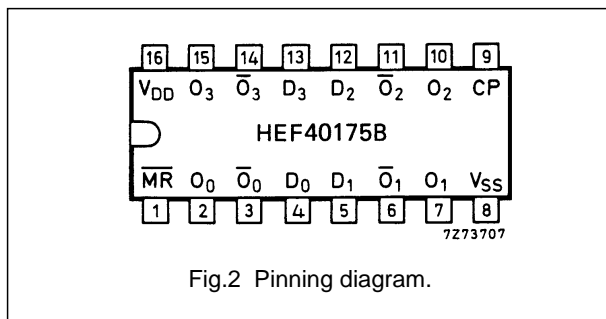
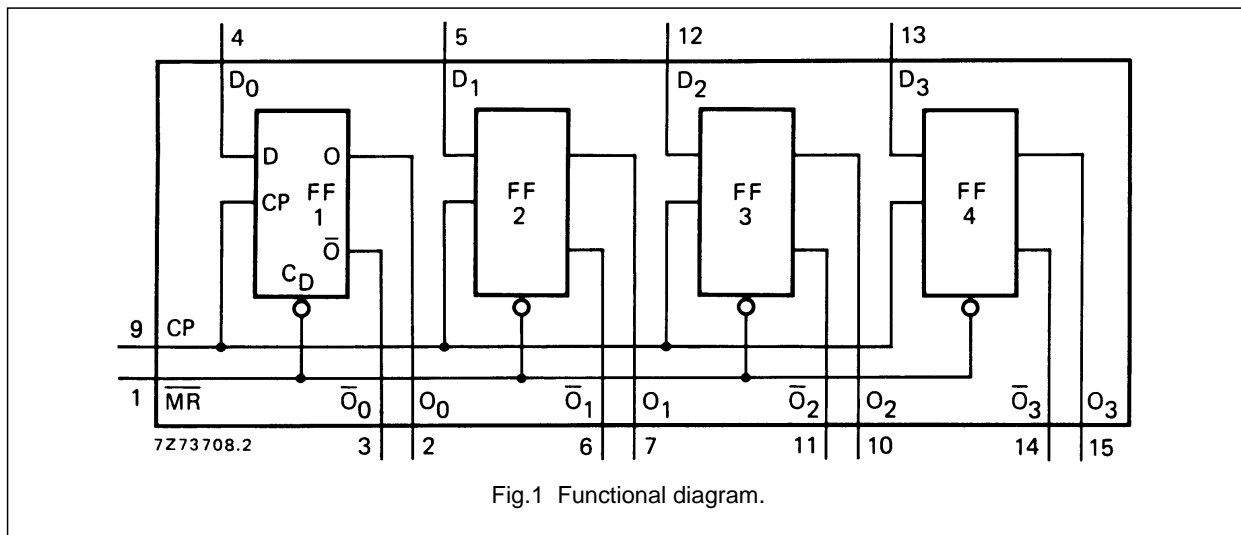
# Quadruple D-type flip-flop

## HEF40175B MSI

### DESCRIPTION

The HEF40175B is a quadruple edge-triggered D-type flip-flop with four data inputs ( $D_0$  to  $D_3$ ), a clock input (CP), an overriding asynchronous master reset input (MR), four buffered outputs ( $O_0$  to  $O_3$ ), and four complementary

buffered outputs ( $\bar{O}_0$  to  $\bar{O}_3$ ). Information on  $D_0$  to  $D_3$  is transferred to  $O_0$  to  $O_3$  on the LOW to HIGH transition of CP if MR is HIGH. When LOW, MR resets all flip-flops ( $O_0$  to  $O_3 = \text{LOW}$ ,  $\bar{O}_0$  to  $\bar{O}_3 = \text{HIGH}$ ), independent of CP and  $D_0$  to  $D_3$ .



### PINNING

- $D_0$  to  $D_3$  data inputs
- CP clock input (LOW to HIGH; edge-triggered)
- $\overline{\text{MR}}$  master reset input (active LOW)
- $O_0$  to  $O_3$  buffered outputs
- $\bar{O}_0$  to  $\bar{O}_3$  complementary buffered outputs

### FUNCTION TABLE

INPUTS			OUTPUTS	
CP	D	$\overline{\text{MR}}$	O	$\bar{O}$
	H	H	H	L
	L	H	L	H
	X	H	no change	no change
X	X	L	L	H

### Notes

- H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)  
X = state is immaterial
- = positive-going transition  
 = negative-going transition

- HEF40175BP(N): 16-lead DIL; plastic (SOT38-1)
  - HEF40175BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
  - HEF40175BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

### FAMILY DATA, I<sub>DD</sub> LIMITS category MSI

See Family Specifications

Quadruple D-type flip-flop

HEF40175B  
MSI

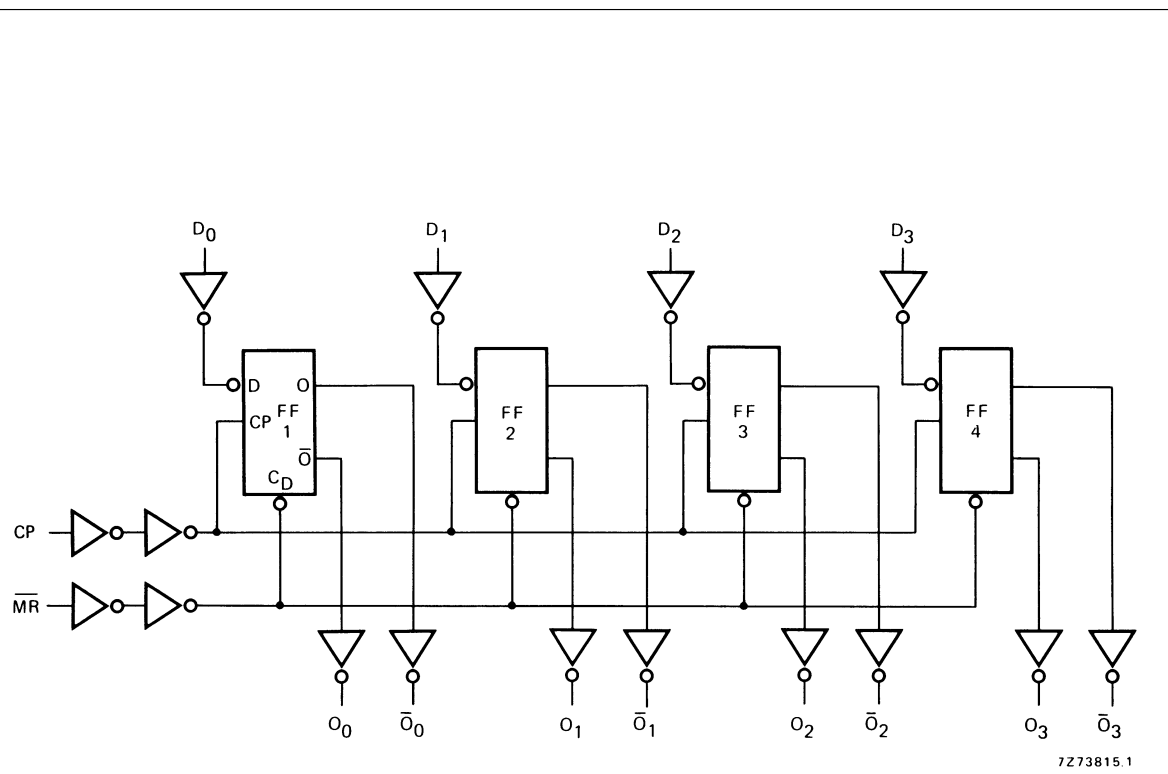


Fig.3 Logic diagram.

## Quadruple D-type flip-flop

HEF40175B  
MSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $CP \rightarrow O_n, \bar{O}_n$ HIGH to LOW	5	$t_{PHL}$		80	160	ns	53 ns + (0,55 ns/pF) $C_L$
	10		35	70	ns	24 ns + (0,23 ns/pF) $C_L$	
	15		25	50	ns	17 ns + (0,16 ns/pF) $C_L$	
LOW to HIGH	5	$t_{PLH}$		70	140	ns	43 ns + (0,55 ns/pF) $C_L$
	10		30	65	ns	19 ns + (0,23 ns/pF) $C_L$	
	15		25	45	ns	17 ns + (0,16 ns/pF) $C_L$	
$\bar{MR} \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$		75	155	ns	48 ns + (0,55 ns/pF) $C_L$
	10		30	65	ns	19 ns + (0,23 ns/pF) $C_L$	
	15		25	50	ns	17 ns + (0,16 ns/pF) $C_L$	
$\bar{MR} \rightarrow \bar{O}_n$ LOW to HIGH	5	$t_{PLH}$		70	140	ns	43 ns + (0,55 ns/pF) $C_L$
	10		30	65	ns	19 ns + (0,23 ns/pF) $C_L$	
	15		25	50	ns	17 ns + (0,16 ns/pF) $C_L$	
Output transition times HIGH to LOW	5	$t_{THL}$		60	120	ns	10 ns + (1,0 ns/pF) $C_L$
	10		30	60	ns	9 ns + (0,42 ns/pF) $C_L$	
	15		20	40	ns	6 ns + (0,28 ns/pF) $C_L$	
LOW to HIGH	5	$t_{TLH}$		60	120	ns	10 ns + (1,0 ns/pF) $C_L$
	10		30	60	ns	9 ns + (0,42 ns/pF) $C_L$	
	15		20	40	ns	6 ns + (0,28 ns/pF) $C_L$	
Set-up time $D_n \rightarrow CP$	5	$t_{su}$	60	30		ns	see also waveforms Fig.4
	10		20	10		ns	
	15		15	5		ns	
Hold time $D_n \rightarrow CP$	5	$t_{hold}$	25	-5		ns	
	10		10	0		ns	
	15		10	0		ns	
Minimum clock pulse width; LOW	5	$t_{WCPL}$	90	45		ns	
	10		35	15		ns	
	15		25	10		ns	
Minimum $\bar{MR}$ pulse width; LOW	5	$t_{WMRL}$	80	40		ns	
	10		30	15		ns	
	15		20	10		ns	
Recovery time for $\bar{MR}$	5	$t_{RMR}$	0	-30		ns	
	10		0	-20		ns	
	15		0	-15		ns	
Maximum clock pulse frequency	5	$f_{max}$	5	11		MHz	
	10		15	30		MHz	
	15		20	45		MHz	

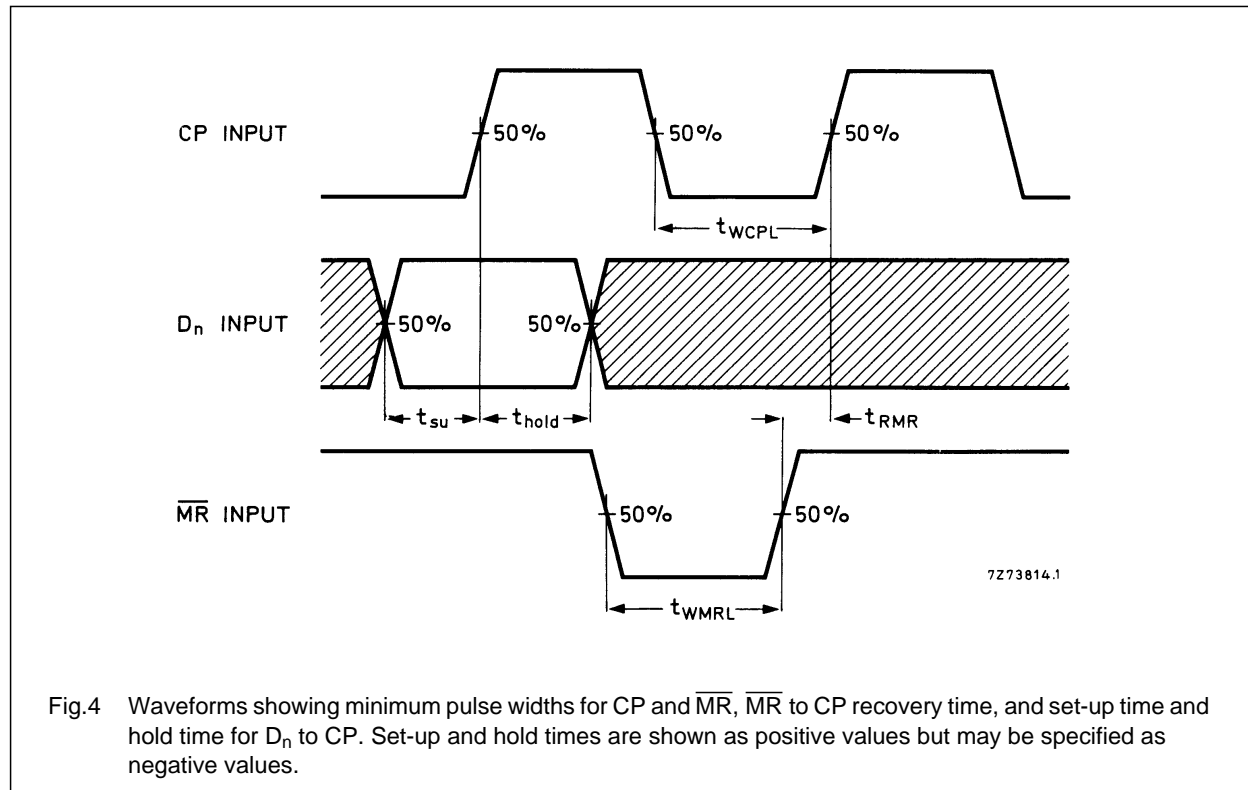
## Quadruple D-type flip-flop

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## AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ )	
Dynamic power dissipation per package (P)	5	$2000 f_i + \sum (f_o C_L) \times V_{DD}^2$	where
	10	$8400 f_i + \sum (f_o C_L) \times V_{DD}^2$	$f_i$ = input freq. (MHz)
	15	$22\,500 f_i + \sum (f_o C_L) \times V_{DD}^2$	$f_o$ = output freq. (MHz)
			$C_L$ = load capacitance (pF)
			$\sum (f_o C_L)$ = sum of outputs
			$V_{DD}$ = supply voltage (V)



## APPLICATION INFORMATION

Some examples of applications for the HEF40175B are:

- Shift registers
- Buffer/storage register
- Pattern generator