

DATA SHEET

74HC1G125; 74HCT1G125 Bus buffer/line driver; 3-state

Product specification
File under Integrated Circuits, IC06

1998 Nov 10

Bus buffer/line driver; 3-state

74HC1G125; 74HCT1G125

FEATURES

- Wide operating voltage:
2.0 to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Very small 5 pins package
- Output capability: bus driver.

DESCRIPTION

The 74HC1G/HCT1G125 is a high-speed Si-gate CMOS device.

The 74HC1G/HCT1G125 provides one non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input (\overline{OE}). A HIGH at \overline{OE} causes the output as assume a high-impedance OFF-state.

The bus driver output currents are equal compared to the 74HC/HCT125.

FUNCTION TABLE

See note 1.

INPUTS		OUTPUT
\overline{OE}	inA	outY
L	L	L
L	H	H
H	X	Z

Note

1. H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF state.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f \leq 6.0\text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
			HC1G	HCT1G	
t_{PHL}/t_{PLH}	propagation delay inA to outY	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	9	10	ns
C_I	input capacitance		1.5	1.5	pF
C_{PD}	power dissipation capacitance	notes 1 and 2	30	27	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

2. For HC1G the condition is $V_I = \text{GND to } V_{CC}$.

For HCT1G the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$.

PINNING

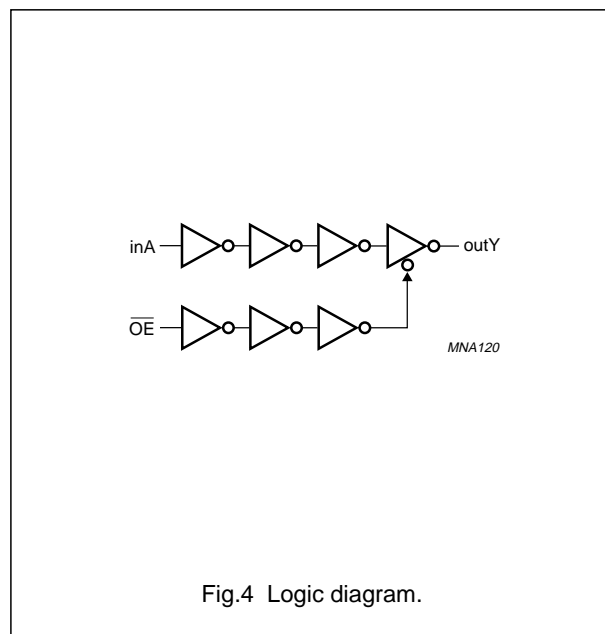
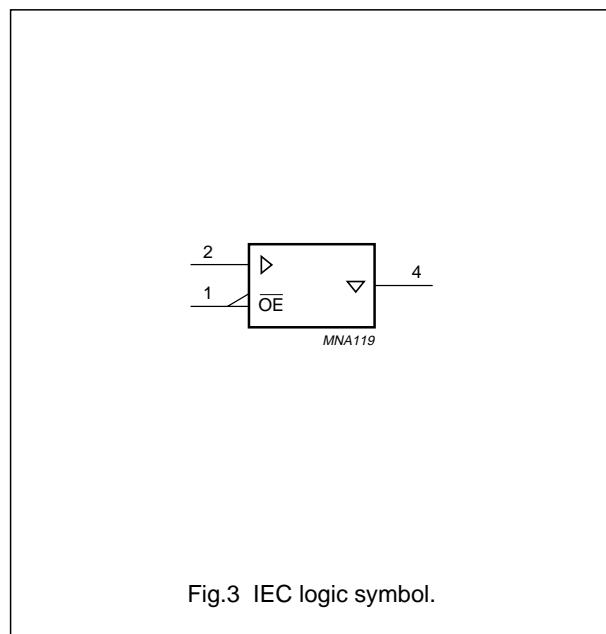
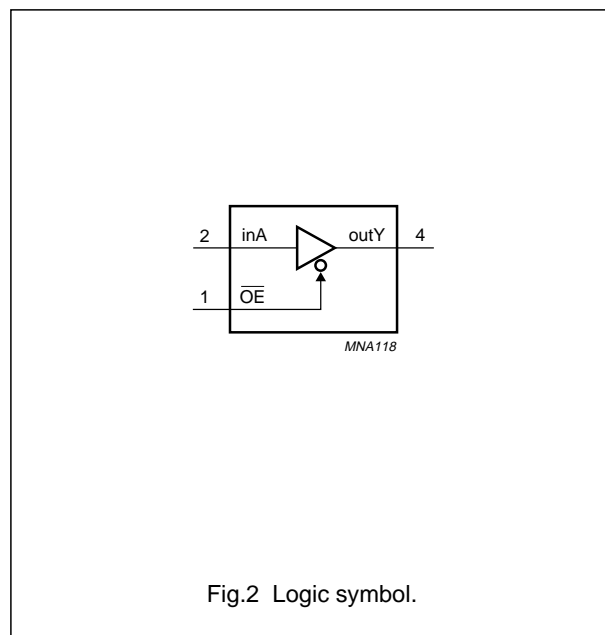
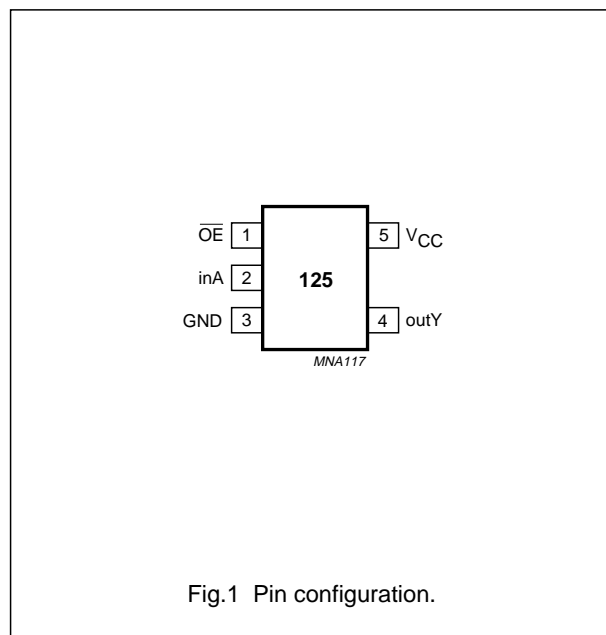
PIN	SYMBOL	DESCRIPTION
1	\overline{OE}	output enable input
2	inA	data input
3	GND	ground (0 V)
4	outY	data output
5	V_{CC}	DC supply voltage

Bus buffer/line driver; 3-state

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ORDERING INFORMATION

OUTSIDE NORTH AMERICA	PACKAGES					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC1G125GW	-40 to +125 °C	5	SC-88A	plastic	SOT353	HM
74HCT1G125GW		5	SC-88A	plastic	SOT353	TM



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC1G04			74HCT1G04			UNIT	CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	input voltage	0	–	V_{CC}	0	–	V_{CC}	V	
V_O	output voltage	0	–	V_{CC}	0	–	V_{CC}	V	
T_{amb}	operating ambient temperature	–40	+25	+125	–40	+25	+125	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times except for Schmitt trigger inputs	–	–	1000	–	–	–	ns	$V_{CC} = 2.0\text{ V}$
		–	–	500	–	–	500	ns	$V_{CC} = 4.5\text{ V}$
		–	–	400	–	–	–	ns	$V_{CC} = 6.0\text{ V}$

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		–0.5	+7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$; note 1	–	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$; note 1	–	20	mA
$\pm I_O$	DC output source or sink current standard outputs	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$; note 1	–	12.5	mA
$\pm I_{CC}$	DC V_{CC} or GND current for types with standard outputs	note 1	–	25	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	temperature range: –40 to +125 °C; note 2	–	200	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 55 °C the value of P_D derates linearly with 2.5 mW/K.

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DC CHARACTERISTICS

Family 74HC1G

Additional type data to the recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	T _{amb} (°C)					UNIT	TEST CONDITIONS	
		-40 to +85			-40 to +125			V _{CC} (V)	OTHER
		MIN.	TYP. ⁽¹⁾	MAX.	MIN.	MAX.			
V _{IH}	HIGH-level input voltage	1.5	1.2	–	1.5	–	V	2.0	
		3.15	2.4	–	3.15	–		4.5	
		4.2	3.2	–	4.2	–		6.0	
V _{IL}	LOW-level input voltage	–	0.8	0.5	–	0.5	V	2.0	
		–	2.1	1.35	–	1.35		4.5	
		–	2.8	1.8	–	1.8		6.0	
V _{OH}	HIGH-level output voltage; all outputs	1.9	2.0	–	1.9	–	V	2.0	V _I = V _{IH} or V _{IL} ; –I _O = 20 μA
		4.4	4.5	–	4.4	–		4.5	
		5.9	6.0	–	5.9	–		6.0	
V _{OH}	HIGH-level output voltage; standard outputs	4.13	4.32	–	3.7	–	V	4.5	V _I = V _{IH} or V _{IL} ; –I _O = 2.0 mA
		5.63	5.81	–	5.2	–		6.0	V _I = V _{IH} or V _{IL} ; –I _O = 2.6 mA
V _{OL}	LOW-level output voltage; all outputs	–	0	0.1	–	0.1	V	2.0	V _I = V _{IH} or V _{IL} ; I _O = 20 μA
		–	0	0.1	–	0.1		4.5	
		–	0	0.1	–	0.1		6.0	
V _{OL}	LOW-level output voltage; standard outputs	–	0.15	0.33	–	0.4	V	4.5	V _I = V _{IH} or V _{IL} ; I _O = 2.0 mA
		–	0.16	0.33	–	0.4		6.0	V _I = V _{IH} or V _{IL} ; I _O = 2.6 mA
I _I	input leakage current	–	–	1.0	–	1.0	μA	6.0	V _I = V _{CC} or GND
I _{CC}	quiescent supply current	–	–	10	–	20	μA	6.0	V _I = V _{CC} or GND; I _O = 0

Note

1. All typical values are measured at T_{amb} = 25 °C.

Bus buffer/line driver; 3-state

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Family 74HCT1G

Additional type data to the recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	T _{amb} (°C)					UNIT	TEST CONDITIONS	
		-40 to +85			-40 to +125			V _{CC} (V)	OTHER
		MIN.	TYP. ⁽¹⁾	MAX.	MIN.	MAX.			
V _{IH}	HIGH-level input voltage	2.0	1.6	–	2.0	–	V	4.5 to 5.5	
V _{IL}	LOW-level input voltage	–	1.2	0.8	–	0.8	V	4.5 to 5.5	
V _{OH}	HIGH-level output voltage; all outputs	4.4	4.5	–	4.4	–	V	4.5	V _I = V _{IH} or V _{IL} ; –I _O = 20 μA
V _{OH}	HIGH-level output voltage; standard outputs	4.13	4.32	–	3.7	–	V	4.5	V _I = V _{IH} or V _{IL} ; –I _O = 2.0 mA
V _{OL}	LOW-level output voltage; all outputs	–	0	0.1	–	0.1	V	4.5	V _I = V _{IH} or V _{IL} ; I _O = 20 μA
V _{OL}	LOW-level output voltage; standard outputs	–	0.15	0.33	–	0.4	V	4.5	V _I = V _{IH} or V _{IL} ; I _O = 2.0 mA
I _I	input leakage current	–	–	1.0	–	1.0	μA	5.5	V _I = V _{CC} or GND
I _{CC}	quiescent supply current	–	–	10.0	–	20	μA	5.5	V _I = V _{CC} or GND; I _O = 0
ΔI _{CC}	additional supply current per input	–	–	500	–	850	μA	4.5 to 5.5	V _I = V _{CC} – 2.1; I _O = 0

Note

1. All typical values are measured at T_{amb} = 25 °C.

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AC CHARACTERISTICS

Type 74HC1G125

GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		-40 to +85			-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP. ⁽¹⁾	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay inA to outY	–	24	125	–	150	ns	2.0	see Figs 5 and 7
		–	10	25	–	30	ns	4.5	
		–	8	21	–	26	ns	6.0	
t_{PZH}/t_{PZL}	3-state output enable time \overline{OE} to outY	–	19	155	–	190	ns	2.0	see Figs 6 and 7
		–	9	31	–	38	ns	4.5	
		–	7	26	–	32	ns	6.0	
t_{PHZ}/t_{PLZ}	3-state output disable time \overline{OE} to outY	–	18	155	–	190	ns	2.0	see Figs 6 and 7
		–	12	31	–	38	ns	4.5	
		–	11	26	–	32	ns	6.0	

Note

1. All typical values are measured at $T_{amb} = 25$ °C.

Type 74HCT1G125

GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		-40 to +85			-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP. ⁽¹⁾	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay inA to outY	–	11	30	–	36	ns	4.5	see Figs 5 and 7
t_{PZH}/t_{PZL}	3-state output enable time \overline{OE} to outY	–	10	35	–	42	ns	4.5	see Figs 6 and 7
t_{PHZ}/t_{PLZ}	3-state output disable time \overline{OE} to outY	–	11	31	–	38	ns	4.5	see Figs 6 and 7

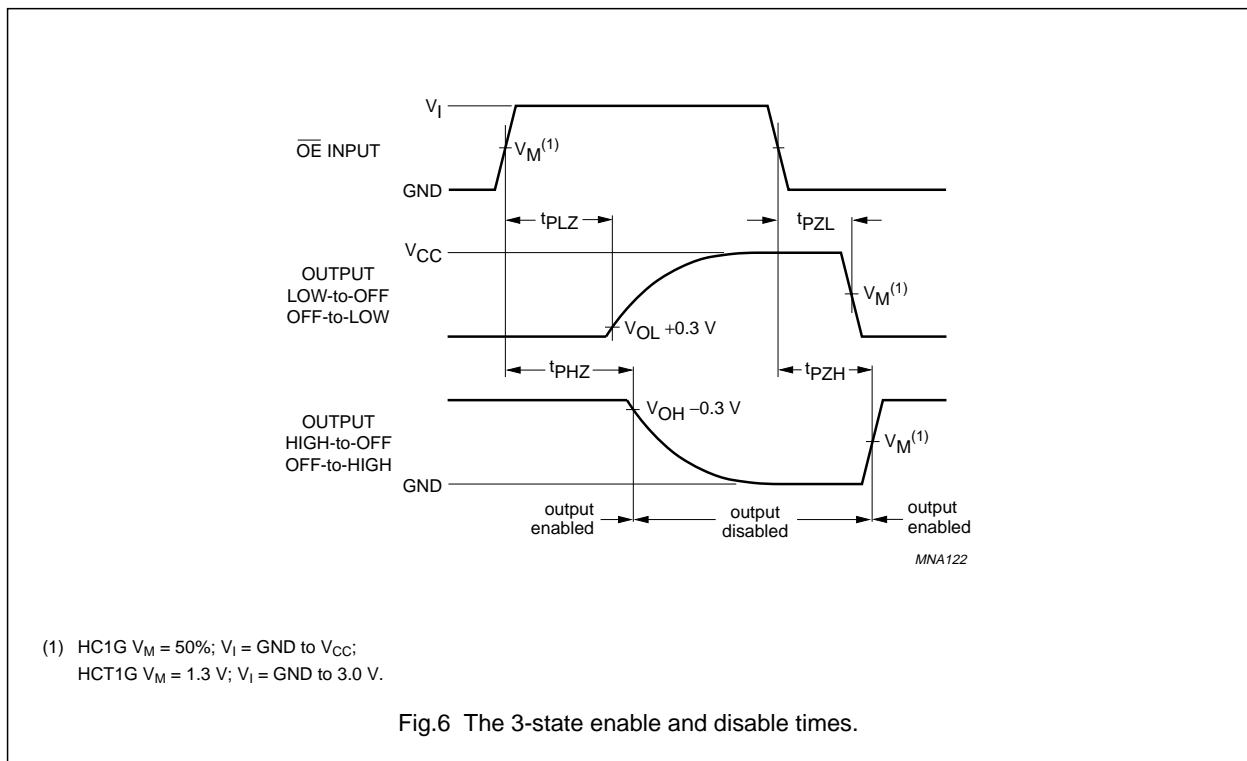
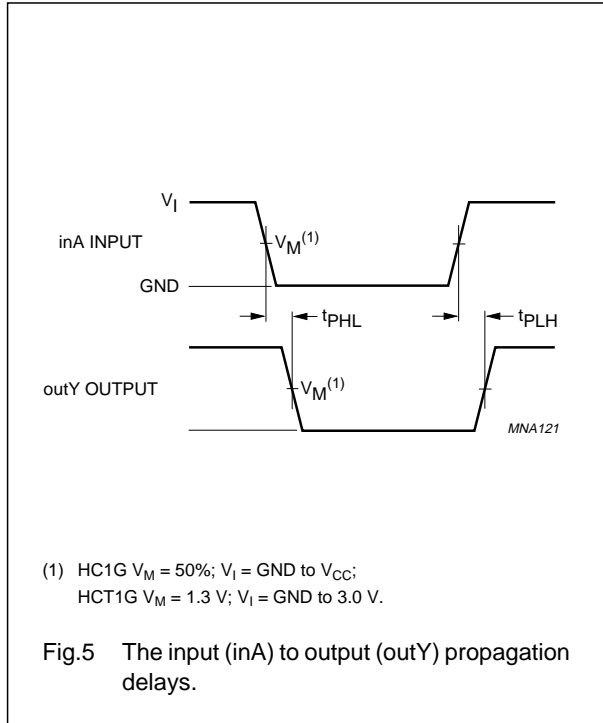
Note

1. All typical values are measured at $T_{amb} = 25$ °C.

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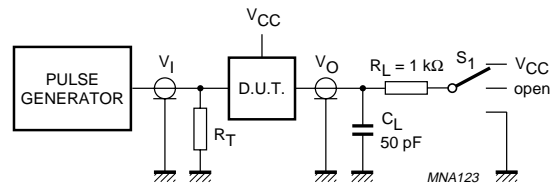
74HC1G125; 74HCT1G125

AC WAVEFORMS



Bus buffer/line driver; 3-state

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Definitions for test circuit;

C_L = load capacitance including jig and probe capacitance.
(See "AC characteristics")

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

TEST	S_1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

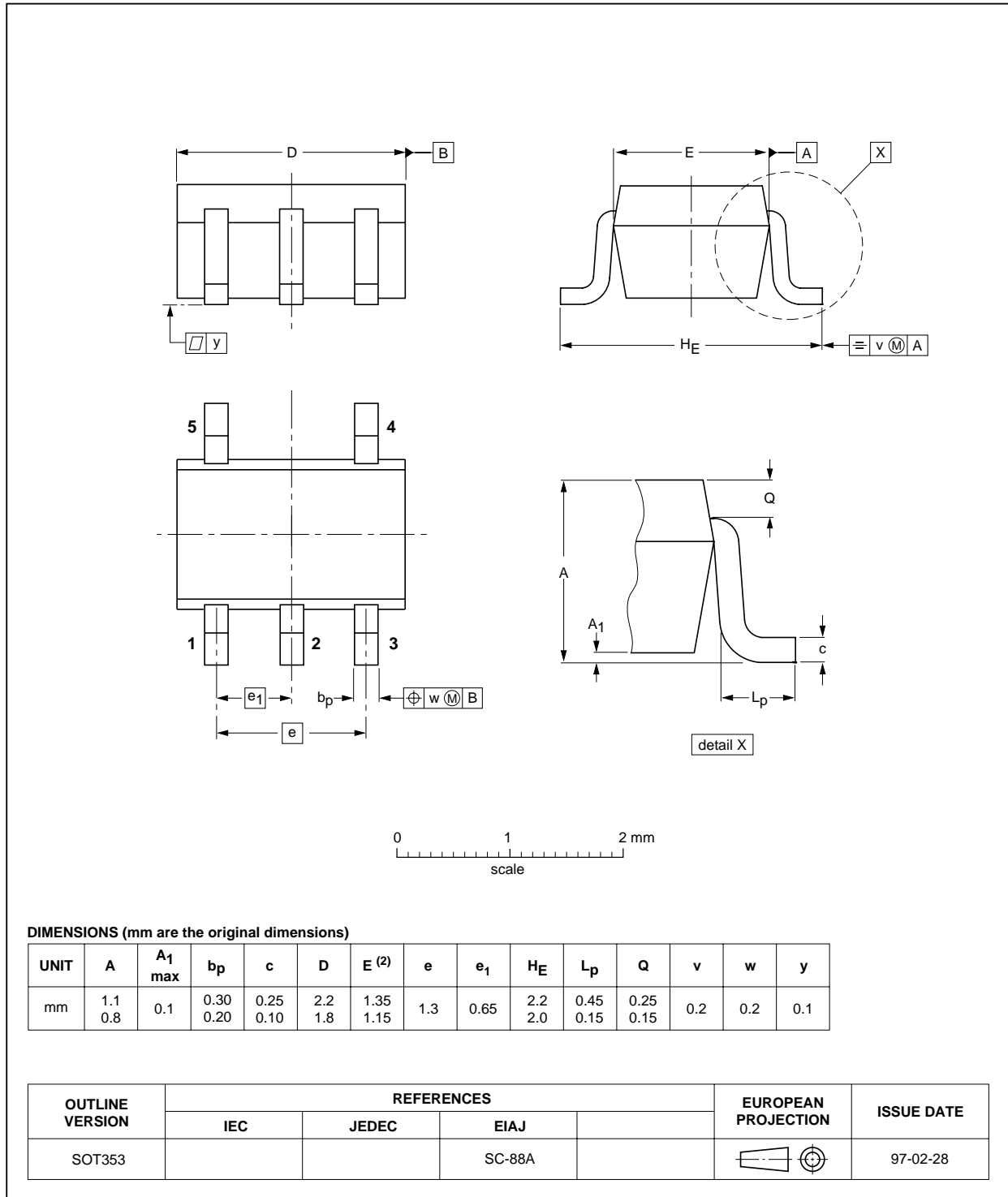
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PACKAGE OUTLINE

Plastic surface mounted package; 5 leads

SOT353



Bus buffer/line driver; 3-state**74HC1G125; 74HCT1G125**

SOLDERING**Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted IC's, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering IC's can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

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Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bouchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
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China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
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2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax. +381 11 635 777

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International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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