

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4007UB**

### **gates**

Dual complementary pair and inverter

Product specification  
File under Integrated Circuits, IC04

January 1995

# Dual complementary pair and inverter

# HEF4007UB gates

### DESCRIPTION

The HEF4007UB is a dual complementary pair and an inverter with access to each device. It has three n-channel and three p-channel enhancement mode MOS transistors.

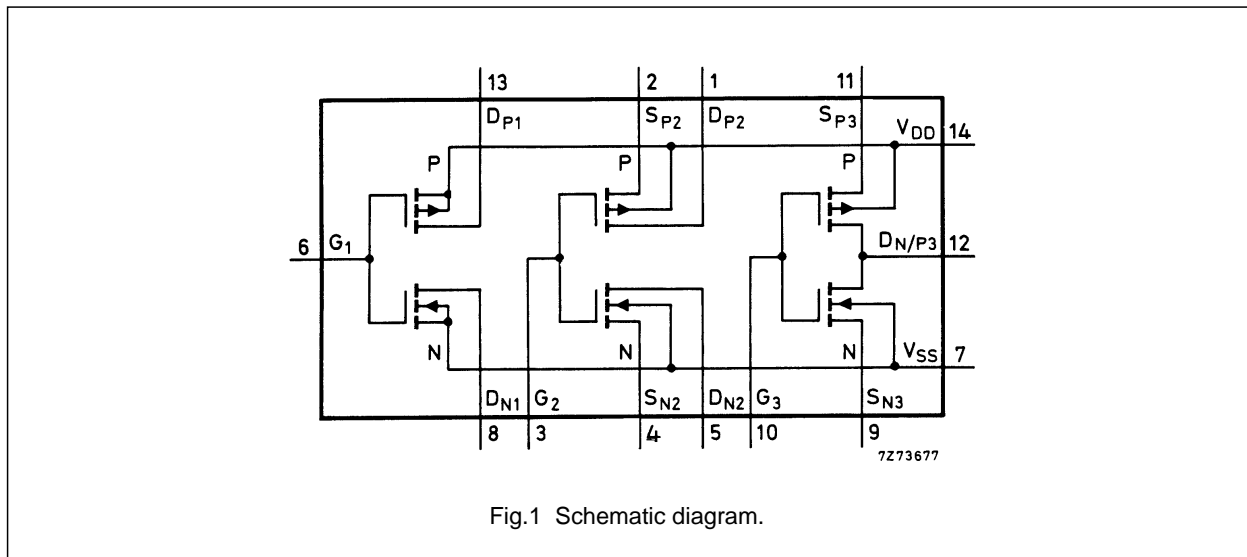


Fig.1 Schematic diagram.

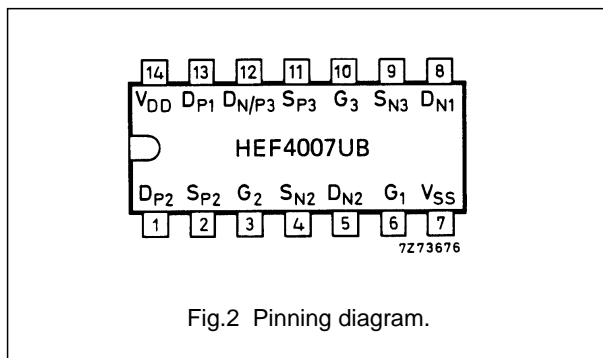


Fig.2 Pinning diagram.

### PINNING

- SP<sub>2</sub>, SP<sub>3</sub> source connections to 2nd and 3rd p-channel transistors
- DP<sub>1</sub>, DP<sub>2</sub> drain connections from the 1st and 2nd p-channel transistors
- DN<sub>1</sub>, DN<sub>2</sub> drain connections from the 1st and 2nd n-channel transistors
- SN<sub>2</sub>, SN<sub>3</sub> source connections to the 2nd and 3rd n-channel transistors
- DN/P<sub>3</sub> common connection to the 3rd p-channel and n-channel transistor drains
- G<sub>1</sub> to G<sub>3</sub> gate connections to n-channel and p-channel of the three transistor pairs

- HEF4007UBP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4007UBD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4007UBT(D): 14-lead SO; plastic (SOT108-1)
- ( ): Package Designator North America

### FAMILY DATA, I<sub>DD</sub> LIMITS category GATES

See Family Specifications for V<sub>IH</sub>/V<sub>IL</sub> unbuffered stages

## Dual complementary pair and inverter

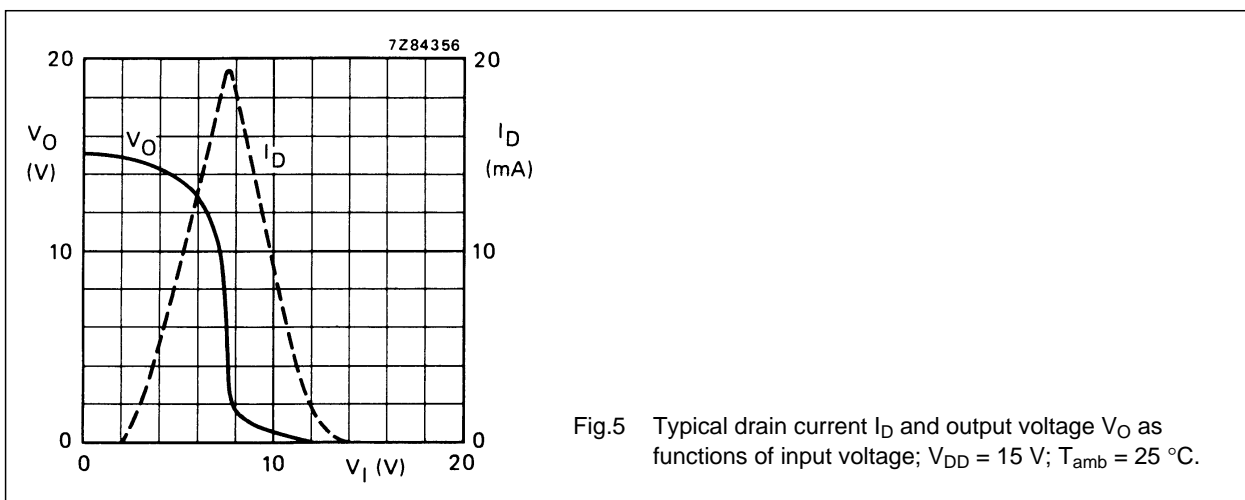
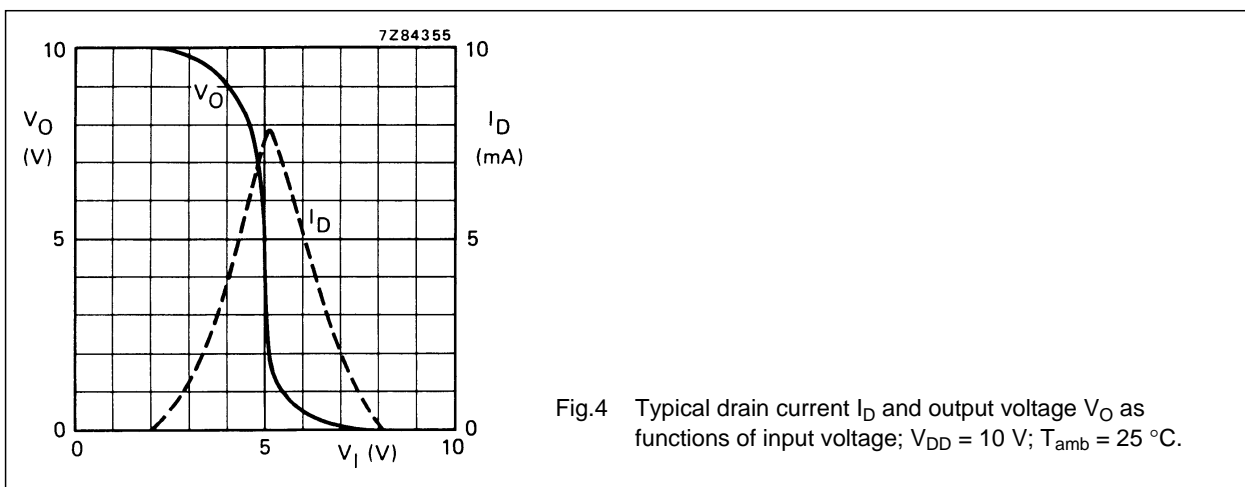
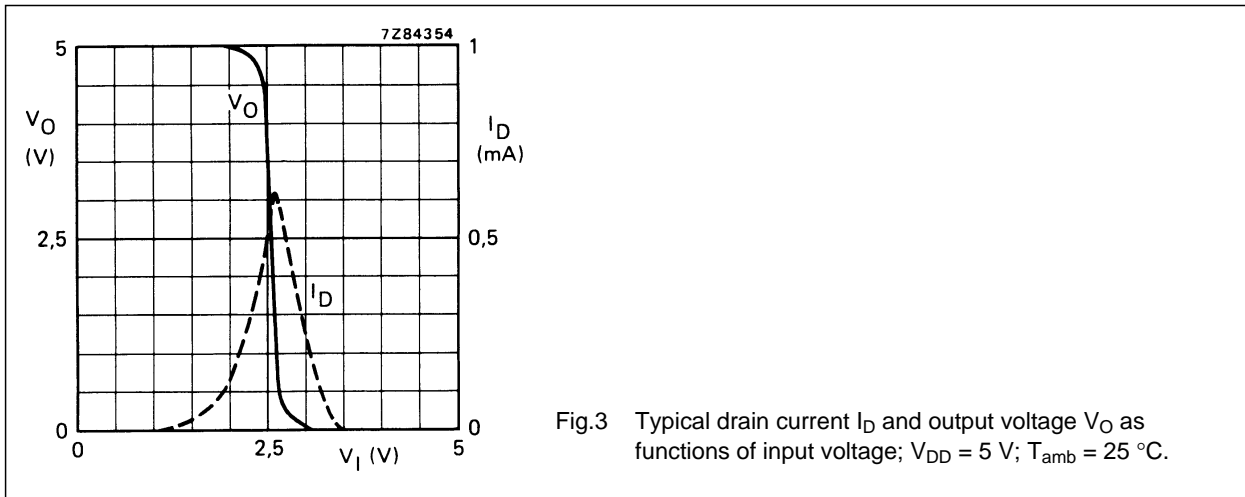
HEF4007UB  
gates**AC CHARACTERISTICS** $V_{SS} = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF; input transition times  $\leq 20$  ns

	$V_{DD}$ V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays $G_n \rightarrow D_N$ ; $D_P$ HIGH to LOW	5	$t_{PHL}$	40	80	ns	$13 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		20	40	ns	$9 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		15	30	ns	$7 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5	$t_{PLH}$	40	75	ns	$13 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		20	40	ns	$9 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		15	30	ns	$7 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	$t_{THL}$	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5	$t_{TLH}$	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu$ W)	
Dynamic power dissipation per package (P)	5	$4500 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$20\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$50\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

Dual complementary pair and inverter

HEF4007UB  
gates



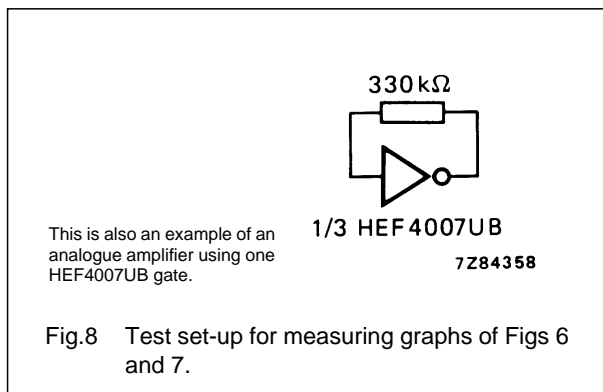
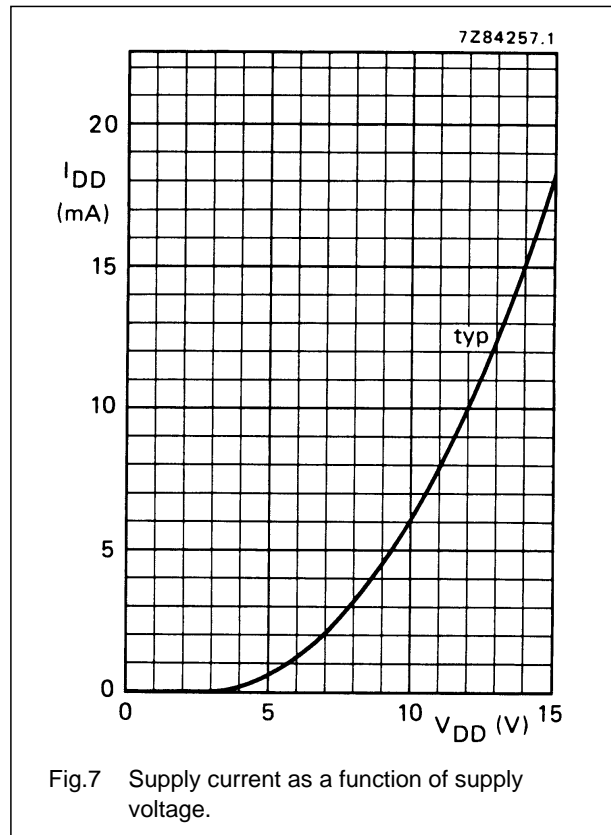
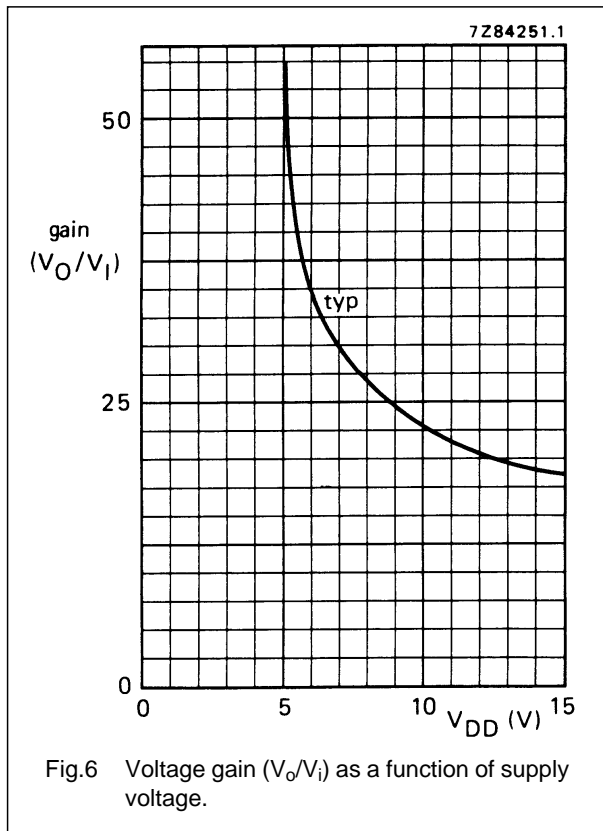
Dual complementary pair and inverter

HEF4007UB  
gates

APPLICATION INFORMATION

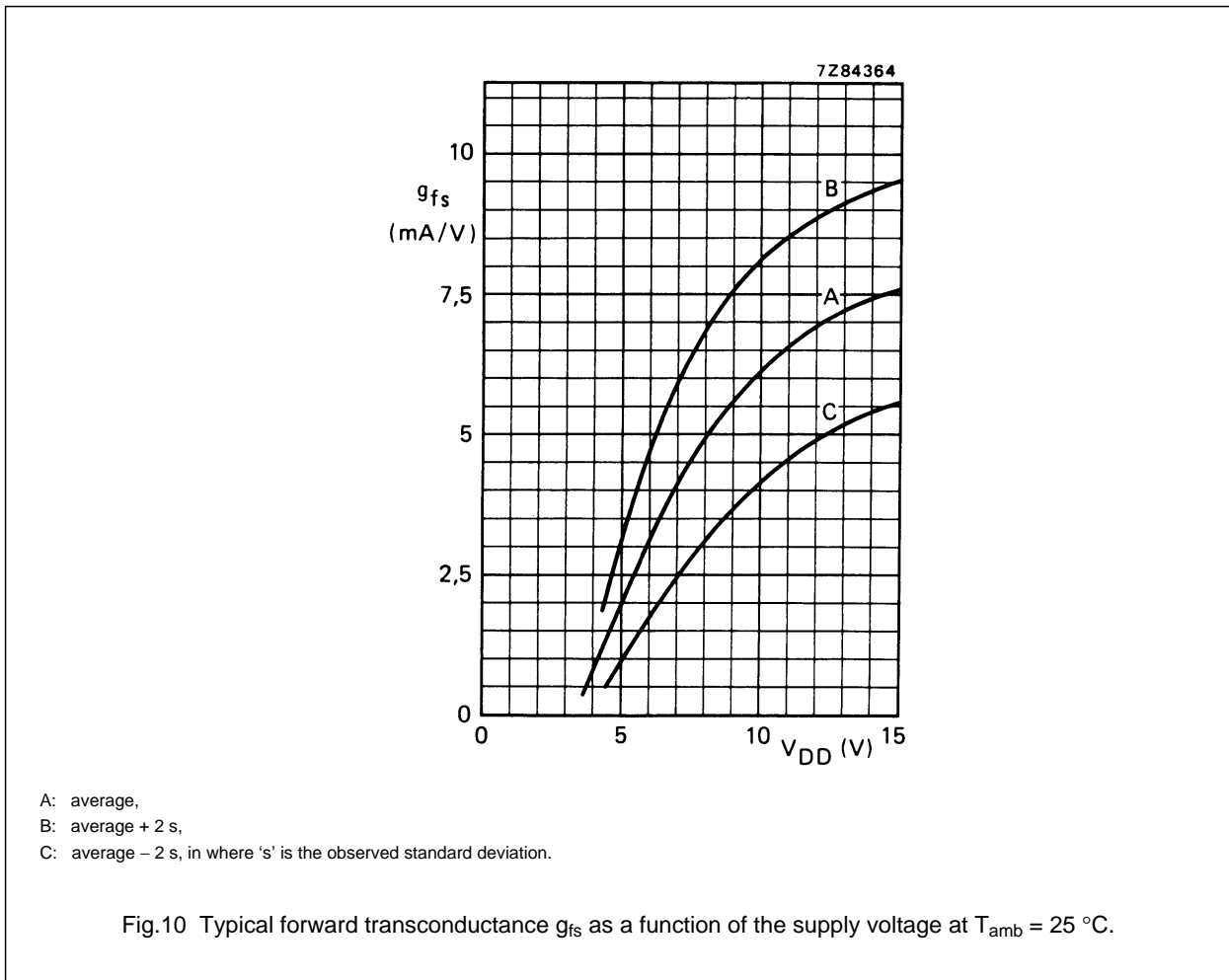
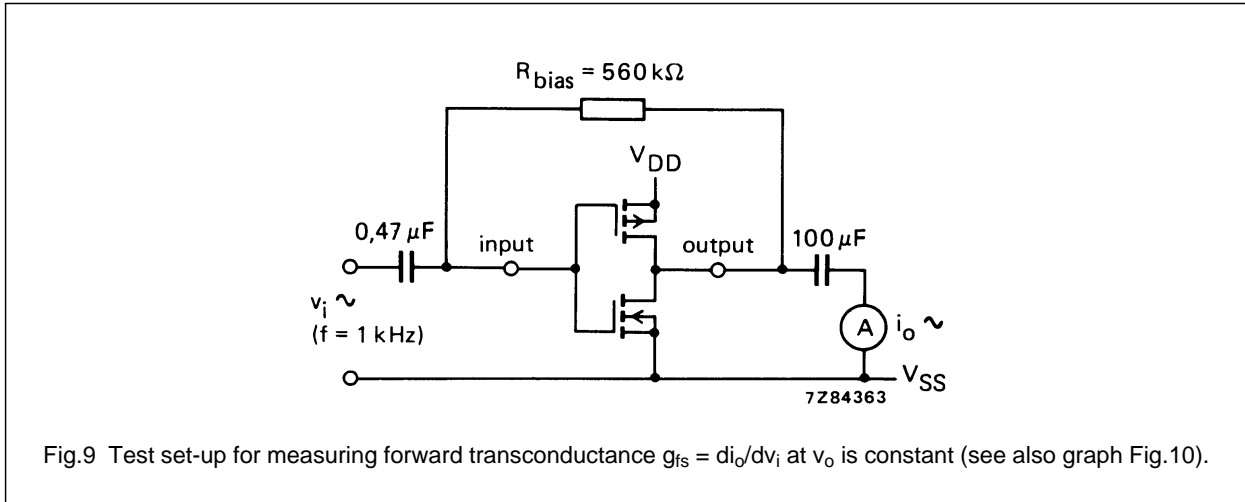
Some examples of applications for the HEF4007UB are:

- High input impedance amplifiers
- Linear amplifiers
- (Crystal) oscillators
- High-current sink and source drivers
- High impedance buffers.



Dual complementary pair and inverter

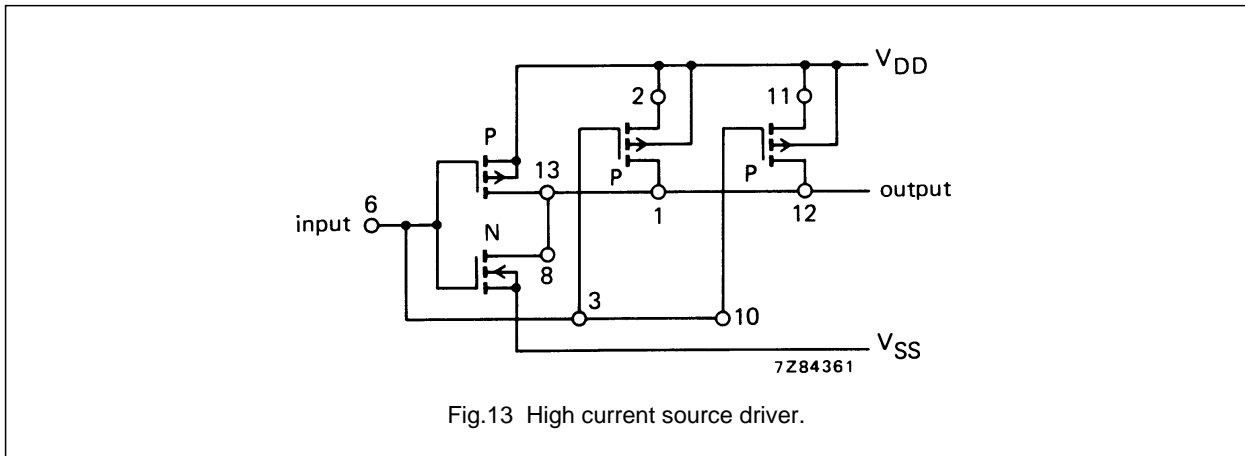
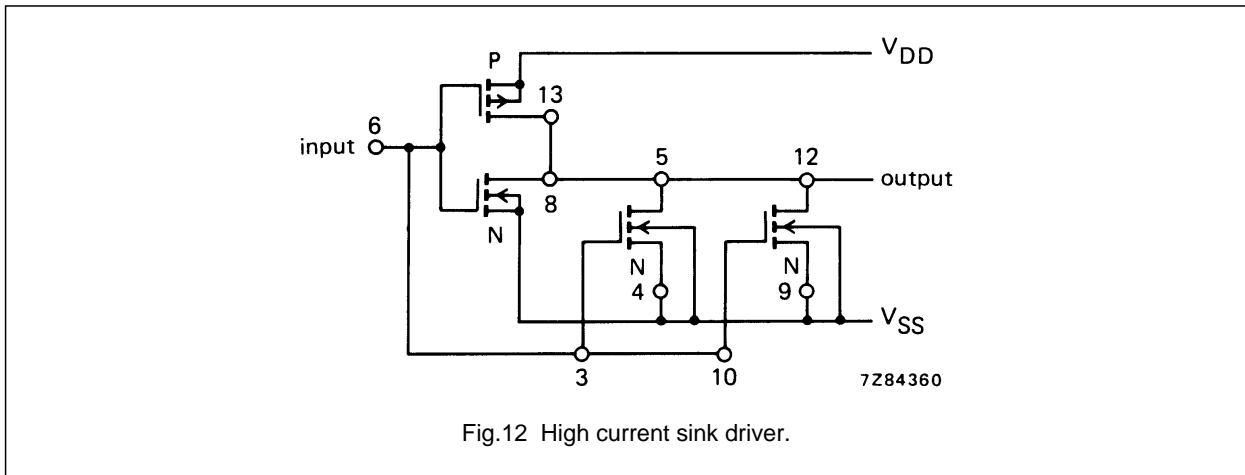
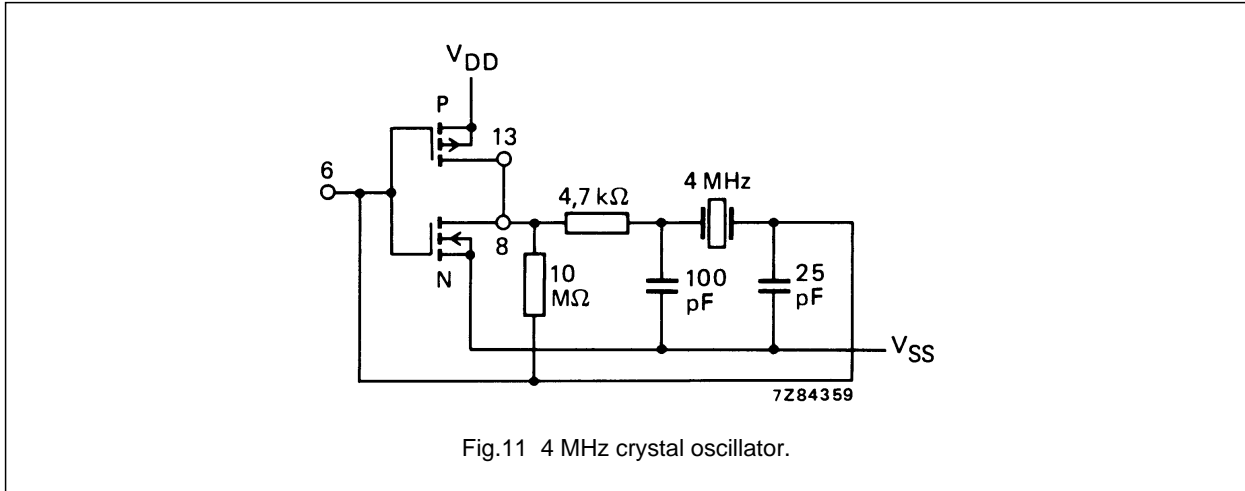
HEF4007UB  
gates



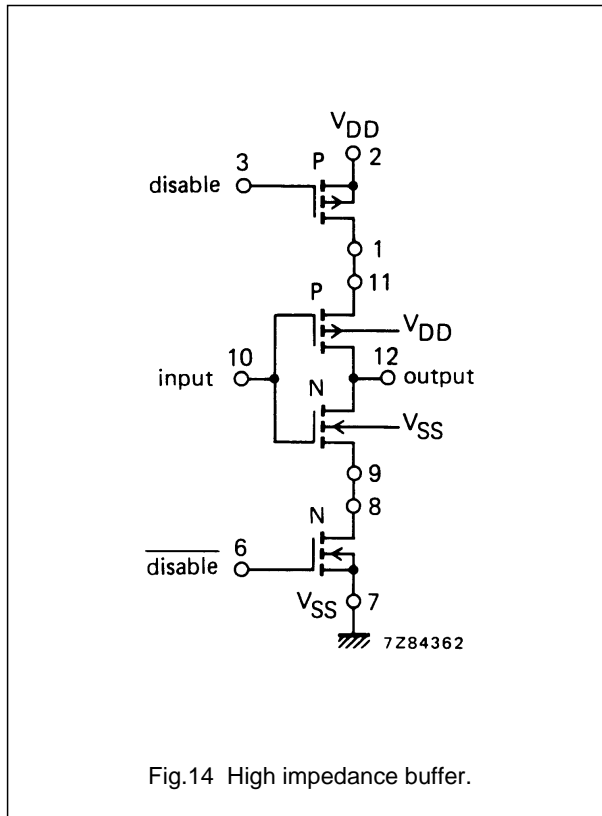
Dual complementary pair and inverter

HEF4007UB  
gates

Figures 11 to 14 show some applications in which the HEF4007UB is used.



## Dual complementary pair and inverter

HEF4007UB  
gates

FUNCTION TABLE for Fig.14.

INPUT	DISABLE	OUTPUT
H	L	L
L	L	H
X	H	open

**Notes**

- H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)  
X = state is immaterial

**NOTE**

Rules for maintaining electrical isolation between transistors and monolithic substrate:

- Pin number 14 must be maintained at the most positive (or equally positive) potential with respect to any other pin of the HEF4007UB.
- Pin number 7 must be maintained at the most negative (or equally negative) potential with respect to any other pin of the HEF4007UB.

Violation of these rules will result in improper transistor operation and/or possible permanent damage to the HEF4007UB.