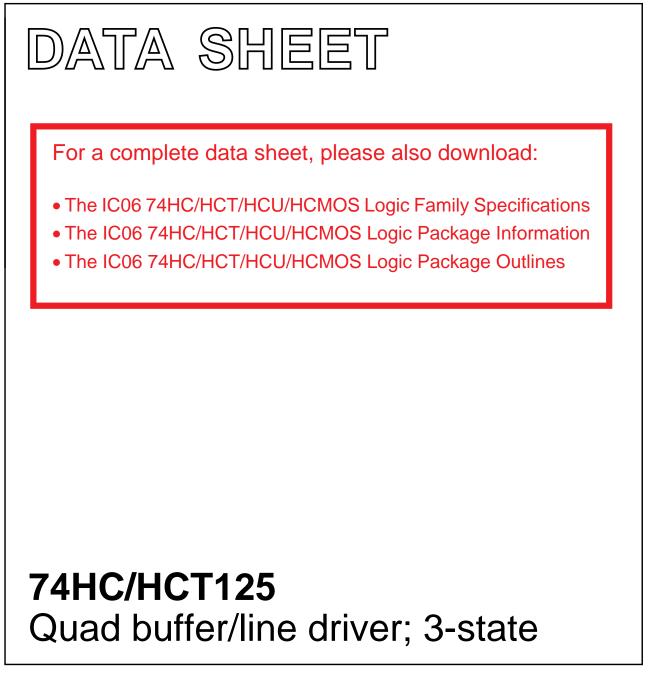
# INTEGRATED CIRCUITS



Product specification File under Integrated Circuits, IC06 December 1990



**Semiconductors** 

**Philips** 

### 74HC/HCT125

### FEATURES

- Output capability: bus driver
- I<sub>CC</sub> category: MSI

#### **GENERAL DESCRIPTION**

The 74HC/HCT125 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT125 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ( $\overline{nOE}$ ). A HIGH at  $\overline{nOE}$  causes the outputs to assume a HIGH impedance OFF-state.

The "125" is identical to the "126" but has active LOW enable inputs.

### QUICK REFERENCE DATA

$GND = 0 V; T_{amb}$	= 25 °C;	$t_r = t_f = 6 \text{ ns}$
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SYMBOL	PARAMETER	CONDITIONS	ТҮР			
STWBOL	FARAMETER	CONDITIONS	НС	нст		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	$C_{L} = 15 \text{ pF}; V_{CC} = 5 \text{ V}$	9	12	ns	
CI	input capacitance		3.5	3.5	pF	
C <sub>PD</sub>	power dissipation capacitance per buffer	notes 1 and 2	22	24	pF	

#### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz

 $f_o = output frequency in MHz$ 

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$ 

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub> For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

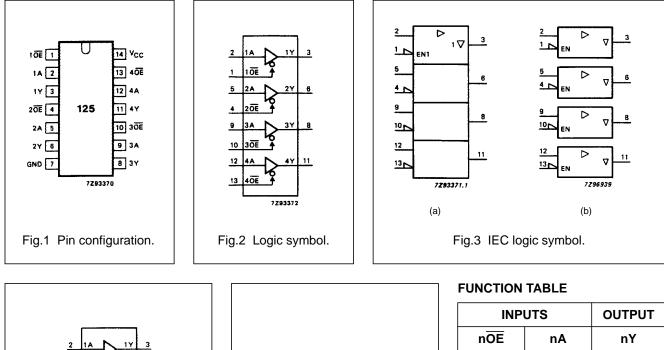
#### **ORDERING INFORMATION**

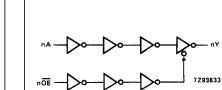
See "74HC/HCT/HCU/HCMOS Logic Package Information".

# 74HC/HCT125

### **PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION	
1, 4, 10, 13	$1\overline{OE}$ to $4\overline{OE}$	outputs enable inputs (active LOW)	
2, 5, 9, 12	1A to 4A	data inputs	
3, 6, 8, 11	1Y to 4Y	data outputs	
7	GND	ground (0 V)	
14	V <sub>CC</sub>	positive supply voltage	



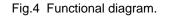


INP	OUTPUT	
nOE	nA	nY
L	L	L
L	н	Н
Н	Х	Z

### Note

H = HIGH voltage level
L = LOW voltage level
X = don't care

Z = high impedance OFF-state



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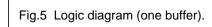
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9

10

12

13



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## 74HC/HCT125

### DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver  $I_{CC}$  category: MSI

### AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$ 

	PARAMETER	T <sub>amb</sub> (°C)								TEST CONDITIONS	
SYMBOL		74HC									WAVEFORMS
		+25			-40 to +85 -40 t		-40 to +125		V <sub>CC</sub> (V)	WAVEFORINS	
		min.	typ.	max.	min.	max.	min.	max.		(•)	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay		30	100		125		150	ns	2.0	Fig.6
	nA to nY		11	20		25		30		4.5	
			9	17		21		26		6.0	
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time		41	125		155		190	ns	2.0	Fig.7
	nOE to nY		15	25		31		38		4.5	
			12	21		26		32		6.0	
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time		41	125		155		190	ns	2.0	Fig.7
	nOE to nY		15	25		31		38		4.5	
			12	21		26		32		6.0	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14	60		75		90	ns	2.0	Fig.6
			5	12		15		18		4.5	
			4	10		13		15		6.0	

## 74HC/HCT125

### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver  $I_{CC}$  category: MSI

#### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, n <mark>OE</mark>	1.00

### **AC CHARACTERISTICS FOR 74HCT**

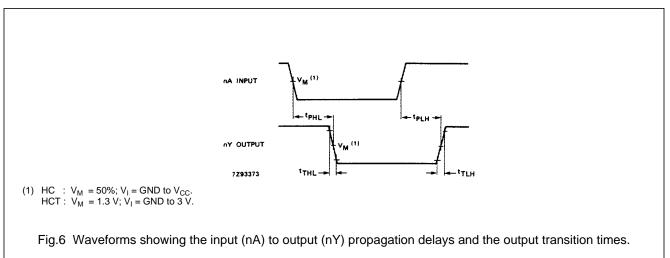
GND = 0 V;  $t_r = t_f = 6 ns$ ;  $C_L = 50 pF$ 

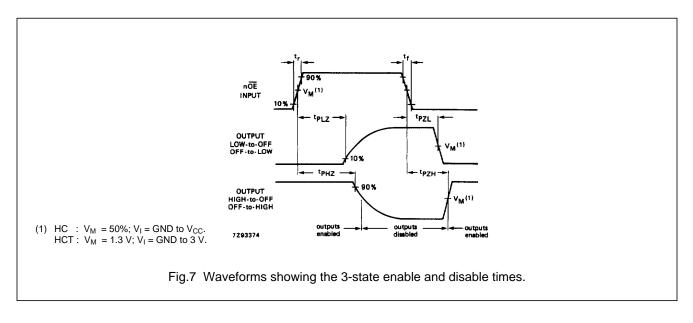
	PARAMETER	T <sub>amb</sub> (°C)								TEST CONDITIONS	
SYMBOL		74HCT									WAVEFORMS
STIVIBUL		+25			–40 to +85		-40 to +125		UNIT	V <sub>CC</sub> (V)	WAVEFORWIS
		min.	typ.	yp. max.	min.	max.	min.	max.		(-)	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY		15	25		31		38	ns	4.5	Fig.6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time nOE to nY		15	28		35		42	ns	4.5	Fig.7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time nOE to nY		15	25		31		38	ns	4.5	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.6

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## 74HC/HCT125

### AC WAVEFORMS





### PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

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