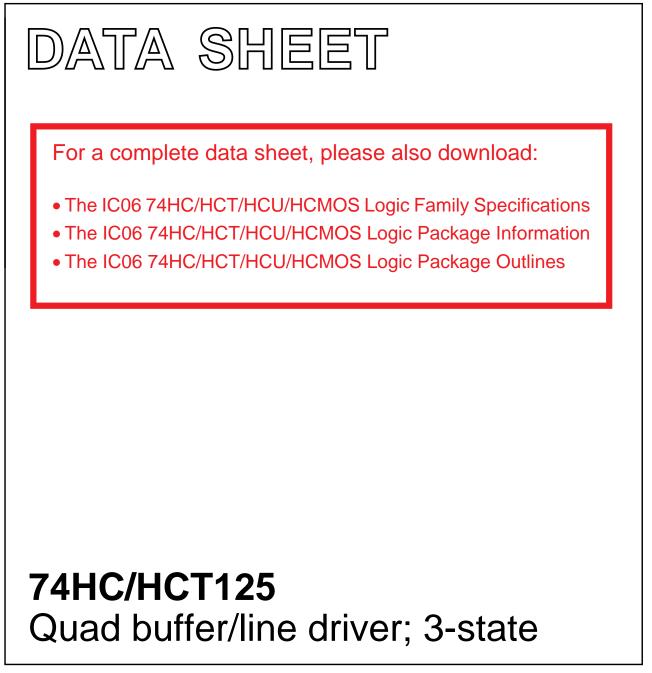
INTEGRATED CIRCUITS



Product specification File under Integrated Circuits, IC06 December 1990



Semiconductors

Philips

74HC/HCT125

FEATURES

- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT125 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT125 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (\overline{nOE}). A HIGH at \overline{nOE} causes the outputs to assume a HIGH impedance OFF-state.

The "125" is identical to the "126" but has active LOW enable inputs.

QUICK REFERENCE DATA

$GND = 0 V; T_{amb}$	= 25 °C;	$t_r = t_f = 6 \text{ ns}$
----------------------	----------	----------------------------

SYMBOL	PARAMETER	CONDITIONS	ТҮР			
STWBOL	FARAMETER	CONDITIONS	НС	нст		
t _{PHL} / t _{PLH}	propagation delay nA to nY	$C_{L} = 15 \text{ pF}; V_{CC} = 5 \text{ V}$	9	12	ns	
CI	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	22	24	pF	

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz

 $f_o = output frequency in MHz$

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} – 1.5 V

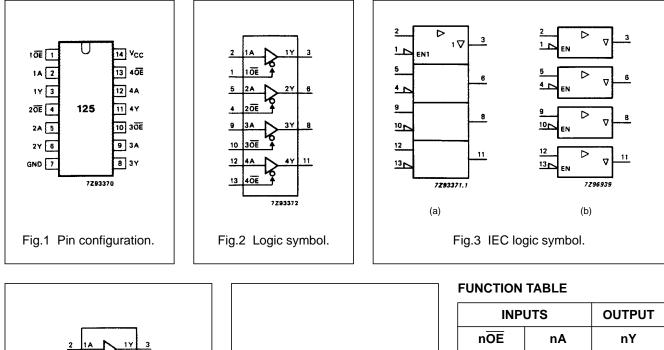
ORDERING INFORMATION

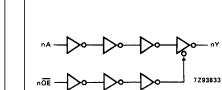
See "74HC/HCT/HCU/HCMOS Logic Package Information".

74HC/HCT125

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	
1, 4, 10, 13	$1\overline{OE}$ to $4\overline{OE}$	outputs enable inputs (active LOW)	
2, 5, 9, 12	1A to 4A	data inputs	
3, 6, 8, 11	1Y to 4Y	data outputs	
7	GND	ground (0 V)	
14	V _{CC}	positive supply voltage	



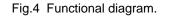


INP	OUTPUT	
nOE	nA	nY
L	L	L
L	н	Н
Н	Х	Z

Note

H = HIGH voltage level
L = LOW voltage level
X = don't care

Z = high impedance OFF-state



7293372

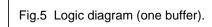
5

9

10

12

13



Downloaded from Elcodis.com electronic components distributor

74HC/HCT125

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	PARAMETER	T _{amb} (°C)								TEST CONDITIONS	
SYMBOL		74HC									WAVEFORMS
		+25			-40 to +85 -40 t		-40 to +125		V _{CC} (V)	WAVEFORINS	
		min.	typ.	max.	min.	max.	min.	max.		(•)	
t _{PHL} / t _{PLH}	propagation delay		30	100		125		150	ns	2.0	Fig.6
	nA to nY		11	20		25		30		4.5	
			9	17		21		26		6.0	
t _{PZH} / t _{PZL}	3-state output enable time		41	125		155		190	ns	2.0	Fig.7
	nOE to nY		15	25		31		38		4.5	
			12	21		26		32		6.0	
t _{PHZ} / t _{PLZ}	3-state output disable time		41	125		155		190	ns	2.0	Fig.7
	nOE to nY		15	25		31		38		4.5	
			12	21		26		32		6.0	
t _{THL} / t _{TLH}	output transition time		14	60		75		90	ns	2.0	Fig.6
			5	12		15		18		4.5	
			4	10		13		15		6.0	

74HC/HCT125

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, n <mark>OE</mark>	1.00

AC CHARACTERISTICS FOR 74HCT

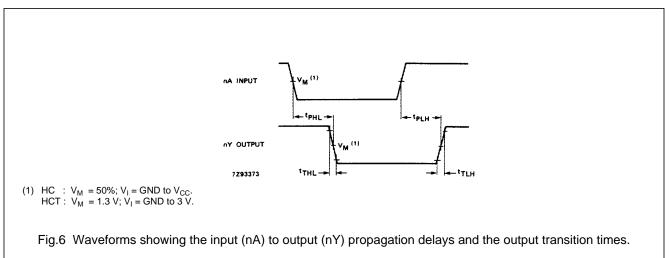
GND = 0 V; $t_r = t_f = 6 ns$; $C_L = 50 pF$

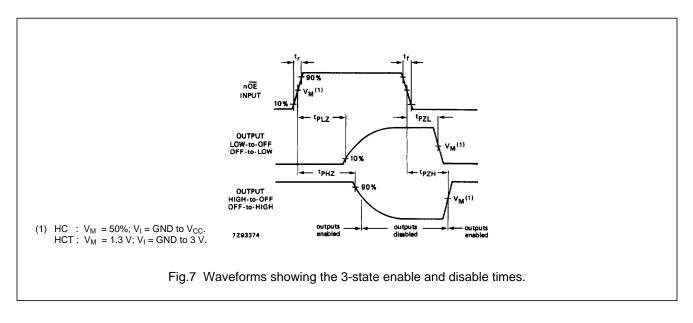
	PARAMETER	T _{amb} (°C)								TEST CONDITIONS	
SYMBOL		74HCT									WAVEFORMS
STIVIBUL		+25			–40 to +85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORWIS
		min.	typ.	yp. max.	min.	max.	min.	max.		(-)	
t _{PHL} / t _{PLH}	propagation delay nA to nY		15	25		31		38	ns	4.5	Fig.6
t _{PZH} / t _{PZL}	3-state output enable time nOE to nY		15	28		35		42	ns	4.5	Fig.7
t _{PHZ} / t _{PLZ}	3-state output disable time nOE to nY		15	25		31		38	ns	4.5	Fig.7
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6

Downloaded from Elcodis.com electronic components distributor

74HC/HCT125

AC WAVEFORMS





PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

December 1990