**FAIRCHILD**

SEMICONDUCTOR ™

# MM74HC14
# Hex Inverting Schmitt Trigger

## General Description

The MM74HC14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 74HC logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to $V_{CC}$ and ground.
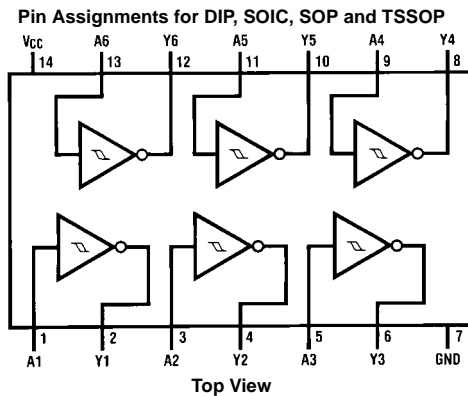
## Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
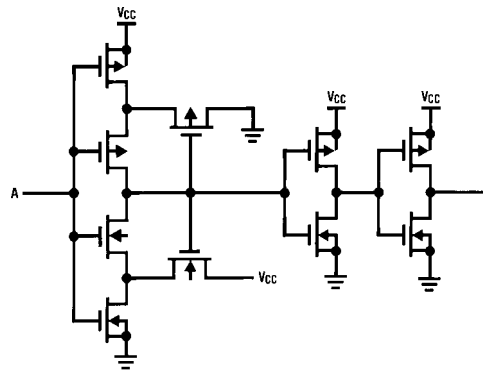- Typical hysteresis voltage: 0.9V at $V_{CC} = 4.5V$

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| MM74HC14M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow |
| MM74HC14SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HC14MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HC14N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram

**Pin Assignments for DIP, SOIC, SOP and TSSOP**



**Top View**

## Logic Diagram



DS005105.prf   www.fairchildsemi.com

**MM74HC14**

## Absolute Maximum Ratings (Note 1)

(Note 2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5 to +7.0V |
| DC Input Voltage ($V_{IN}$) | −1.5 to $V_{CC}$ +1.5V |
| DC Output Voltage ($V_{OUT}$) | −0.5 to $V_{CC}$ +0.5V |
| Clamp Diode Current ($I_{IK}$, $I_{OK}$) | ±20 mA |
| DC Output Current, per pin ($I_{OUT}$) | ±25 mA |
| DC $V_{CC}$ or GND Current, per pin ($I_{CC}$) | ±50 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temperature ($T_L$) | |
| (Soldering 10 seconds) | 260°C |

## Recommended Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 2 | 6 | V |
| DC Input or Output Voltage ($V_{IN}$, $V_{OUT}$) | 0 | $V_{CC}$ | V |
| Operating Temperature Range ($T_A$) | −40 | +85 | °C |

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: − 12 mW/°C from 65°C to 85°C.

## DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A = 25°C$ Typ | $T_A = 25°C$ Guaranteed Limits | $T_A = -40$ to $85°C$ Guaranteed Limits | $T_A = -55$ to $125°C$ Guaranteed Limits | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{T+}$ | Positive Going Threshold Voltage | Minimum | 2.0V | 1.2 | 1.0 | 1.0 | 1.0 | V |
| | | | 4.5V | 2.7 | 2.0 | 2.0 | 2.0 | V |
| | | | 6.0V | 3.2 | 3.0 | 3.0 | 3.0 | V |
| | | Maximum | 2.0V | 1.2 | 1.5 | 1.5 | 1.5 | V |
| | | | 4.5V | 2.7 | 3.15 | 3.15 | 3.15 | V |
| | | | 6.0V | 3.2 | 4.2 | 4.2 | 4.2 | V |
| $V_{T-}$ | Negative Going Threshold Voltage | Minimum | 2.0V | 0.7 | 0.3 | 0.3 | 0.3 | V |
| | | | 4.5V | 1.8 | 0.9 | 0.9 | 0.9 | V |
| | | | 6.0V | 2.2 | 1.2 | 1.2 | 1.2 | V |
| | | Maximum | 2.0V | 0.7 | 1.0 | 1.0 | 1.0 | V |
| | | | 4.5V | 1.8 | 2.2 | 2.2 | 2.2 | V |
| | | | 6.0V | 2.2 | 3.0 | 3.0 | 3.0 | V |
| $V_H$ | Hysteresis Voltage | Minimum | 2.0V | 0.5 | 0.2 | 0.2 | 0.2 | V |
| | | | 4.5V | 0.9 | 0.4 | 0.4 | 0.4 | V |
| | | | 6.0V | 1.0 | 0.5 | 0.5 | 0.5 | V |
| | | Maximum | 2.0V | 0.5 | 1.0 | 1.0 | 1.0 | V |
| | | | 4.5V | 0.9 | 1.4 | 1.4 | 1.4 | V |
| | | | 6.0V | 1.0 | 1.5 | 1.5 | 1.5 | V |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | $V_{IN} = V_{IL}$ $|I_{OUT}| = 20$ µA | 2.0V | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | 4.4 | V |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | 5.9 | V |
| | | $V_{IN} = V_{IL}$ $|I_{OUT}| = 4.0$ mA | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | V |
| | | $|I_{OUT}| = 5.2$ mA | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | V |
| $V_{OL}$ | Maximum LOW Level Output Voltage | $V_{IN} = V_{IH}$ $|I_{OUT}| = 20$ µA | 2.0V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | | 6.0V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | $V_{IN} = V_{IH}$ $|I_{OUT}| = 4.0$ mA | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | $|I_{OUT}| = 5.2$ mA | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| $I_{IN}$ | Maximum Input Current | $V_{IN} = V_{CC}$ or GND | 6.0V | | ±0.1 | ±1.0 | ±1.0 | µA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$ µA | 6.0V | | 2.0 | 20 | 40 | µA |

**Note 4:** For a power supply of 5V ±10% the worst case output voltages ($V_{OH}$, and $V_{OL}$) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5V and 4.5V respectively. (The $V_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0V values should be used.

## AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

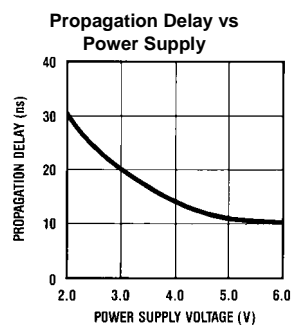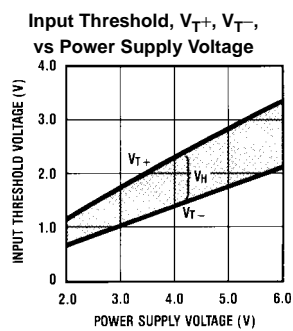| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay | | 12 | 22 | ns |

## AC Electrical Characteristics

$V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

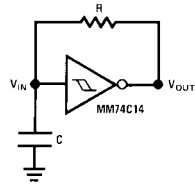| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A = 25°C$ Typ | $T_A = 25°C$ | $T_A = -40$ to $85°C$ | $T_A = -55$ to $125°C$ | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | Guaranteed Limits | | | |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation | | 2.0V | 60 | 125 | 156 | 188 | ns |
| | Delay | | 4.5V | 13 | 25 | 31 | 38 | ns |
| | | | 6.0V | 11 | 21 | 26 | 32 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Rise | | 2.0V | 30 | 75 | 95 | 110 | ns |
| | and Fall Time | | 4.5V | 8 | 15 | 19 | 22 | ns |
| | | | 6.0V | 7 | 13 | 16 | 19 | ns |
| $C_{PD}$ | Power Dissipation Capacitance (Note 5) | (per gate) | | 27 | | | | pF |
| $C_{IN}$ | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | pF |

**Note 5:** $C_{PD}$ determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.
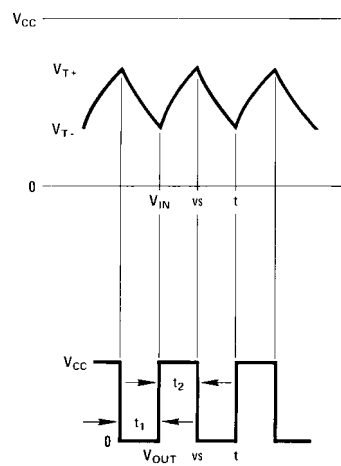
## Typical Performance Characteristics

**Input Threshold, $V_T+$, $V_T-$, vs Power Supply Voltage**



**Propagation Delay vs Power Supply**

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# Typical Applications

**Low Power Oscillator**

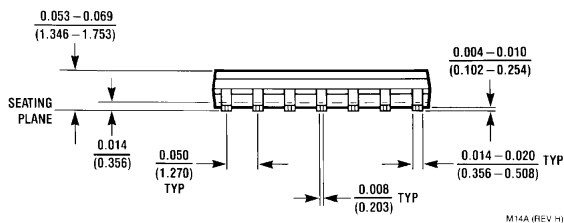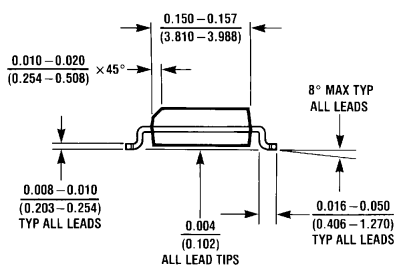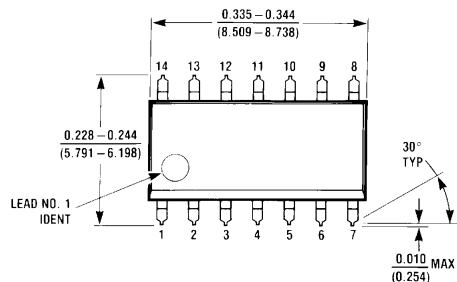$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

$$t_2 \approx RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$

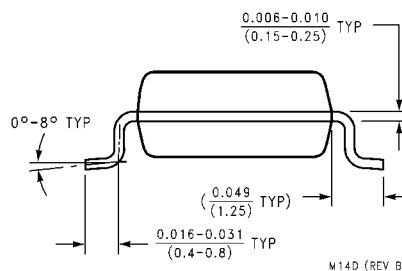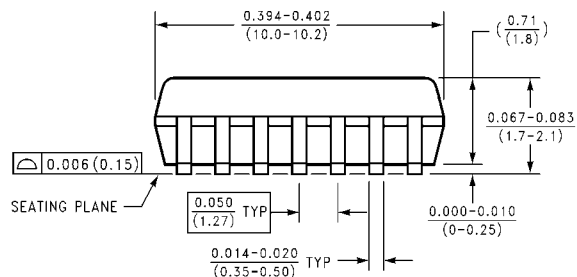$$f \approx \frac{1}{RC \ln \dfrac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}}$$
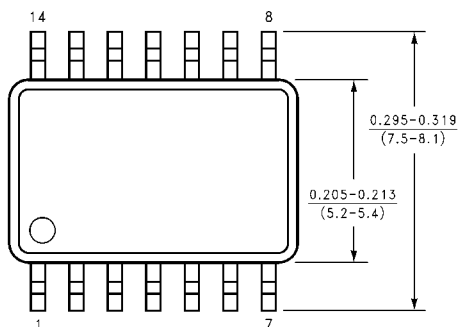
**Note:** The equations assume $t_1 + t_2 \gg t_{pd0} + t_{pd1}$

# Physical Dimensions inches (millimeters) unless otherwise noted

0.335 − 0.344
(8.509 − 8.738)

14 13 12 11 10 9 8

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO. 1
IDENT

1 2 3 4 5 6 7

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020
(0.356 − 0.508) TYP

M14A (REV H)

**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow**
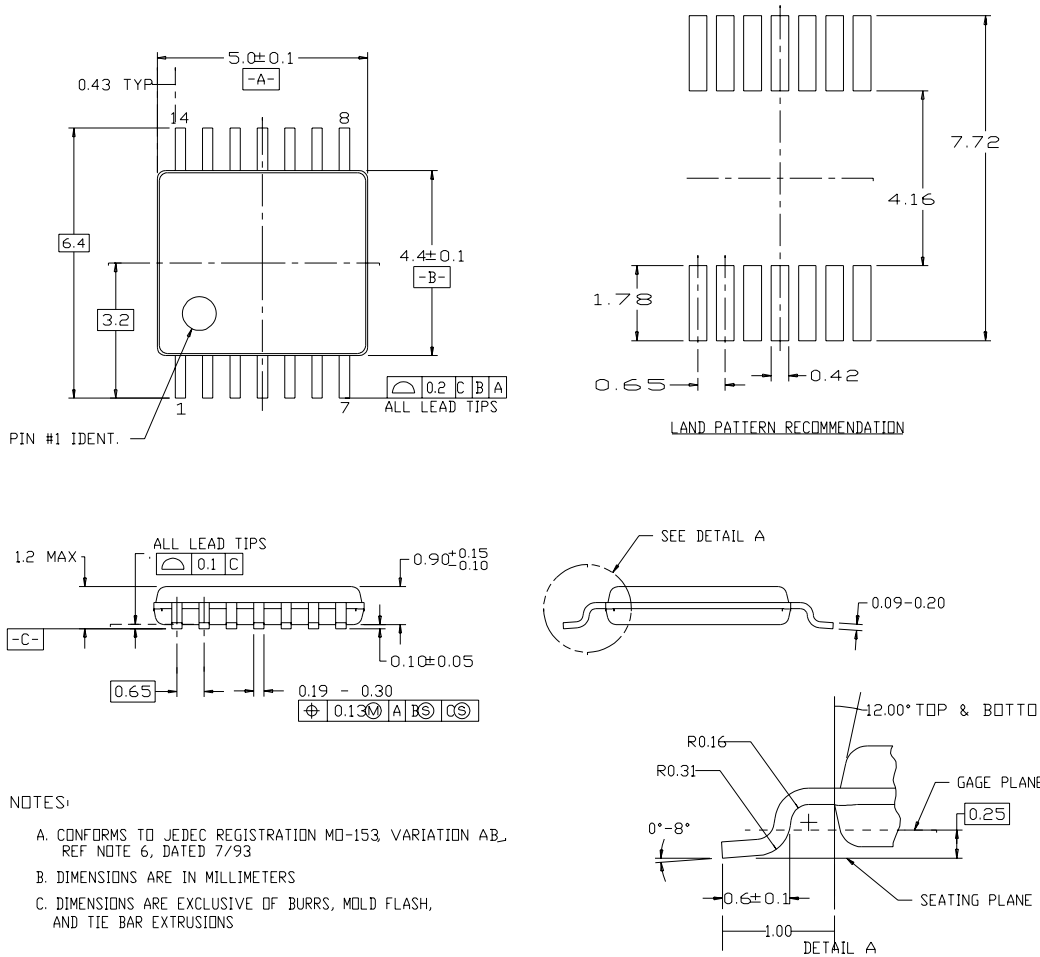**Package Number M14A**

14 8

0.295−0.319
(7.5−8.1)

0.205−0.213
(5.2−5.4)

1 7

0.394−0.402
(10.0−10.2)

( 0.71 )
( 1.8 )

0.067−0.083
(1.7−2.1)

0.006−0.010
(0.15−0.25) TYP

0.006 (0.15)

SEATING PLANE

0°−8° TYP

0.050 TYP
(1.27)

0.014−0.020
(0.35−0.50) TYP

0.000−0.010
(0−0.25)

( 0.049 TYP)
( 1.25 )

0.016−0.031
(0.4−0.8) TYP

M14D (REV B)

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M14D**

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# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

14LD, TSSOP, JEDEC MO-153, 4.4MM WIDE

5.0±0.1
-A-

0.43 TYP

14          8

6.4

3.2

4.4±0.1
-B-

0.2 C B A
ALL LEAD TIPS

1          7

PIN #1 IDENT.

7.72

4.16

1.78

0.65          0.42

LAND PATTERN RECOMMENDATION

ALL LEAD TIPS
0.1 C

1.2 MAX

-C-

0.90 +0.15 -0.10

0.10±0.05

0.65

0.19 - 0.30

⊕ 0.13Ⓜ A BⓈ CⓈ

SEE DETAIL A

0.09-0.20

12.00° TOP & BOTTO

R0.16

R0.31

0°-8°

0.6±0.1

1.00

DETAIL A

GAGE PLANE

0.25

SEATING PLANE

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
   REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,
   AND TIE BAR EXTRUSIONS

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC14**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)
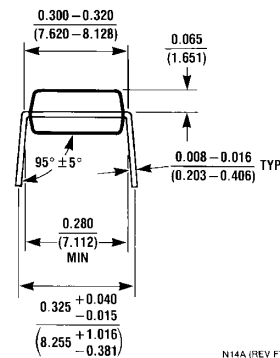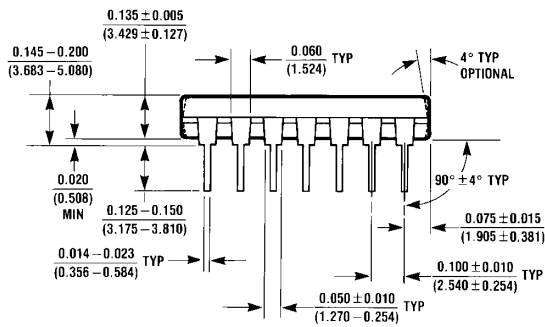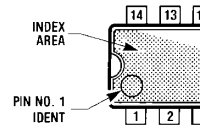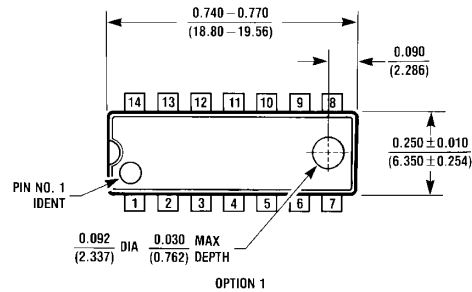


14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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