

MM74HC123A Dual Retriggerable Monostable Multivibrator

General Description

The MM74HC123A high speed monostable multivibrators (one shots) utilize advanced silicon-gate CMOS technology. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The MM74HC123A can be triggered on the positive transition of the clear while A is held LOW and B is held HIGH.

The MM74HC123A is retriggerable. That is it may be triggered repeatedly while their outputs are generating a pulse and the pulse will be extended.

Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The out-

put pulse equation is simply: $PW = (R_{EXT}) (C_{EXT})$; where PW is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 25 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μ A maximum (74HC Series)
- Low input current: 1 μ A maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula $T = RC$
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: $\pm 5\%$ (typ)
- Schmitt Trigger A & B inputs enable infinite signal input rise and fall times.

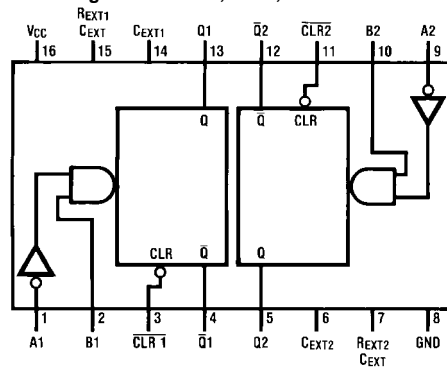
Ordering Code:

| Order Number | Package Number | Package Description |
|---------------|----------------|--|
| MM74HC123AM | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HC123ASJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HC123AMTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HC123AN | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

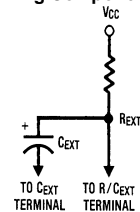
Connection Diagram

Pin Assignment for DIP, SOIC, SOP and TSSOP



Top View

Timing Component



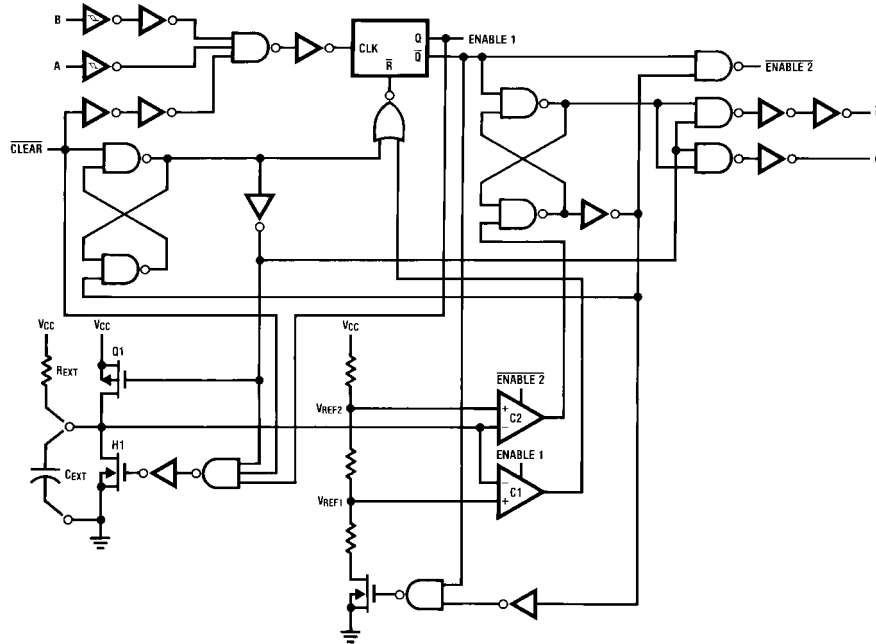
Note: Pin 6 and Pin 14 must be hard-wired to GND.

Truth Table

| Inputs | | | Outputs | |
|--------|---|---|----------------------|---------------------|
| Clear | A | B | Q | \bar{Q} |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | One HIGH Level Pulse | One LOW Level Pulse |
| H | ↓ | H | One HIGH Level Pulse | One LOW Level Pulse |
| ↑ | L | H | One HIGH Level Pulse | One LOW Level Pulse |

H = HIGH Level
 L = LOW Level
 ↑ = Transition from LOW-to-HIGH
 ↓ = Transition from HIGH-to-LOW
 ┌── = One HIGH Level Pulse
 └── = One LOW Level Pulse
 X = Irrelevant

Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

| | |
|--|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Voltage (V_{IN}) | -1.5V to $V_{CC} + 1.5V$ |
| DC Output Voltage (V_{OUT}) | -0.5V to $V_{CC} + 0.5V$ |
| Clamp Diode Current (I_{IK}, I_{OK}) | ± 20 mA |
| DC Output Current, per pin (I_{OUT}) | ± 25 mA |
| DC V_{CC} or GND Current, per pin (I_{CC}) | ± 50 mA |
| Storage Temperature Range (T_{STG}) | -65°C to +150°C |
| Power Dissipation (P_D) | |
| (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temperature (T_L) | |
| (Soldering 10 seconds) | 260°C |

Recommended Operating Conditions

| | Min | Max | Units |
|--|-----|----------|-------|
| Supply Voltage (V_{CC}) | 2 | 6 | V |
| DC Input or Output Voltage (V_{IN}, V_{OUT}) | 0 | V_{CC} | V |
| Operating Temperature Range (T_A) | -40 | +85 | °C |
| Input Rise or Fall Times (Clear Input) | | | |
| (t_r, t_f) $V_{CC} = 2.0V$ | | 1000 | ns |
| $V_{CC} = 4.5V$ | | 500 | ns |
| $V_{CC} = 6.0V$ | | 400 | ns |

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature Derating: Plastic "N" Package: -12mW/°C from 65°C to 85°C

DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | V_{CC} | $T_A = 25^\circ C$ | | | $T_A = -40$ to $85^\circ C$ | $T_A = -55$ to $125^\circ C$ | Units |
|----------|--|---|----------|--------------------|-------------------|-----------|-----------------------------|------------------------------|-------|
| | | | | Typ | Guaranteed Limits | | | | |
| V_{IH} | Minimum HIGH Level Input Voltage | | 2.0V | | 1.5 | 1.5 | 1.5 | V | |
| | | | 4.5V | | 3.15 | 3.15 | 3.15 | V | |
| | | | 6.0V | | 4.2 | 4.2 | 4.2 | V | |
| V_{IL} | Maximum LOW Level Input Voltage | | 2.0V | | 0.3 | 0.3 | 0.3 | V | |
| | | | 4.5V | | 0.9 | 0.9 | 0.9 | V | |
| | | | 6.0V | | 1.2 | 1.2 | 1.2 | V | |
| V_{OH} | Minimum HIGH Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$ | 2.0V | 2.0 | 1.9 | 1.9 | 1.9 | V | |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | 4.4 | V | |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | 5.9 | V | |
| | | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | V | |
| | | | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | V | |
| | | | | | | | | V | |
| V_{OL} | Maximum LOW Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$ | 2.0V | 0 | 0.1 | 0.1 | 0.1 | V | |
| | | | 4.5V | 0 | 0.1 | 0.1 | 0.1 | V | |
| | | | 6.0V | 0 | 0.1 | 0.1 | 0.1 | V | |
| | | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4$ mA $ I_{OUT} \leq 5.2$ mA | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | V | |
| | | | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 | V | |
| | | | | | | | | V | |
| I_{IN} | Maximum Input Current (Pins 7, 15) | $V_{IN} = V_{CC}$ or GND | 6.0V | | ± 0.5 | ± 5.0 | ± 5.0 | μA | |
| I_{IN} | Maximum Input Current (all other pins) | $V_{IN} = V_{CC}$ or GND | 6.0V | | ± 0.1 | ± 1.0 | ± 1.0 | μA | |
| I_{CC} | Maximum Quiescent Supply Current (standby) | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$ | 6.0V | | 8.0 | 80 | 160 | μA | |
| I_{CC} | Maximum Active Supply Current (per monostable) | $V_{IN} = V_{CC}$ or GND $R/C_{EXT} = 0.5V_{CC}$ | 2.0V | 36 | 80 | 110 | 130 | μA | |
| | | | 4.5V | 0.33 | 1.0 | 1.3 | 1.6 | mA | |
| | | | 6.0V | 0.7 | 2.0 | 2.6 | 3.2 | mA | |

Note 4: For a power supply of $5V \pm 10\%$ the worst-case output voltages (V_{OH}, V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15\text{ pF}$, $t_r = t_f = 6\text{ ns}$

| Symbol | Parameter | Conditions | Typ | Limit | Units |
|---------------|---|---|-----|-------|---------|
| t_{PLH} | Maximum Trigger Propagation Delay A, B or Clear to Q | | 22 | 33 | ns |
| t_{PHL} | Maximum Trigger Propagation Delay A, B or Clear to \bar{Q} | | 25 | 42 | ns |
| t_{PHL} | Maximum Propagation Delay, Clear to Q | | 20 | 27 | ns |
| t_{PLH} | Maximum Propagation Delay, Clear to \bar{Q} | | 22 | 33 | ns |
| t_W | Minimum Pulse Width, A, B or Clear | | 14 | 26 | ns |
| t_{REM} | Minimum Clear Removal Time | | | 0 | ns |
| $t_{WQ(MIN)}$ | Minimum Output Pulse Width | $C_{EXT} = 28\text{ pF}$ $R_{EXT} = 2\text{ k}\Omega$ | 400 | | ns |
| t_{WQ} | Output Pulse Width | $C_{EXT} = 1000\text{ pF}$ $R_{EXT} = 10\text{ k}\Omega$ | 10 | | μs |

AC Electrical Characteristics

$C_L = 50\text{ pF}$, $t_r = t_f = 6\text{ ns}$ (unless otherwise specified)

| Symbol | Parameter | Conditions | V_{CC} | $T_A = 25^\circ C$ | | $T_A = -40\text{ to }85^\circ C$ | $T_A = -55\text{ to }125^\circ C$ | Units | |
|--------------------|--|--|------------|--------------------|-------------------|----------------------------------|-----------------------------------|---------|----|
| | | | | Typ | Guaranteed Limits | | | | |
| t_{PLH} | Maximum Trigger Propagation Delay, A, B or Clear to Q | | 2.0V | 77 | 169 | 194 | 210 | ns | |
| | | | 4.5V | 26 | 42 | 51 | 57 | ns | |
| | | | 6.0V | 21 | 32 | 39 | 44 | ns | |
| t_{PHL} | Maximum Trigger Propagation Delay, A, B or Clear to \bar{Q} | | 2.0V | 88 | 197 | 229 | 250 | ns | |
| | | | 4.5V | 29 | 48 | 60 | 67 | ns | |
| | | | 6.0V | 24 | 38 | 46 | 51 | ns | |
| t_{PHL} | Maximum Propagation Delay Clear to Q | | 2.0V | 54 | 114 | 132 | 143 | ns | |
| | | | 4.5V | 23 | 34 | 41 | 45 | ns | |
| | | | 6.0V | 19 | 28 | 33 | 36 | ns | |
| t_{PLH} | Maximum Propagation Delay Clear to \bar{Q} | | 2.0V | 56 | 116 | 135 | 147 | ns | |
| | | | 4.5V | 25 | 36 | 42 | 46 | ns | |
| | | | 6.0V | 20 | 29 | 34 | 37 | ns | |
| t_W | Minimum Pulse Width A, B, Clear | | 2.0V | 57 | 123 | 144 | 157 | ns | |
| | | | 4.5V | 17 | 30 | 37 | 42 | ns | |
| | | | 6.0V | 12 | 21 | 27 | 30 | ns | |
| t_{REM} | Minimum Clear Removal Time | | 2.0V | | 0 | 0 | 0 | ns | |
| | | | 4.5V | | 0 | 0 | 0 | ns | |
| | | | 6.0V | | 0 | 0 | 0 | ns | |
| t_{TLH}, t_{THL} | Maximum Output Rise and Fall Time | | 2.0V | 30 | 75 | 95 | 110 | ns | |
| | | | 4.5V | 8 | 15 | 19 | 22 | ns | |
| | | | 6.0V | 7 | 13 | 16 | 19 | ns | |
| $t_{WQ(MIN)}$ | Minimum Output Pulse Width | $C_{EXT} = 28\text{ pF}$ $R_{EXT} = 2\text{ k}\Omega$ $R_{EXT} = 6\text{ k}\Omega$ ($V_{CC} = 2V$) | 2.0V | 1.5 | | | | μs | |
| | | | 4.5V | 450 | | | | ns | |
| | | | 6.0V | 380 | | | | ns | |
| t_{WQ} | Output Pulse Width | $C_{EXT} = 0.1\text{ }\mu F$ $R_{EXT} = 10\text{ k}\Omega$ | Min | 5.0V | 1 | 0.9 | 0.86 | 0.85 | ms |
| | | | Max | 5.0V | 1 | 1.1 | 1.14 | 1.15 | ms |
| C_{IN} | Maximum Input Capacitance (Pins 7 & 15) | | | 12 | 20 | 20 | 20 | pF | |
| C_{IN} | Maximum Input Capacitance (other inputs) | | | 6 | 10 | 10 | 10 | pF | |
| C_{PD} | Power Dissipation Capacitance | (Note 5) | | 70 | | | | pF | |

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Theory of Operation

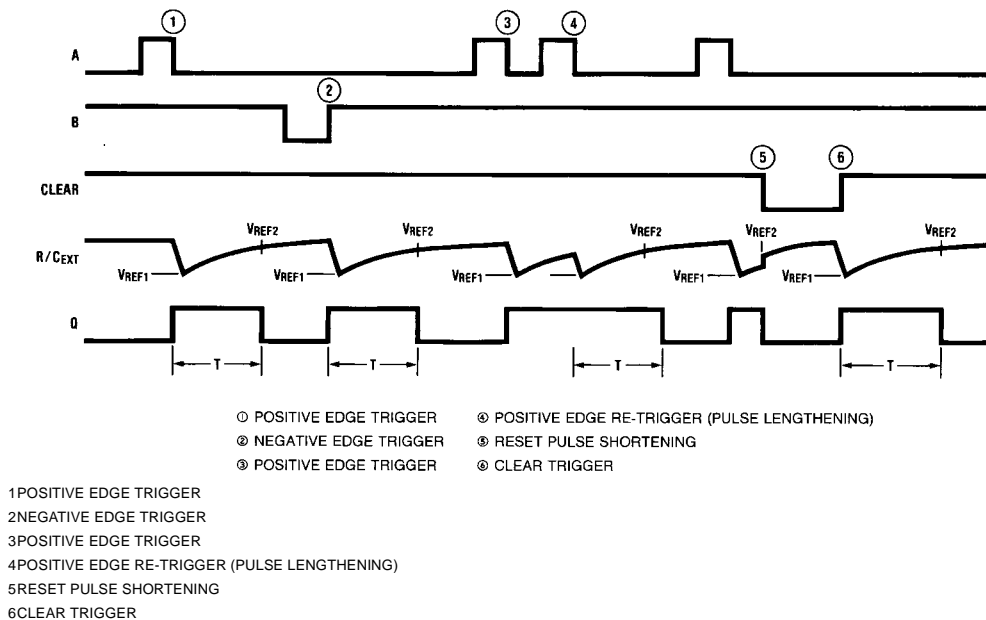


FIGURE 1.

TRIGGER OPERATION

As shown in *Figure 1* and the logic diagram, before an input trigger occurs, the one shot is in the quiescent state with the Q output LOW, and the timing capacitor C_{EXT} completely charged to V_{CC} . When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and Nchannel transistor N11. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT} , toward V_{CC} . When the voltage across C_{EXT} equals V_{REF2} , comparator C2 changes state causing the output latch to reset (Q goes LOW) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC}). The MM74HC123A can also be triggered when clear goes from GND to V_{CC} (while A is at GND and B is at V_{CC}).

It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the MM74HC123A is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of

the value of C_{EXT} , R_{EXT} , or the duty cycle of the input waveform.

RETRIGGER OPERATION

The MM74HC123A is retriggered if a valid trigger occurs 3 followed by another trigger 4 before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at the R/C_{EXT} pin has begun to rise from V_{REF1} , but has not yet reached V_{REF2} , will cause an increase in output pulse width T. When a valid retrigger is initiated 4, the voltage at the R/C_{EXT} pin will again drop to V_{REF1} before progressing along the RC charging curve toward V_{CC} . The Q output will remain HIGH until time T, after the last valid retrigger.

Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit, the minimum retrigger time, t_{rr} is a function of internal propagation delays and the discharge time of C_X :

$$t_{rr} \approx 20 + \frac{187}{V_{CC} - 0.7} + \frac{565 + (0.256 V_{CC}) C_X}{[V_{CC} - 0.7]^2}$$

Another removal/retrigger time occurs when a short clear pulse is used. Upon receipt of a clear, the one shot must charge the capacitor up to the upper trip point before the one shot is ready to receive the next trigger. This time is dependent on the capacitor used and is approximately:

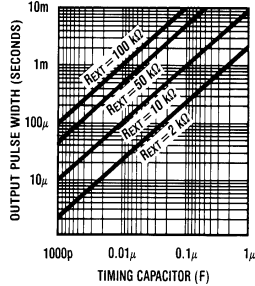
$$t_{rr} = 196 + \frac{640}{V_{CC} - 0.7} + \frac{522 + (0.3 V_{CC}) C_X}{(V_{CC} - 0.7)^2} \text{ ns}$$

RESET OPERATION

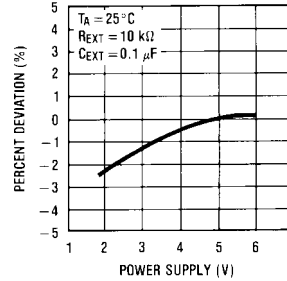
These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 5. When the voltage on the capacitor reaches V_{REF2} , the reset latch will clear and then be ready to accept another pulse. If the

clear input is held low, any trigger inputs that occur will be inhibited and the Q and \bar{Q} outputs of the output latch will not change. Since the Q output is reset when an input low-level is detected on the Clear input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

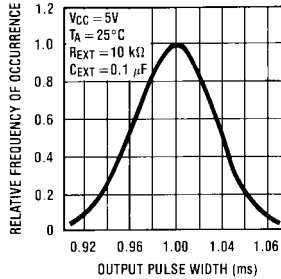
Typical Output Pulse Width vs. Timing Components



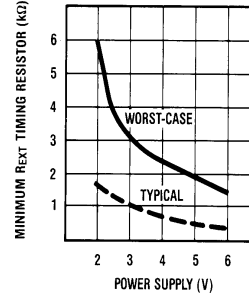
Typical 1ms Pulse Width Variation vs. Supply



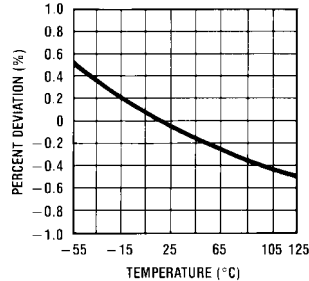
Typical Distribution of Output Pulse Width, Part to Part



Minimum REXT vs. Supply Voltage

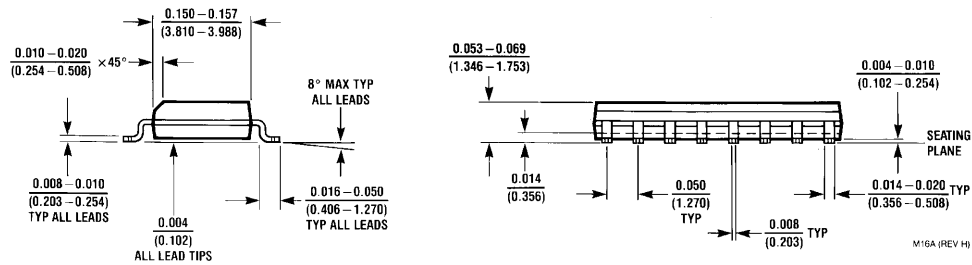
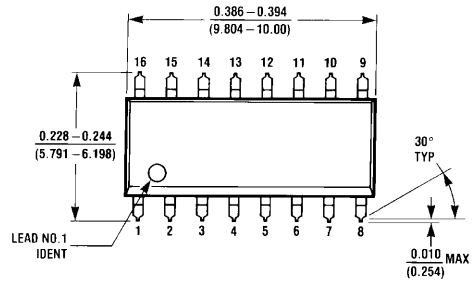


Typical 1ms Pulse Width Variation vs. Temperature

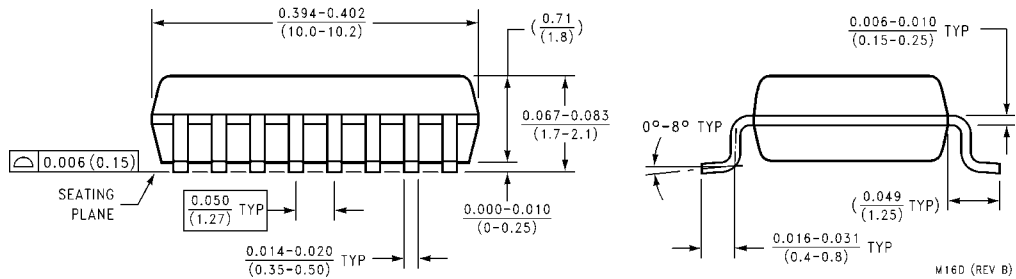
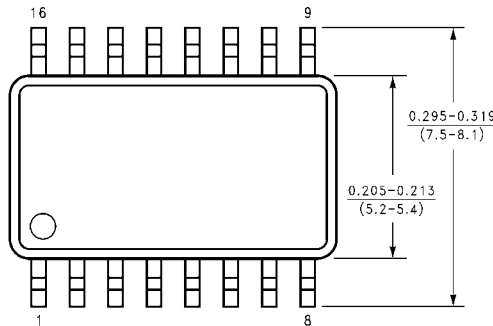


Note: R and C are not subjected to temperature. The C is polypropylene.

Physical Dimensions inches (millimeters) unless otherwise noted

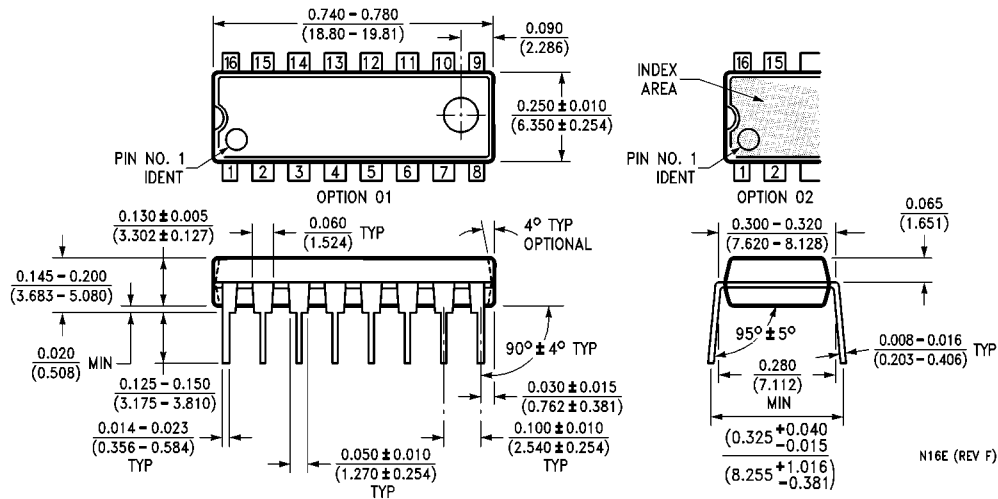


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.