Integrated Device Technology, Inc.

HIGH-SPEED 2K x 9 DUAL-PORT STATIC RAM WITH BUSY & INTERRUPT

IDT70121S/L
IDT70125S/L

FEATURES:

- High-speed access
  – Commercial: 25/35/45/55ns (max.)
- Low-power operation
  – IDT70121/70125S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  – IDT70121/70125L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asychronous operation from either port
- MASTER IDT70121 easily expands data bus width to 18 bits or more using SLAVE IDT70125 chip
- On-chip port arbitration logic (IDT70121 only)
- $\overline{BUSY}$ output flag on Master; $\overline{BUSY}$ input on Slave
- $\overline{INT}$ flag for port-to-port communication
- Battery backup operation—2V data retention
- TTL-compatible, signal 5V (±10%) power supply
- Available in 52-pin PLCC
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

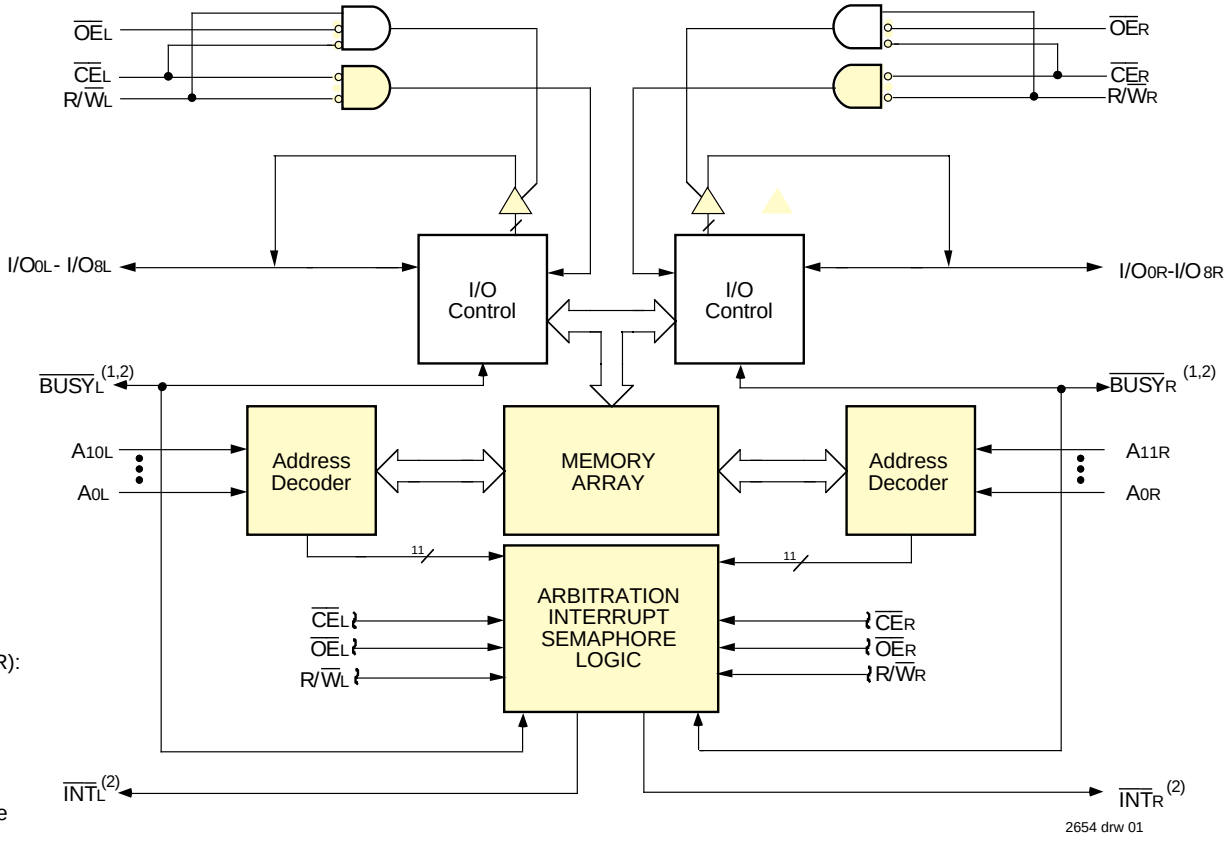
DESCRIPTION:

The IDT70121/IDT70125 are high-speed 2K x 9 Dual-Port Static RAMs. The IDT70121 is designed to be used as a stand-alone 9-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT70125 "SLAVE" Dual-Port in 18-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 18-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power-down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70121/IDT70125 utilizes a 9-bit wide data path to allow for Data/Control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. 70121 (MASTER): $\overline{BUSY}$ is non-tri-stated push-pull output.
   70125 (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{INT}$ is totem-pole output.

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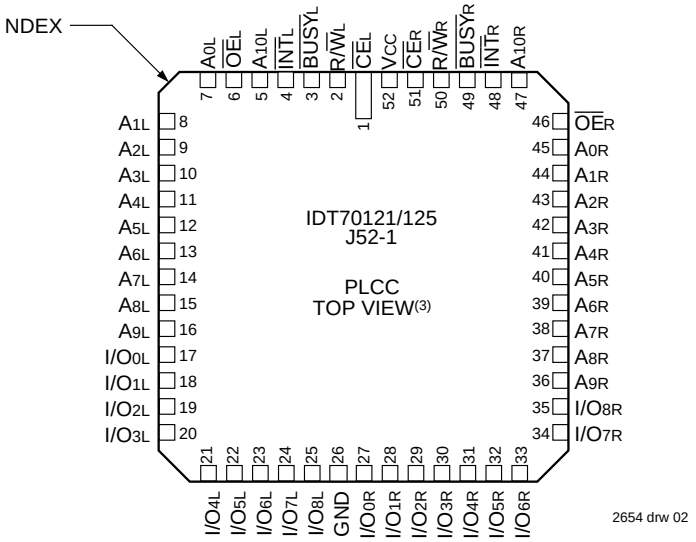
DESCRIPTION (Cont'd):

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 500mW of power. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 200µW from a 2V battery.

The IDT70121/IDT70125 devices are packaged in a 52-pin PLCC.

PIN CONFIGURATIONS (1,2)



NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. This text does not indicate the orientation of the actual part-marking.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2654 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq V_{CC}$ + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2654 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Voltage	2.2	–	6.0(2)	V
V_{IL}	Input Low Voltage	–0.5(1)	–	0.8	V

2654 tbl 03

NOTES:
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE(1) (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Condition(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

2654 tbl 13

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

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DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	70121S 70125S		70121L 70125L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current[5]	V_{CC} = 5.5V, $\overline{CE}$ = V_{IH} V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	2.4	—	V

NOTE:
1. At Vcc ≤ 2.0V leakages are undefined.

2654 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,4] (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version		70121X25 70125X25		70121X35 70125X35		70121X45 70125X45		70121X55 70125X55		Unit
					Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL},Outputs Open, f = f_{MAX}[2]	Com'l.	S	125	260	125	250	125	245	125	240	mA
				L	125	220	125	210	125	205	125	200	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_{"A"}$ and $\overline{CE}_{"B"}$ = V_{IH}, f = f_{MAX}[2]	Com'l.	S	30	65	30	65	30	65	30	65	mA
				L	30	45	30	45	30	45	30	45	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_{"A"}$=V_{IL} and $\overline{CE}_{"B"}$=V_{IH}[5] Active Port Outputs Open, f = f_{MAX}[2]	Com'l.	S	80	175	80	165	80	160	80	155	mA
				L	80	145	80	135	80	130	80	125	
I_{SB3}	Full Standby Current (Both Ports CMOS Level Inputs)	$\overline{CE}_{"A"}$ and $\overline{CE}_{"B"}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[3]	Com'l.	S	1.0	15	1.0	15	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port CMOS Level Inputs)	$\overline{CE}_{"A"}$≤0.2V and $\overline{CE}_{"B"}$≥VCC-0.2V[5] V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[2]	Com'l.	S	70	170	70	160	70	155	70	150	mA
				L	70	140	70	130	70	125	70	120	

NOTES:
1. "X" in part numbers indicates power rating (S or L).
2. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
3. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
4. Vcc=5V, T_A=+25°C for Typical values, and they are not production tested.
5. Port "A" may be either left or right port. Port "B" is opposite from port "A".

2654 tbl 05

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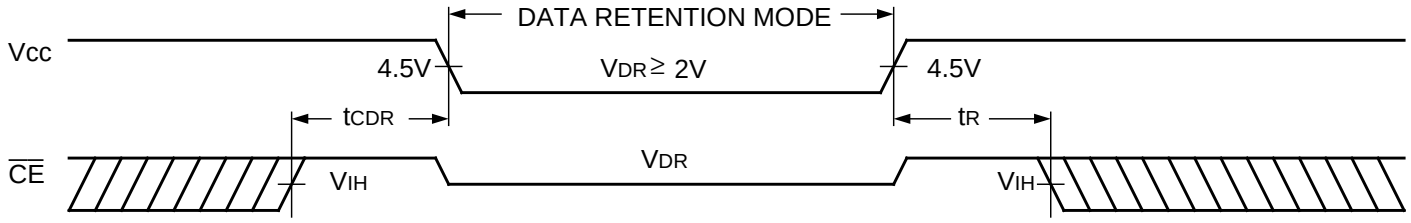
DATA RETENTION CHARACTERISTICS (L Version Only)

Symbol	Parameter	Test Condition		70121L/70125L Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		2	—	—	V
I_{CCDR}	Data Retention Current		Com'l.	—	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

NOTES: 2654 tbl 06
1. V_{CC} = 2V, T_A = +25°C, and are not production tested.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization but is not production tested.

DATA RETENTION WAVEFORM

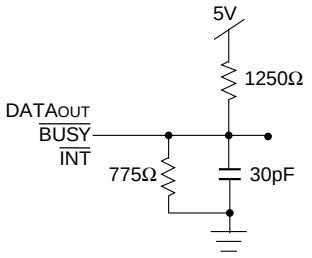


2654 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2654 tbl 07



2654 drw 04

Figure 1. AC Output Test Load

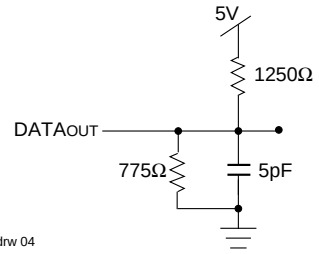


Figure 2. Output Test Load
(For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(3)

Symbol	Parameter	70121X25 70125X25 Min.	Max.	70121X35 70125X35 Min.	Max.	70121X45 70125X45 Min.	Max.	70121X55 70125X55 Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	25	—	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	25	—	35	—	45	—	55	ns
t_{ACE}	Chip Enable Access Time	—	25	—	35	—	45	—	55	ns
t_{AOE}	Output Enable Access Time	—	12	—	25	—	30	—	35	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time(1,2)	0	—	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	10	—	15	—	20	—	30	ns
t_{PU}	Chip Enable to Power-Up Time(2)	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power-Down Time(2)	—	50	—	50	—	50	—	50	ns

NOTES: 2654 tbl 08
1. Transition is measured ±500mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter guaranteed by device characterization, but is not production tested.
3. "X" in part numbers indicates power rating (S or L).

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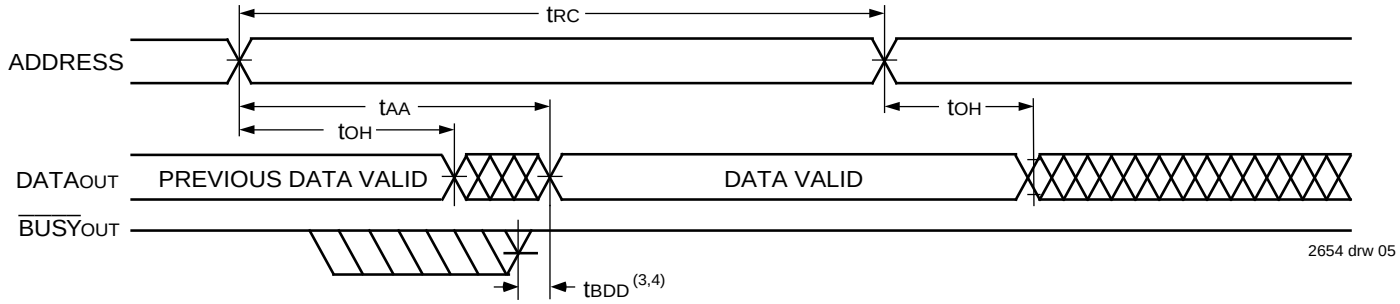
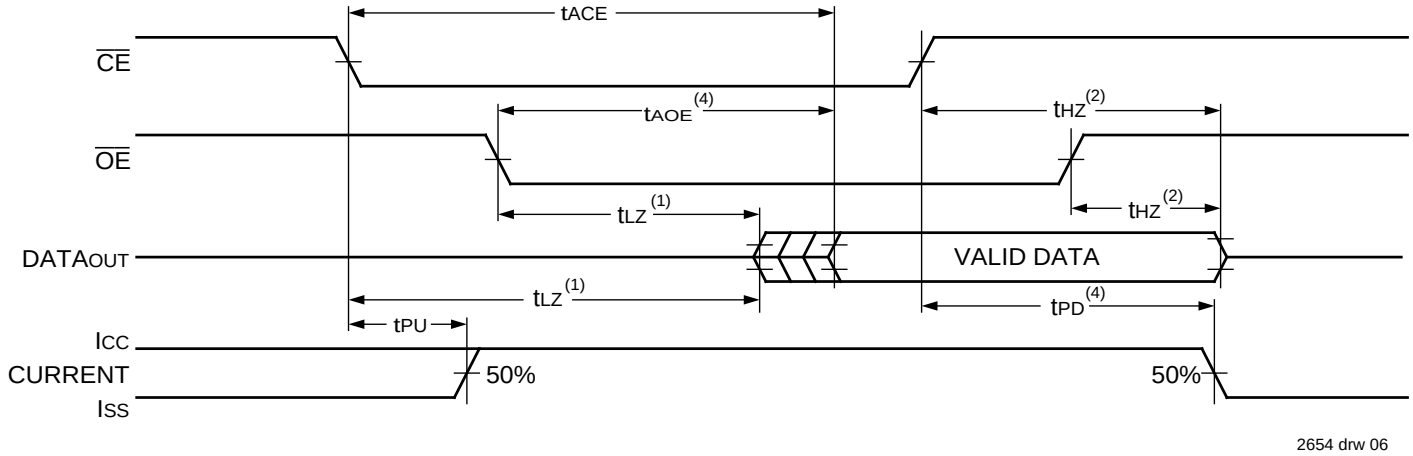
TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE(1,2,4)



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(5,6)



NOTES:
1. Timing depends on which signal is aserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is deaserted first, $\overline{OE}$ or $\overline{CE}$.
3. t_{BDD} delay is required only in a case where the opposite port is completing a write operation to the same address location. For simultanious read operations $\overline{BUSY}$ has no relationship to valid output data.
4. Start of valid data depends on which timing becomes effective last, t_{AOE}, t_{ACE}, t_{AA}, or t_{BDD}.
5. R/$\overline{W}$ = V_{IH}, and the address is valid prior to other coincidental with $\overline{CE}$ transition Low.
6. R/$\overline{W}$ = V_{IH}, $\overline{CE}$ = V_{IL}, and $\overline{OE}$ = V_{IL}. Address is valid prior to or coincident with $\overline{CE}$ transition Low.

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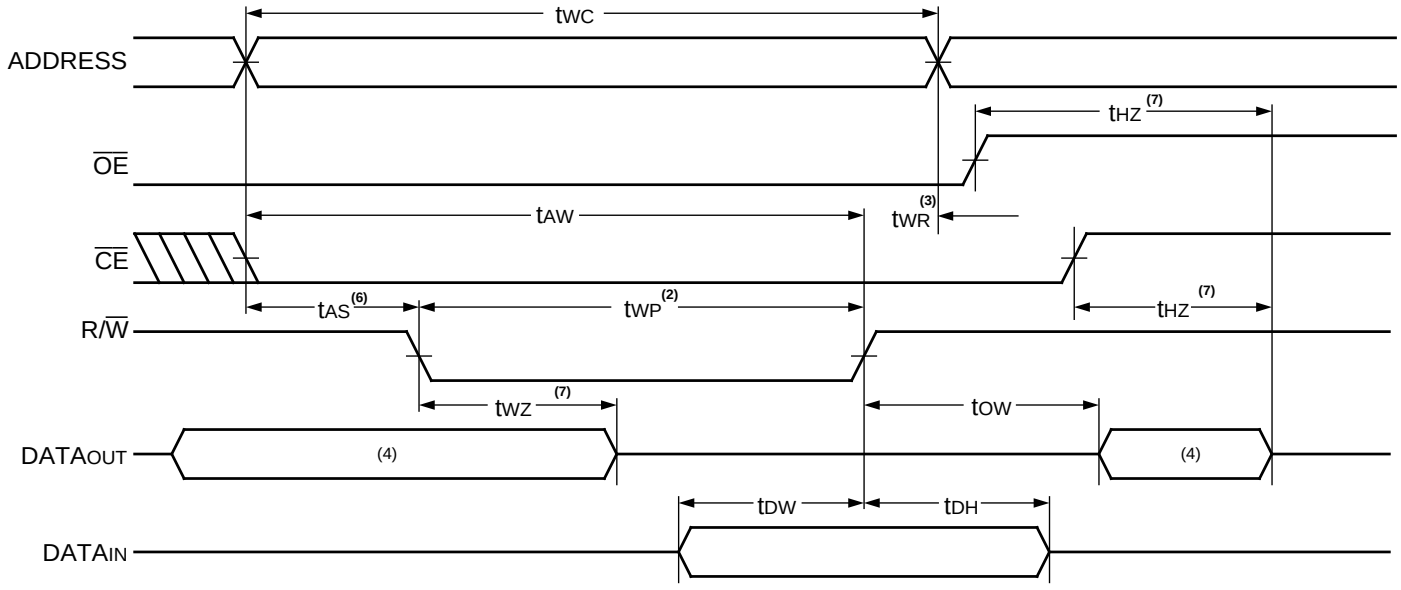
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(4)

Symbol	Parameter	70121X25 70125X25		70121X35 70125X35		70121X45 70125X45		70121X55 70125X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
t_{WC}	Write Cycle Time(3)	25	—	35	—	45	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write	20	—	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End-of-Write	20	—	30	—	35	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width(6)	20	—	30	—	35	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	12	—	20	—	20	—	20	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	10	—	15	—	20	—	30	ns
t_{DH}	Data Hold Time(5)	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enabled to Output in High-Z(1,2)	—	10	—	15	—	20	—	30	ns
t_{OW}	Output Active from End-of-Write(1,2)	0	—	0	—	0	—	0	—	ns

NOTES:
2654 tbl 09

1. Transition is measured ±500mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter guaranteed by device characterization, but is not production tested.
3. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$, since $R/\overline{W} = V_{IL}$ must occur after t_{BAA} .
4. "X" in part numbers indicates power rating (S or L).
5. The specified t_{DH} must be met by the device supplying write date to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature. The actual t_{DH} will always be smaller than the actual t_{OW}.
6. If $\overline{OE}$ is low during a $R/\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WZ} + t_{DW}$) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is High during a $R/\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, $R/\overline{W}$ CONTROLLED TIMING(1,5,8)



NOTES:
2654 drw 07

1. $R/\overline{W}$ or $\overline{CE}$ must be High during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE} = V_{IL}$ and a $R/\overline{W} = V_{IL}$
3. t_{WR} is measured from the earlier of $\overline{CE}$ or $R/\overline{W}$ going High to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ Low transition occurs simultaneously with or after the $R/\overline{W}$ Low transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or $R/\overline{W}$) is asserted last.
7. This parameter is determined be device characterization, but is not production tested. Transition is measured +/- 500mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during a $R/\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WZ} + t_{DW}$) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is High during a $R/\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

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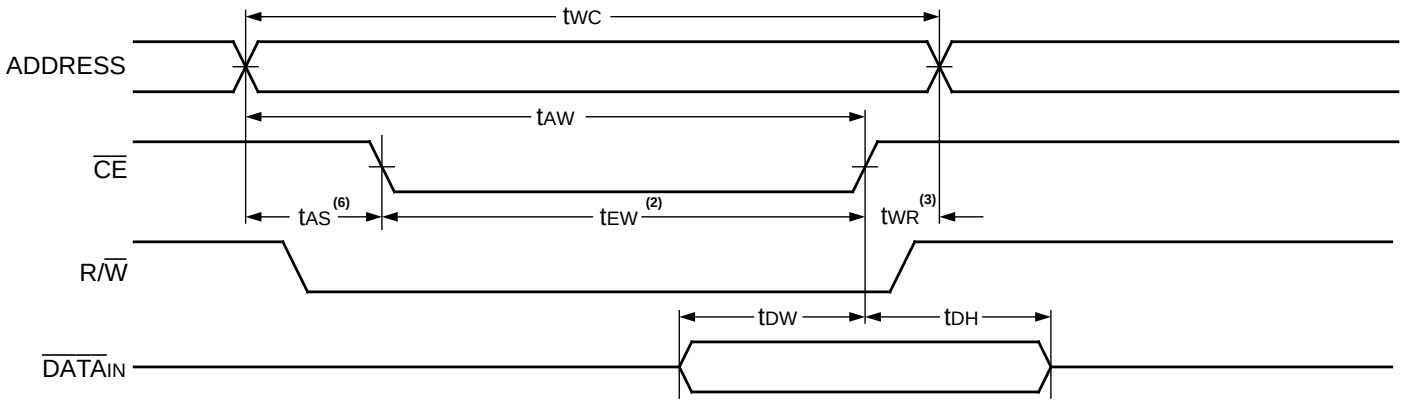
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,5)



2654 drw 08

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be High during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE}$ = V_{IL} and a R/$\overline{W}$ = V_{IL}
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going High to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ Low transition occurs simultaneously with or after the R/$\overline{W}$ Low transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined be device characterization, but is not production tested. Transition is measured +/- 500mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(6)

Symbol	Parameter	70121X25 70125X25		70121X35 70125X35		70121X45 70125X45		70121X55 70125X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Busy Timing (For Master IDT70121 Only)										
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	20	—	20	—	20	—	30	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	20	—	20	—	20	—	30	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	20	—	20	—	30	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	20	—	20	—	30	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	50	—	60	—	70	—	80	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	35	—	45	—	55	—	65	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(3)	—	30	—	30	—	35	—	45	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	15	—	20	—	20	—	20	—	ns
Busy Timing (For Slave IDT70125 Only)										
t_{WB}	Write to $\overline{BUSY}$ Input(4)	0	—	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	15	—	20	—	20	—	20	—	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	50	—	60	—	70	—	80	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	35	—	45	—	55	—	65	ns

2654 tbl 10

NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$".
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} – t_{WP} (actual), or t_{DDD} – t_{DW} (actual).
4. To ensure that a write cycle is inhibited on port 'B' during contention on port 'A'..
5. To ensure that a write cycle is completed on port 'B' after contention on port 'A'.
6. "X" in part numbers indicates power rating (S or L).

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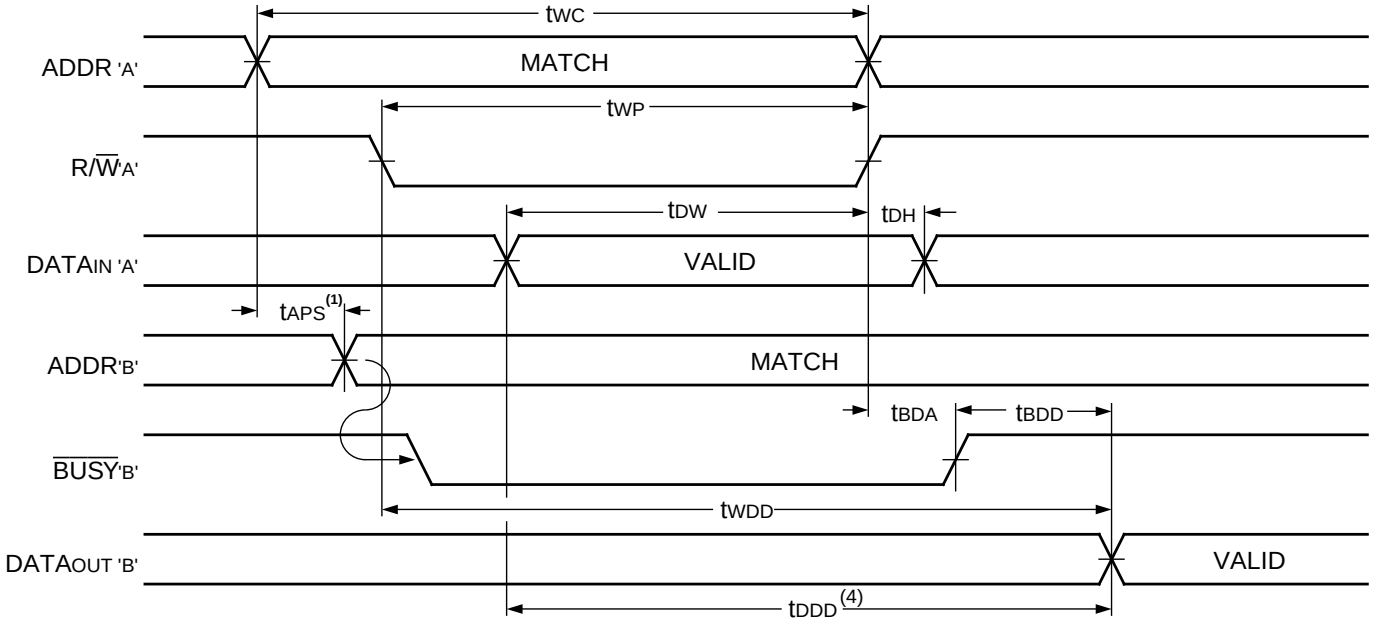
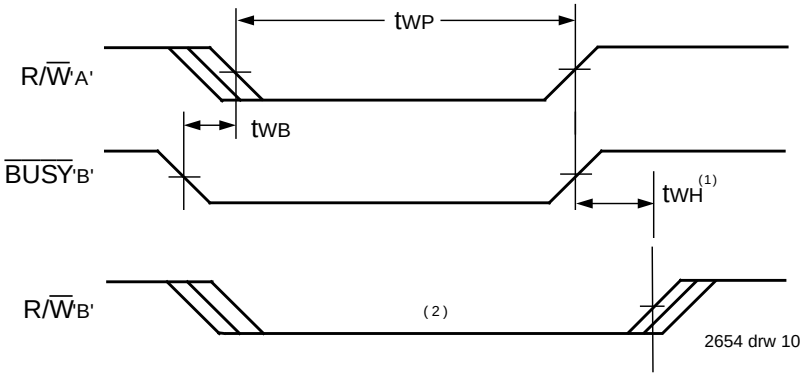
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$ (1,2,3)



2654 drw 09

NOTES:
1. To ensure that the earlier of the two ports wins. t_{APS} is ignored for Slave (IDT 70125).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
3. $\overline{OE} = V_{IL}$ for the reading port.
4. $\overline{All}$ timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port 'B' is opposite from port 'A'.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$



2654 drw 10

NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (slave) and output (master).
2. $\overline{BUSY}$ is asserted on port 'B' blocking $R/\overline{W}_{B'}$, until $\overline{BUSY}_{B'}$ goes High.
3. All timing is the same for left and right ports. Port 'A' may be either left or right port. Port 'B' is the opposite from port 'A'.

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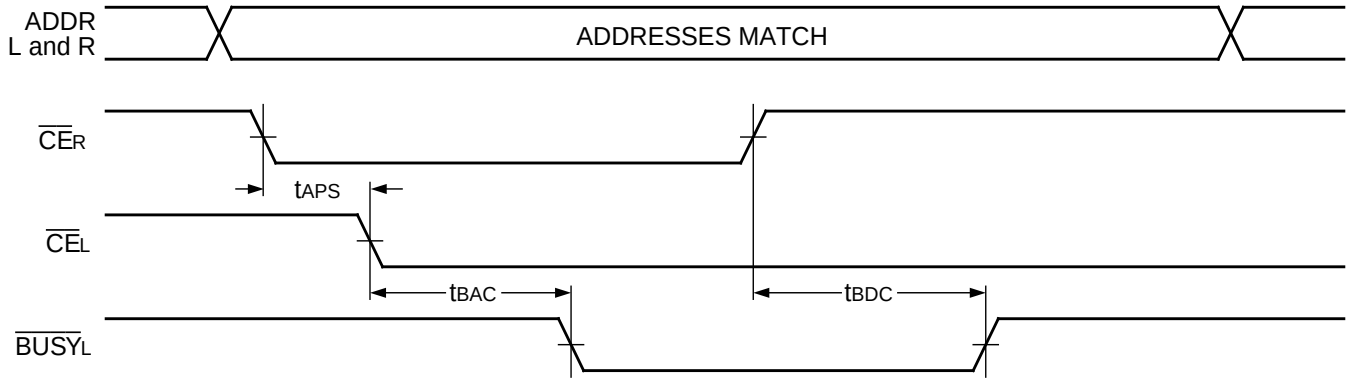
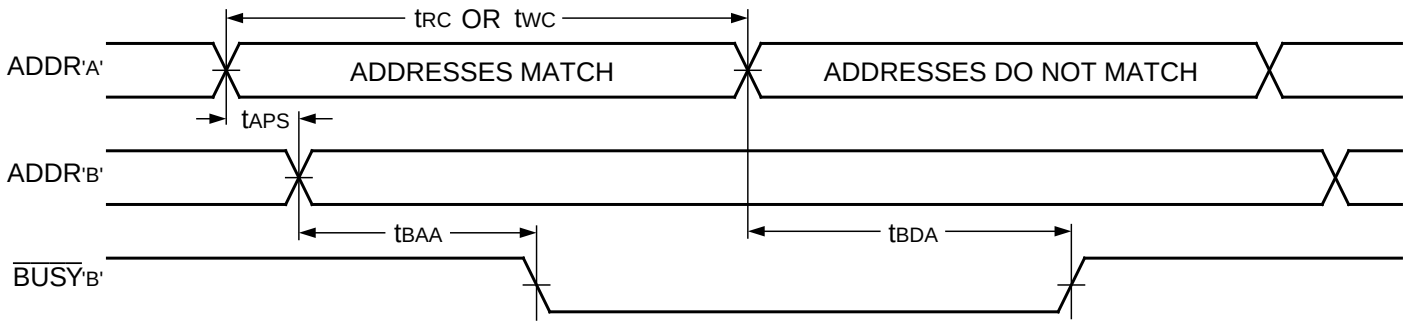
TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING(1)



2654 drw 12

NOTES:
1. All timing is the same for left and right ports. Port 'A' may be either left or right port. Port 'B' is the opposite from port 'A'.
2. If tAPS is not satisified, the BUSY will be asserted on one side or the other, but there is no guarantee on which side BUSY will be asserted (70121 only).

TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY ADDRESS (1)



2654 drw 13

NOTES:
1. All timing is the same for left and right ports. Port 'A' may be either left or right port. Port 'B' is the opposite from port 'A'.
2. If t_{APS} is not satisified, the $\overline{BUSY}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted (70121 only).

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1)

Symbol	Parameter	70121X25 70125X25 Min.	70121X25 70125X25 Max.	70121X35 70125X35 Min.	70121X35 70125X35 Max.	70121X45 70125X45 Min.	70121X45 70125X45 Max.	70121X55 70125X55 Min.	70121X55 70125X55 Max.	Unit
Interrupt Timing										
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	25	—	40	—	45	ns
tINR	Interrupt Reset Time	—	25	—	35	—	40	—	45	ns

NOTE: 2654 tbl 11
1. "X" in part numbers indicates power rating (S or L).

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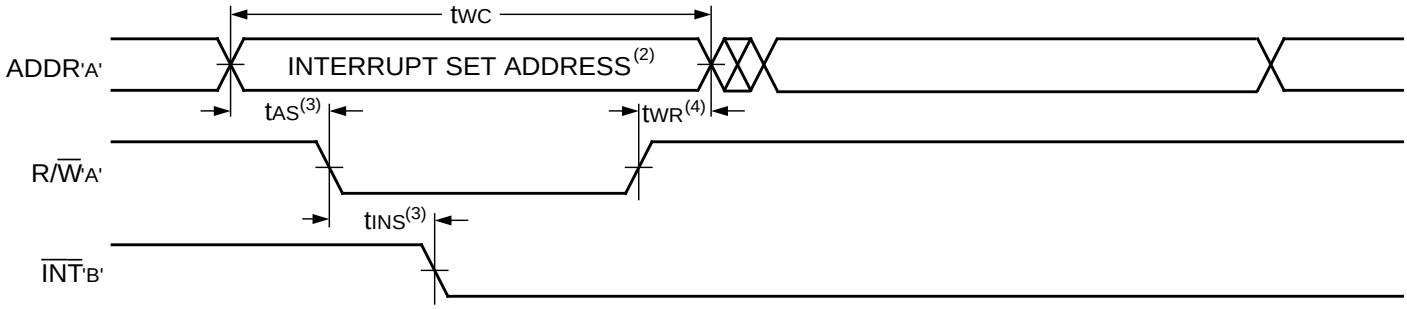
TIMING WAVEFORM OF INTERRUPT MODE



2654 drw 14

NOTES:.
1. All timing is the same for left and right ports. Port 'A' may be either left or right port. Port 'B' is the opposite from port 'A'.
2. See Interupt Truth Table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TRUTH TABLE I – NON-CONTENTION READ/WRITE CONTROL(4)

Left or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D0–8	Function
X	H	X	Z	Port Disabled and in Power-Down Mode, ISB2 or ISB4
X	H	X	Z	$\overline{CE}_R$ = $\overline{CE}_L$ = H, Power-Down Mode, ISB1 or ISB3
L	L	X	DATAIN	Data on Port Written Into Memory(2)
H	L	L	DATAOUT	Data in Memory Output on Port(3)
H	L	H	Z	High-impedance Outputs

NOTES: 2654 tbl 12
1. A0L – A10L ≠ A0R – A10R.
2. If $\overline{BUSY}$ = VIL, data is not written.
3. If $\overline{BUSY}$ = VIL, data may not be valid, see tWDD and tDDD timing.
4. 'H' = VIH, 'L' = VIL, 'X' = DON'T CARE, 'Z' = High-impedance.

TRUTH TABLE II – INTERRUPT FLAG(1,4)

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A0L – A10L	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A0L – A10R	$\overline{INT}_R$	Function
L	L	X	7FF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	7FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES: 2654 tbl 13
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = VIH
2. If $\overline{BUSY}_L$ = VIL, then No Change.
3. If $\overline{BUSY}_R$ = VIL, then No Change.
4. 'H' = VIH,' L' = VIL,' X' = DON'T CARE.

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FUNCTIONAL DESCRIPTION

The IDT70121/125 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70121/125 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FE (HEX), where a write is defined as the $\overline{CE} = R/\overline{W} = V_{IL}$ per the Truth Table. The left port clears the interrupt by access address location 7FE access when $\overline{CE}_R = \overline{OE}_R = V_{IL}, R/\overline{W}$ is a "Don't Care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must access the memory location 7FF. The message (9 bits) at 7FE or 7FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is “Busy”. The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by using the IDT70125 (SLAVE). In the IDT70125, the busy pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT70121/125 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT70121/125 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT70121 RAM the busy pin is an output of the part, and the busy pin is an input of the IDT70125 as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write

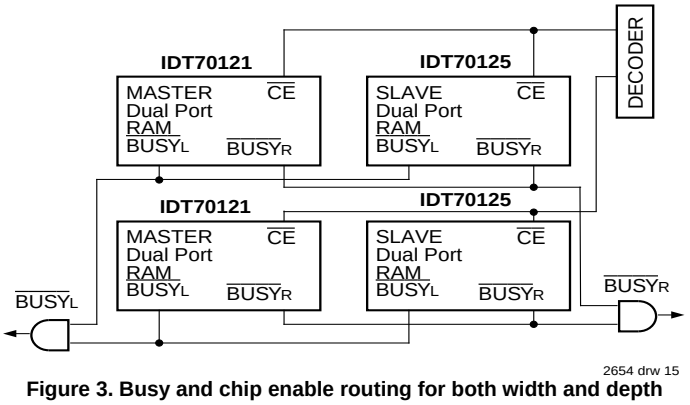

Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70121 (Master) and IDT70125 (Slave) RAMs.

operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the $R/\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

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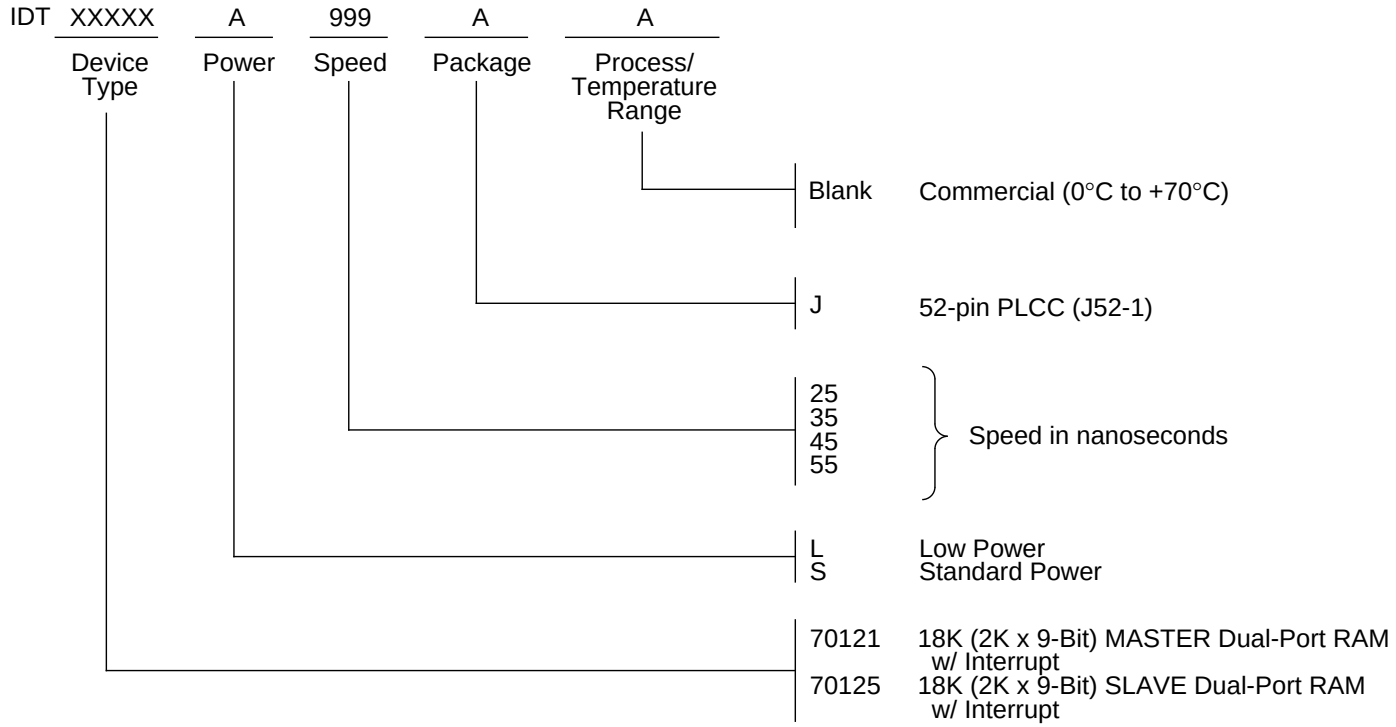
ORDERING INFORMATION



2654 drw 16

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