Stereo 2.6W Audio Amplifier(With Gain Control)

Features

- Low operating current with 6mA
- Improved depop circuitry to eliminate turn-on transients in outputs
- High PSRR
- Internal gain control, eliminate external components.
- 2.6W per channel output power into 3Ω load at 5V, BTL mode
- Multiple input modes allowable selected by HP /$\overline{\text{LINE}}$ pin (APA2030)
- Two output modes allowable with BTL and SE modes selected by SE/$\overline{\text{BTL}}$ pin (for APA2030 only)
- Low current consumption in shutdown mode (50μA)
- Short Circuit Protection
- TSSOP-24-P (APA2030) and TSSOP-20-P (APA2031) with thermal pad package.

Applications

- NoteBook PC
- LCD Monitor

General Description

APA2030/1 is a monolithic integrated circuit, which provides internal gain control, and a stereo bridged audio power amplifiers capable of producing 2.6W (1.9W) into 3Ω with less than 10% (1.0%) THD+N. By control the two gain setting pins, Gain0 and Gain1, The amplifier can provide 6dB, 10dB, 15.6dB, and 21.6dB gain settings. The advantage of internal gain setting can be less components and PCB area. Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in APA2030/1, that reduces pops and clicks noise during power up or shutdown mode operation. It also improved the power off pop noise and protects the chip from being destroyed by over temperature and short current failure. To simplify the audio system design APA2030 combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/$\overline{\text{BTL}}$ input control pin signal. Besides the multiple input selections is used for portable audio system. APA2031 eliminates both input selection and single-end (SE) mode function to simplifying the design and save the PCB space.

Ordering and Marking Information

APA2030/1 □□-□□□

- Lead Free Code
- Handling Code
- Temp. Range
- Package Code

Package Code
R : TSSOP-P *
Temp. Range
I : - 40 to 85 °C
Handling Code
TU : Tube TR : Tape & Reel
TY : Tray
Lead Free Code
L : Lead Free Device Blank : Original Device

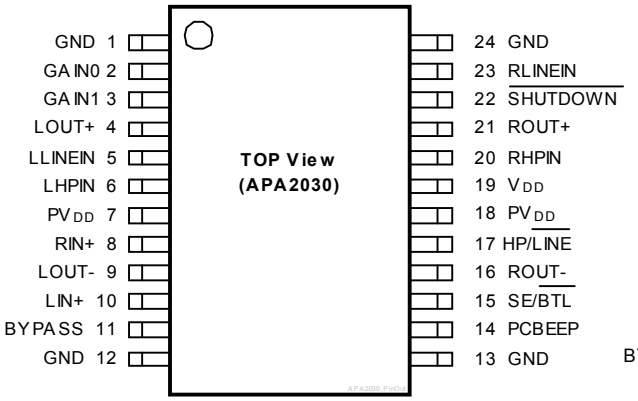
APA2030/1 R : APA2030/1 XXXXX

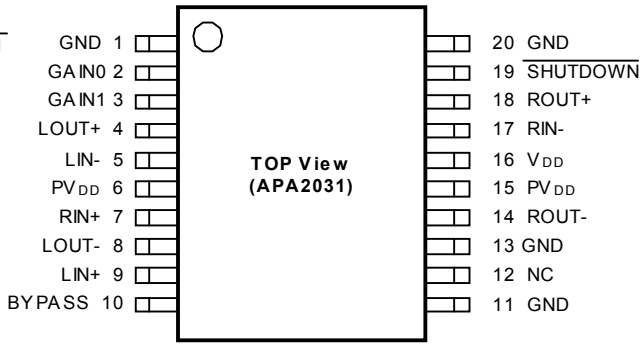
XXXXX - Date Code

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

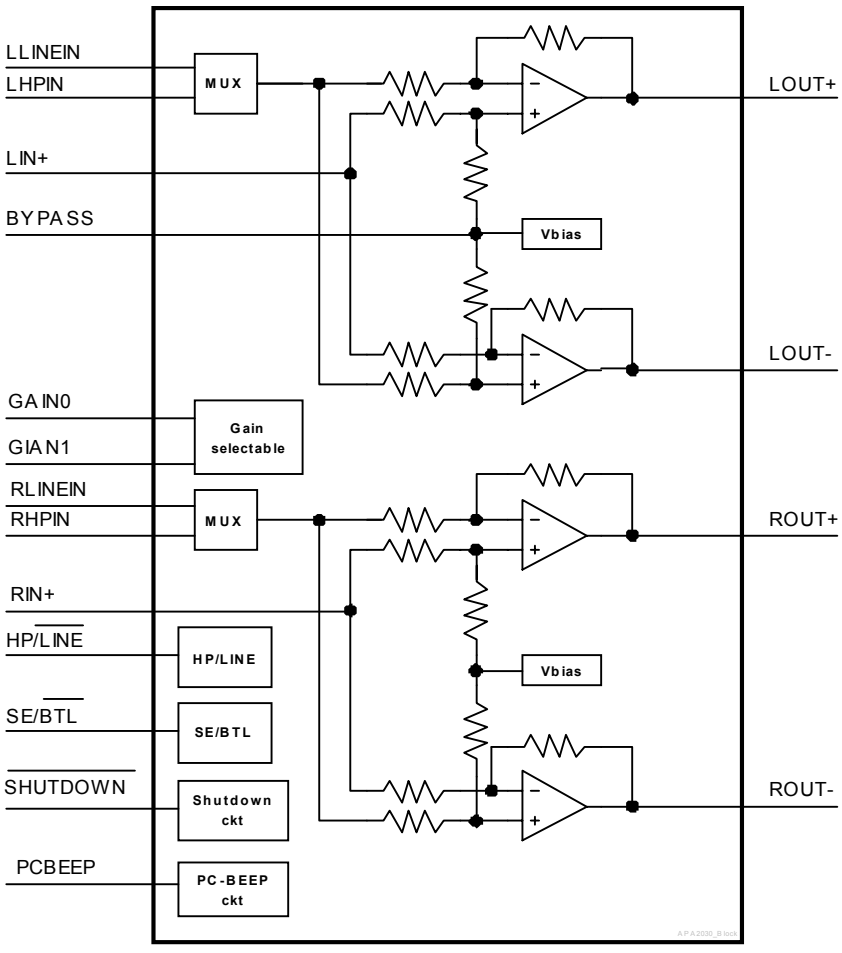
Rev. A.2 -Apr., 2004

Pin Assignment



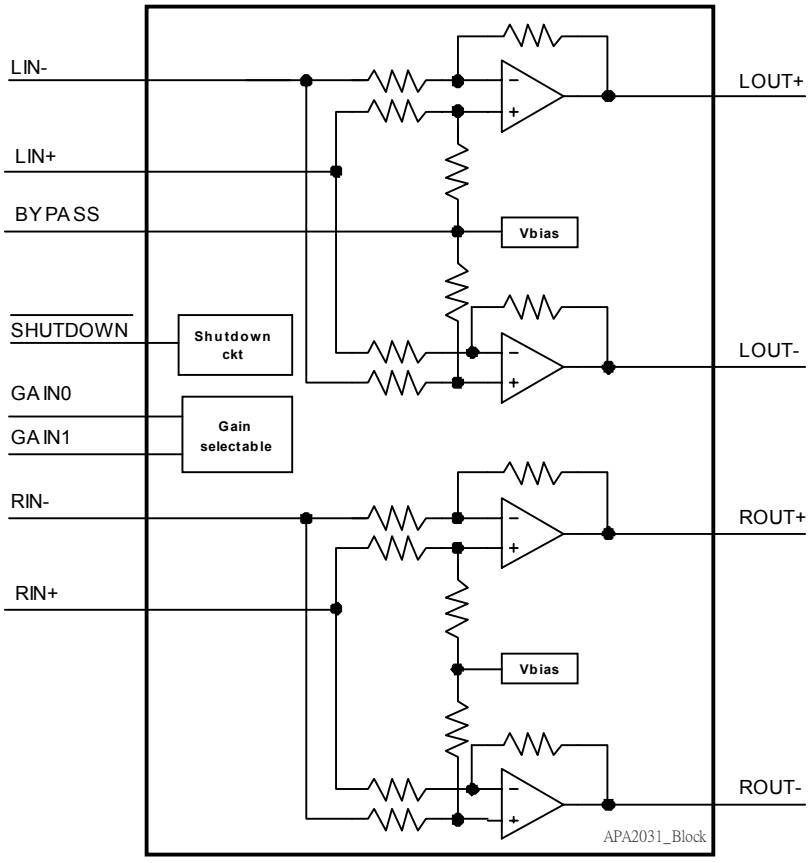


Block Diagram



APA2030

Block Diagram



APA2031

Absolute Maximum Ratings

(Over operating free-air temperature range unless otherwise noted.)

Parameter	Rating
Supply voltage range, V_{DD}, PV_{DD}	-0.3V to 6V
Input voltage range at SE/$\overline{BTL}$, HP/$\overline{LINE}$, $\overline{SHUTDOWN}$,	-0.3V to V_{DD}
Operating ambient temperature range, T_A	-40°C to 85°C
Maximum junction temperature, T_J	Internal Limited
Storage temperature range, T_{STG}	-65°C to 150°C
Soldering Temperature, 10 seconds, T_S	260°C
Electrostatic Discharge, V_{ESD}	-3000 to 3000*1 -200 to 200*2
Power dissipation, P_D	Internal Limited

Note:

*1. Human body model: C=100pF, R=1500Ω, 3 positives pulse plus 3 negative pulses

*2. Machine model: C=200pF, L=0.5mH, 3 positive pulses plus 3 negative pulses

Recommended Operating Conditions

Supply Voltage, V_{DD}.....4.5V to 5.5V

Thermal Characteristics

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal Resistance from Junction to Ambient in Free Air TSSOP-P24* TSSOP-P20*	 45 48	°C/W

* 5 in^2 printed circuit board with 2oz trace and copper pad through 9 25mil diameter vias.
The thermal pad on the TSSOP_P package with solder on the printed circuit board.

Electrical Characteristics

(V_{DD}=5V,-20°C<T_A<85°C, unless otherwise noted.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.3		5.5	V
I_{DD}	Supply current	SE/$\overline{BTL}$ = 0V		6	12	mA
		SE/$\overline{BTL}$ = 5V		4	8	mA
I_{SD}	Supply current in shutdown mode	$\overline{SHUTDOWN}$ = 0V		50	300	µA
V_{IH}	High level threshold Voltage	$\overline{SHUTDOWN}$, GAIN0, GAIN1	2			V
		SE/$\overline{BTL}$, HP/$\overline{LINE}$	4			V
V_{IL}	Low level threshold Voltage	$\overline{SHUTDOWN}$, GAIN0, GAIN1			0.8	V
		SE/$\overline{BTL}$, HP/$\overline{LINE}$			3	V
I_I	Input current	$\overline{SHUTDOWN}$, SE/$\overline{BTL}$, HP/$\overline{LINE}$, GAIN0, GAIN1		5		nA
V_{ICM}	Common mode Input voltage		VDD-1.0			V
V_{OS}	Output differential voltage			5		mV
	PC_beep trigger level			1		Vp.p

Electical Characteristics (Cont.)

Operating Characteristics, BTL mode

Vdd=5V, T_A=25°C, Rl=4Ω, Gain=6dB, (Unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
P_O	Maximum output power	THD=10%, Fin=1khz, RL=3Ω		2.6		W
		THD=10%, Fin=1khz, RL=4Ω		2.3		W
		THD=10%, Fin=1khz, RL=8Ω		1.5		W
		THD=1%, Fin=1khz, RL=3Ω		1.9		W
		THD=1%, Fin=1khz, RL=4Ω		1.7		W
		THD=1%, Fin=1khz, RL=8Ω	1	1.1		W
THD+N	Total harmonic distortion plus noise	Po=1.1W, RL=4Ω Fin=1khz		0.05		%
		Po=0.7W, RL=8Ω, Fin=1khz		0.04		%
PSRR	Power ripple rejection ratio	Vin=0.2Vrms, Rl=8Ω, Cb=0.47µf, f=120Hz		85		dB
xtalk	Channel separation	f=1khz, Cb=0.47µf,		95		dB
	HP/$\overline{\text{LINE}}$ input separation	f=1khz, Cb=0.47µf,		80		dB
S/N	Signal to noise ratio	Po=1.1W, Rl=8Ω , A_weight		105		dB

Operating Characteristics, SE mode (for APA2030 only)

Vdd=5V, T_A=25°C, Rl=32Ω, Gain=4, 1dB, (Unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
P_O	Maximum output power	THD=10%, Fin=1khz, RL=32Ω		110		mW
		THD=1%, Fin=1khz, RL=32Ω		90		mW
THD+N	Total harmonic distortion plus noise	Po=75mW, RL=32Ω .Fin=1khz		0.03		%
PSRR	Power ripple rejection ratio	Vin=0.2Vrms, Rl=32Ω, Cb=0.47µf, f=120,		55		dB
	SE/$\overline{\text{BTL}}$ attenuation			80		dB
xtalk	Channel separation	f=1khz, Cb=0.47µf,		65		dB
	HP/$\overline{\text{LINE}}$ input separation	f=1khz, Cb=0.47µf, BTL		80		dB
S/N	Signal to noise ratio	Po=75mW, Rl=32Ω, A_weight,		100		dB

Pin Descriptions

APA2030

Pin name	Pin no.	Config.	Function Description
GND	1, 12, 13, 24	-	Ground connection, Connected to thermal pad.
GAIN0	2	I/P	Input signal for internal gain setting
GAIN1	3	I/P	Input signal for internal gain setting
LOUT+	4	O/P	Left channel positive output in BTL mode and SE mode
LLINEIN	5	I/P	Left channel line input terminal, selected when HP/$\overline{\text{LINE}}$ is held low.
RLINEIN	23	I/P	Right channel line input terminal, selected when HP/$\overline{\text{LINE}}$ is held low.
LHPIN	6	O/P	Left channel headphone input terminal, selected when HP/$\overline{\text{LINE}}$ is held high.
PVDD	7, 18	-	Supply voltage only for power amplifier
RIN+	8	I/P	Right channel positive signal input, when differential signal is accepted.
LOUT-	9	O/P	Left channel negative output in BTL mode and high impedance in SE mode
LIN+	10	I/P	Left channel positive signal input, when differential signal is accepted.
BYPASS	11	-	Bypass voltage
PCBEEP	14	I/P	PC-beep signal input
SE/$\overline{\text{BTL}}$	15	I/P	Output mode control input pin, high for SE output mode and low for BTL mode
ROUT-	16	O/P	Right channel negative output in BTL mode and high impedance in SE mode
HP/$\overline{\text{LINE}}$	17	I/P	Multi-input selection input, headphone mode when held high, line-in mode when held low
VDD	19	-	Supply voltage for internal circuit excepting power amplifier.
RHPIN	20	I/P	Right channel headphone input terminal, selected when HP/$\overline{\text{LINE}}$ is held high.
ROUT+	21	O/P	Right channel positive output in BTL mode and SE mode
$\overline{\text{SHUTDOWN}}$	22	I/P	It will be into shutdown mode when pull low
RLINEIN	23	I/P	Right channel line input terminal, selected when HP/$\overline{\text{LINE}}$ is held low

APA2031

Pin name	Pin no.	Config.	Function Description
GND	1, 11, 13, 20	-	Ground connection, Connected to thermal pad.
GAIN0	2	I/P	Input signal for internal gain setting
GAIN1	3	I/P	Input signal for internal gain setting
LOUT+	4	O/P	Left channel positive output
LIN-	5	I/P	Left channel negative audio signal input
PVDD	6,15	-	Supply voltage only for power amplifier
RIN+	7	I/P	Right channel positive audio signal input
LOUT-	8	O/P	Left channel negative output
LIN+	9	I/P	Left channel positive audio signal input
BYPASS	10	-	Bypass voltage
NC	12	-	No connection
ROUT-	14	O/P	Right channel negative output
VDD	16	-	Supply voltage for internal circuit excepting power amplifier

Pin Description

APA2031

Pin name	Pin no.	Config.	Function Description
RIN+	17	I/P	Right channel negative audio signal input
ROUT+	18	O/P	Right channel positive output
$\overline{\text{SHUTDOWN}}$	19	I/P	It will be into shutdown mode when pull low

Control Input Table (for APA2030 only)

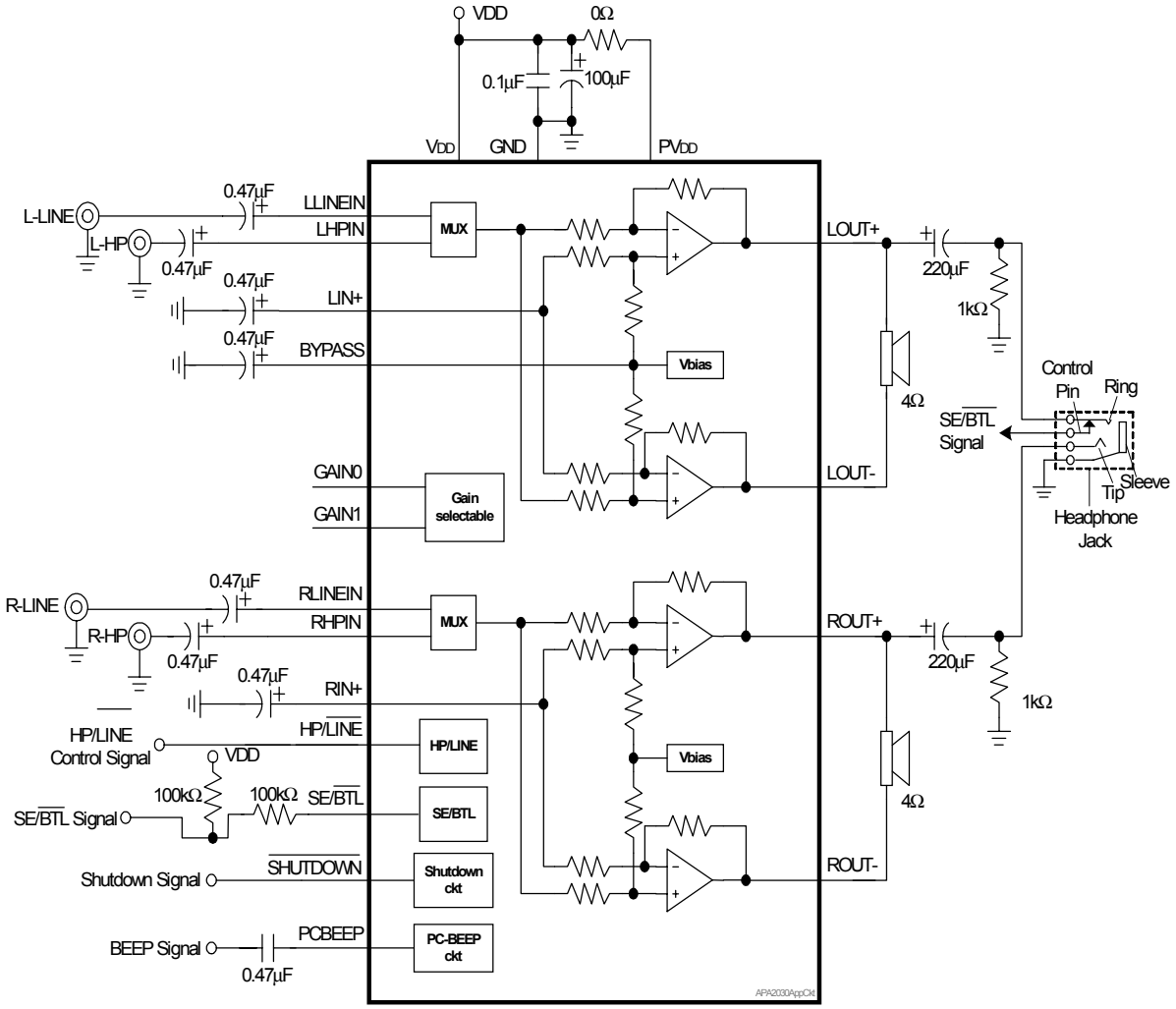
$\overline{\text{HP/ LINE}}$	$\overline{\text{SE/BTL}}$	$\overline{\text{SHUTDOWN}}$	PCBEEP	Operating mode
X	X	L	Disable	Shutdown mode
L	L	H	Disable	Line input, BTL out
H	L	H	Disable	HP input, BTL out
L	H	H	Disable	Line input, SE out
H	H	H	Disable	HP input, SE out
X	X	X	Enable	PCBEEP input, BTL out

Gain Setting Table (for both APA2030 and APA2031)

GAIN0	GAIN1	Ri	Rf	Av
0	0	90KΩ	90KΩ	6dB
0	1	69KΩ	111KΩ	10dB
1	0	42KΩ	138KΩ	15.6dB
1	1	25.7KΩ	154.3KΩ	21.6dB

Typical Application Circuit

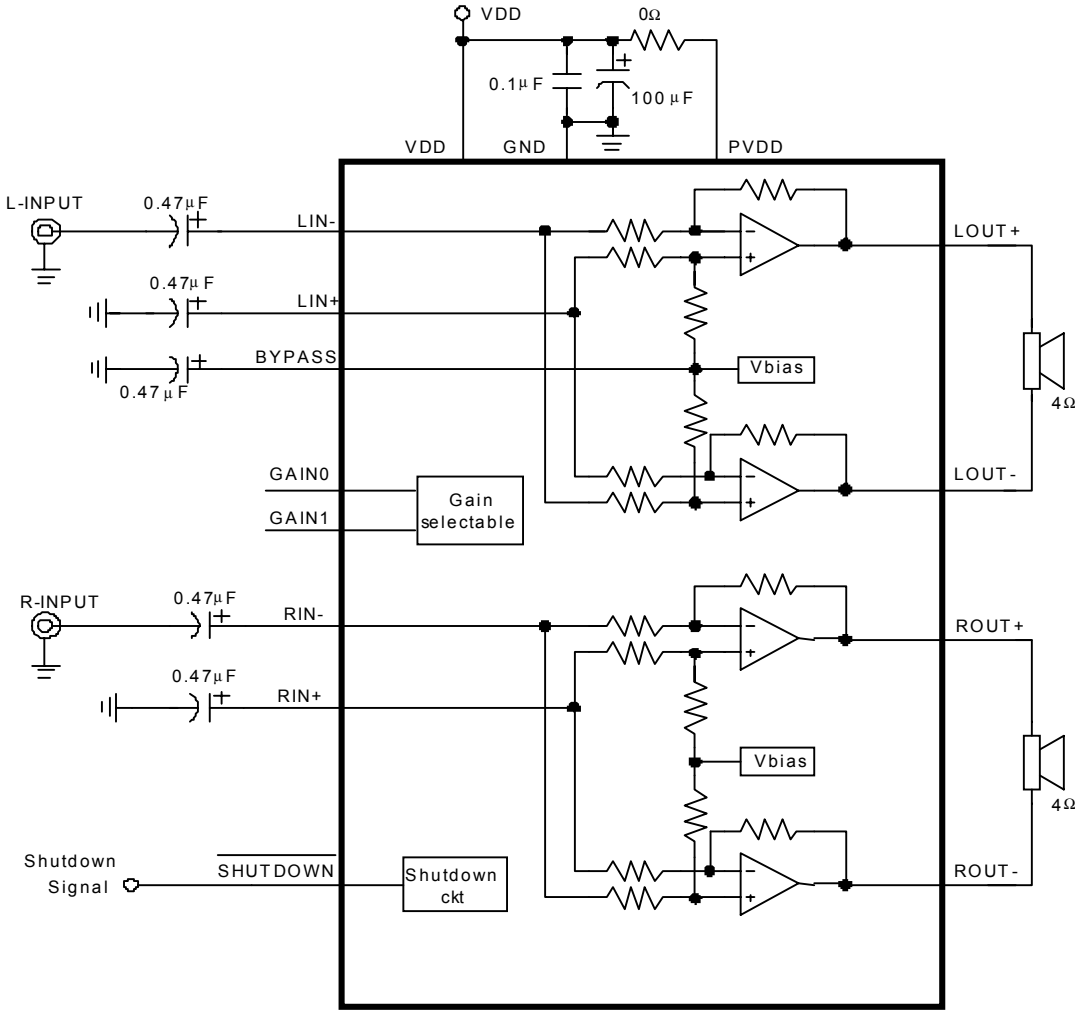
(for APA2030 using SE input signal)



APA 2030

Typical Application Circuit

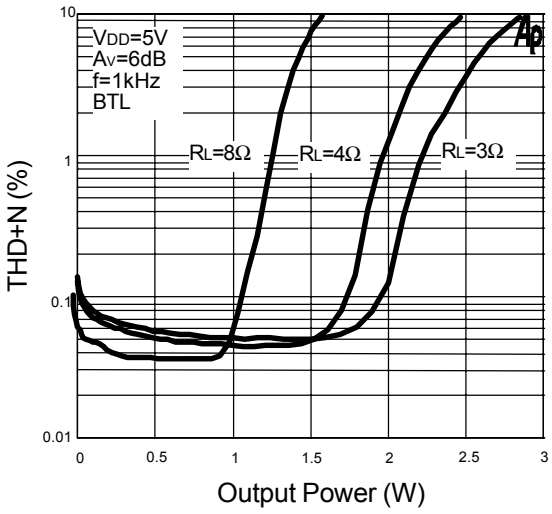
(for APA2031 using SE input signal)



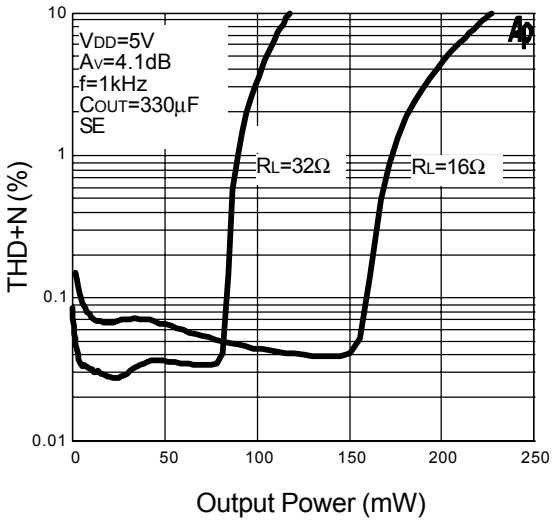
APA 2031

Typical Characteristics

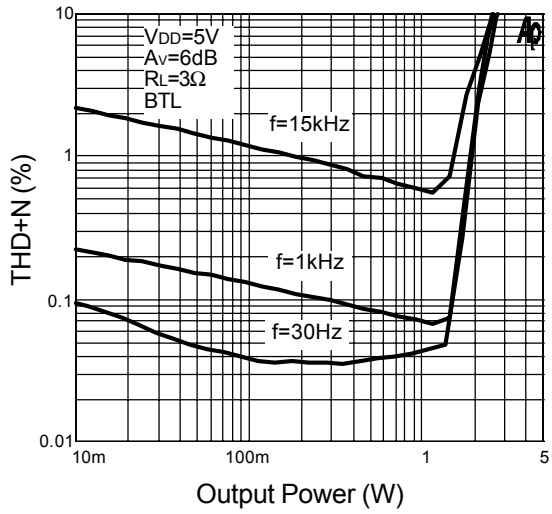
THD+N vs. Output Power



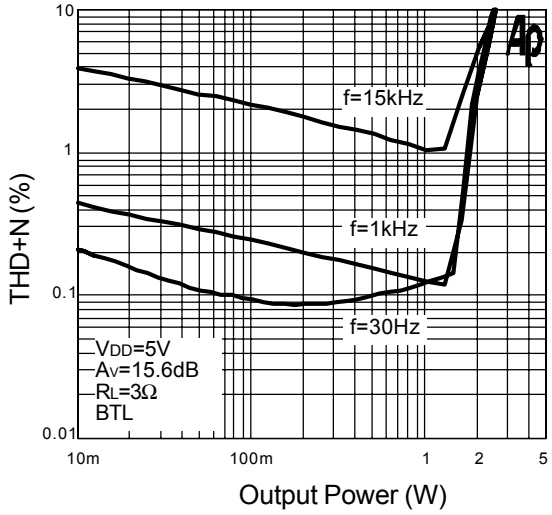
THD+N vs. Output Power



THD+N vs. Output Power

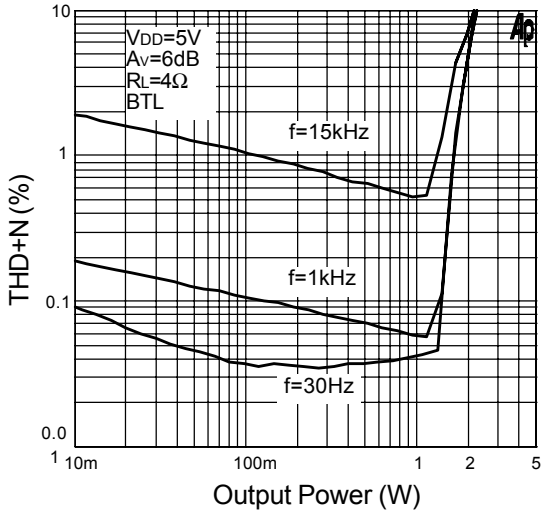


THD+N vs. Output Power

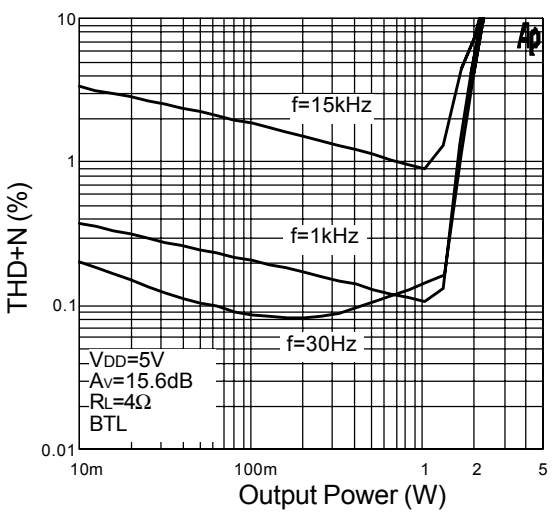


Typical Characteristics (Cont.)

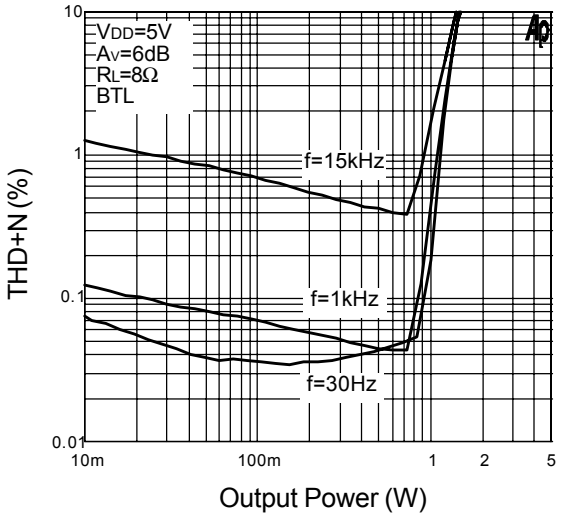
THD+N vs. Output Power



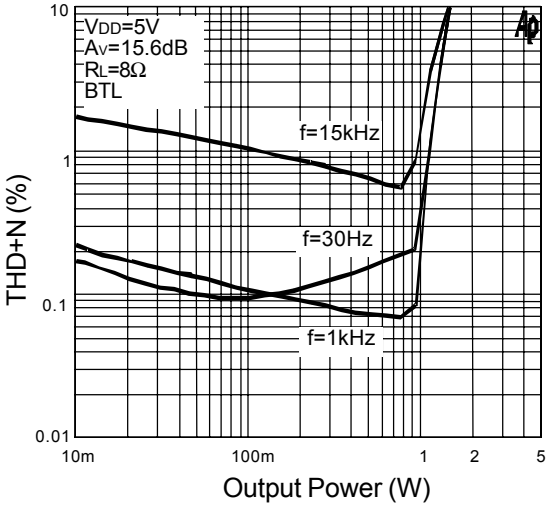
THD+N vs. Output Power



THD+N vs. Output Power

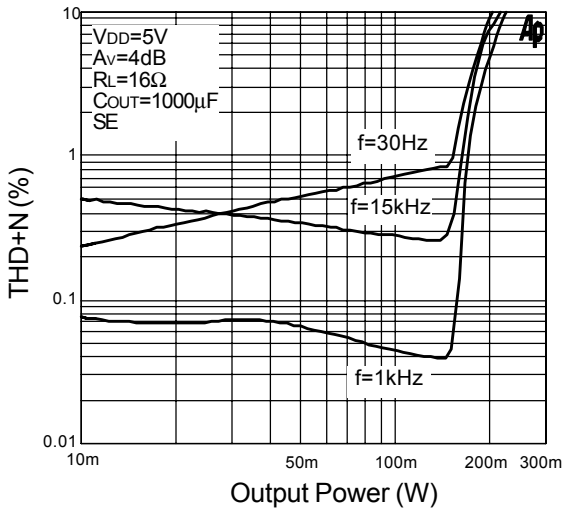


THD+N vs. Frequency

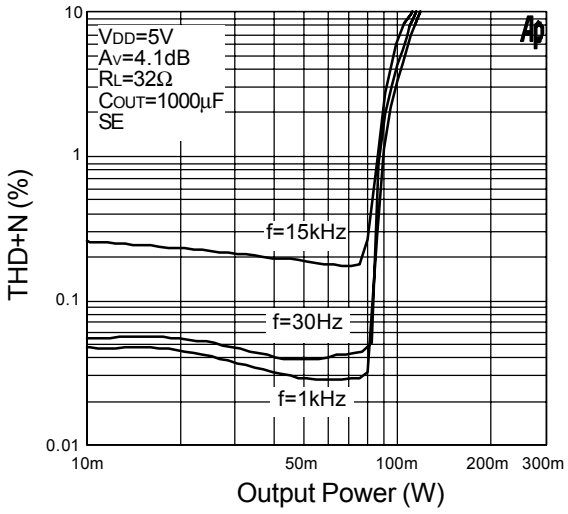


Typical Characteristics (Cont.)

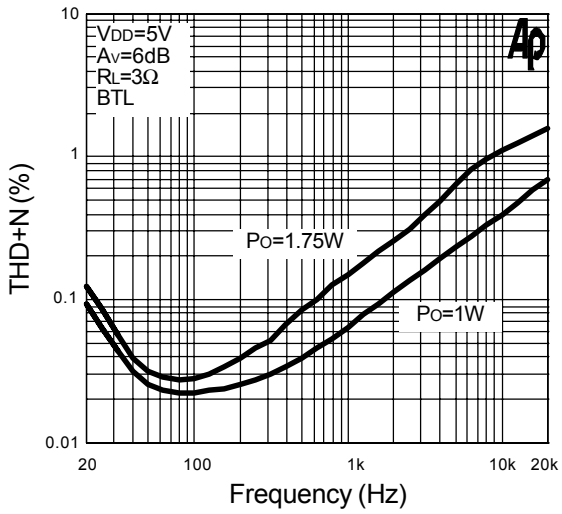
THD+N vs. Output Power



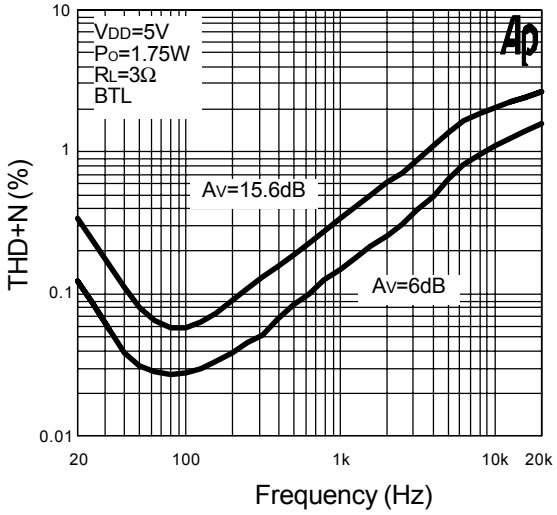
THD+N vs. Output Power



THD+N vs. Frequency

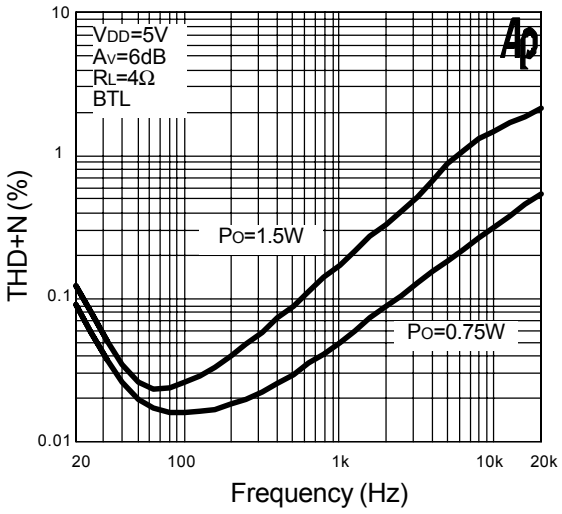


THD+N vs. Frequency

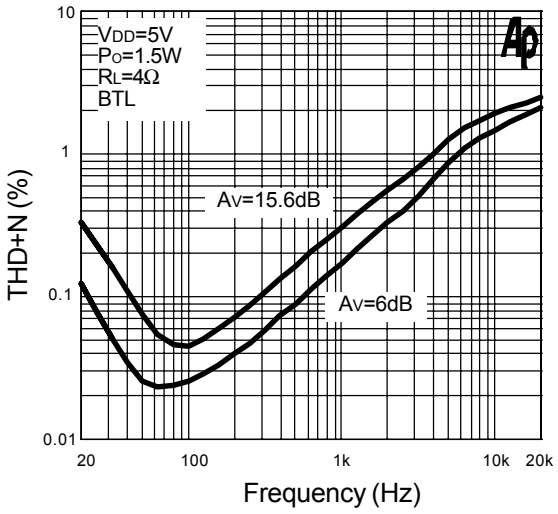


Typical Characteristics (Cont.)

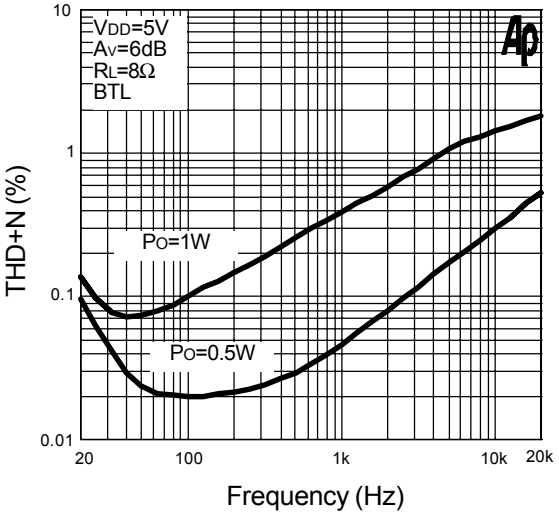
THD+N vs. Frequency



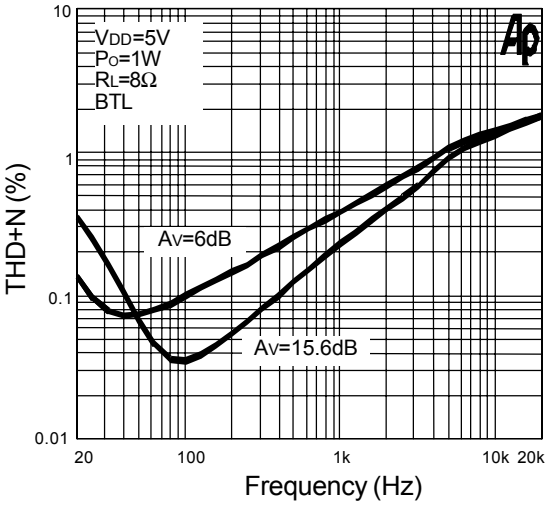
THD+N vs. Frequency



THD+N vs. Frequency

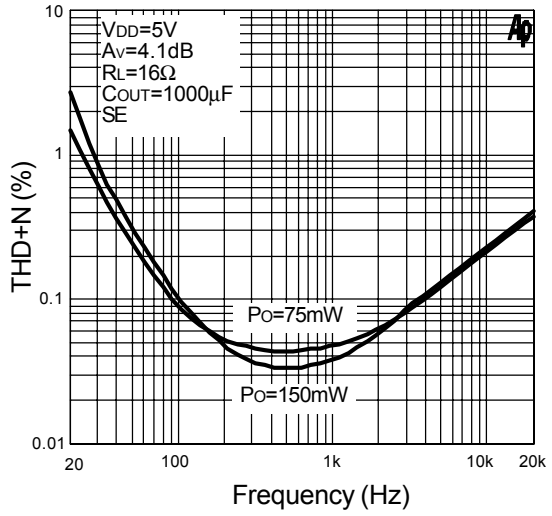


THD+N vs. Frequency

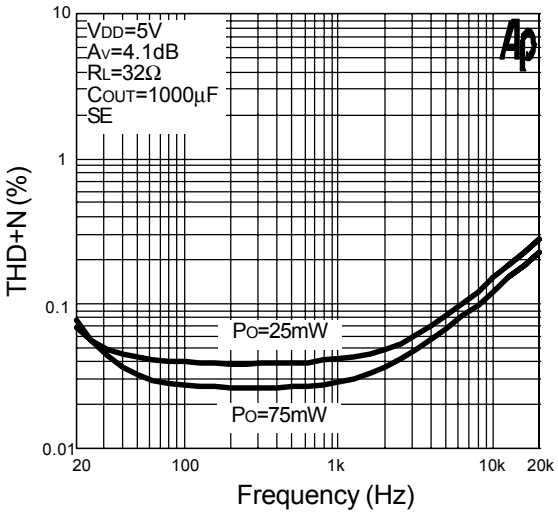


Typical Characteristics (Cont.)

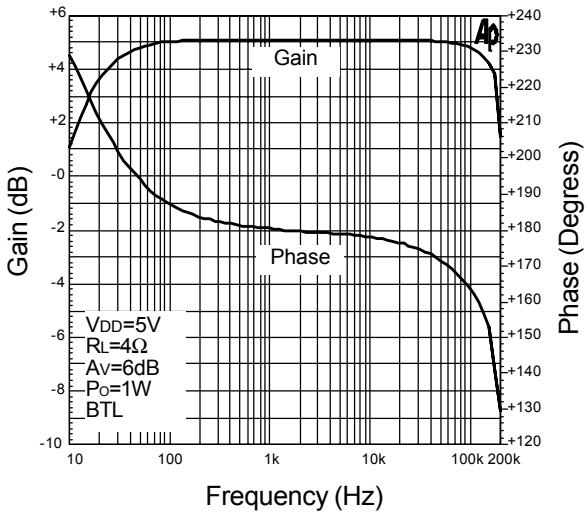
THD+N vs. Frequency



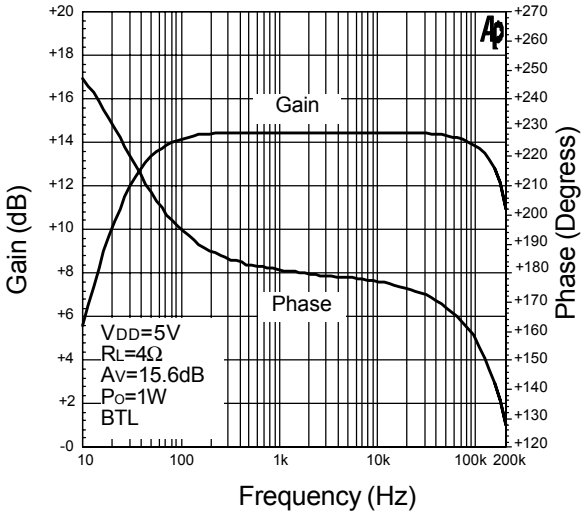
THD+N vs. Frequency



Frequency Response

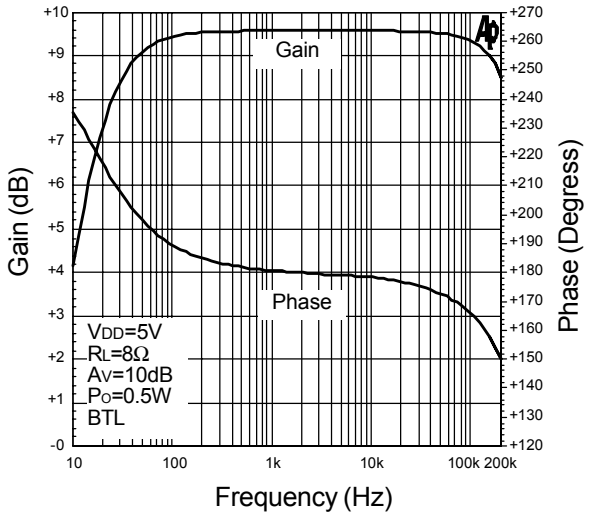


Frequency Response

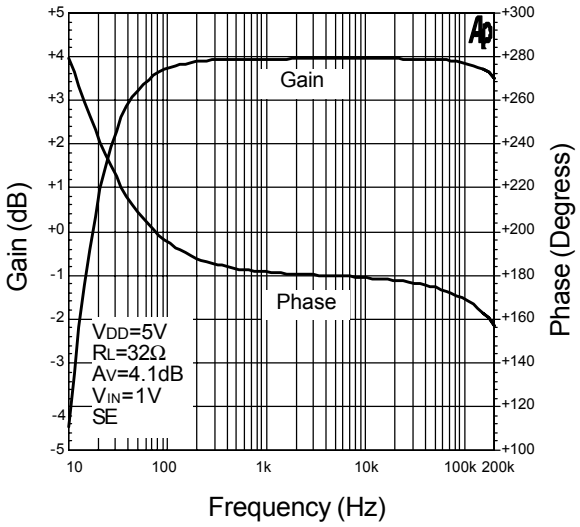


Typical Characteristics (Cont.)

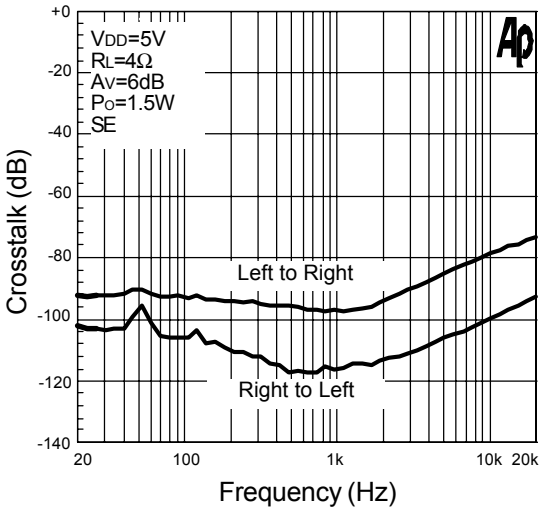
Frequency Response



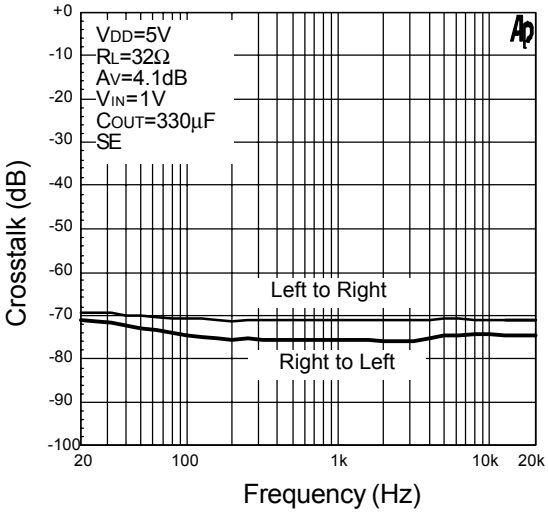
Frequency Response



Crosstalk vs. Frequency

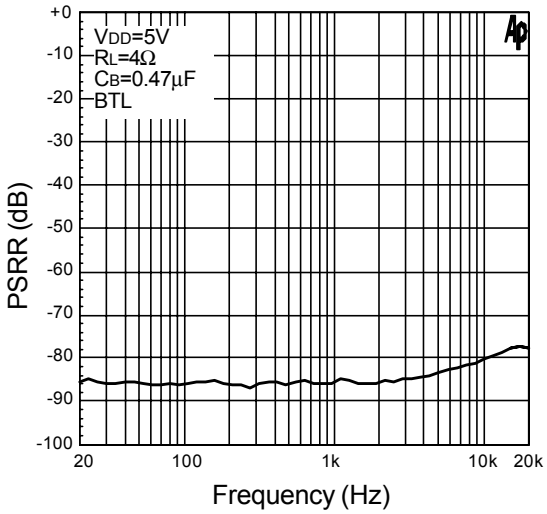


Crosstalk vs. Frequency

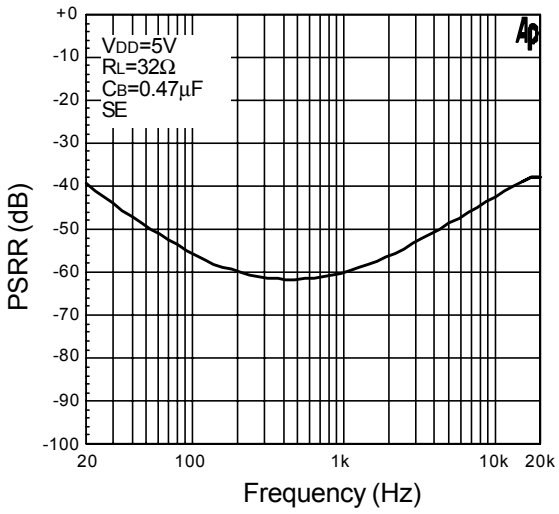


Typical Characteristics (Cont.)

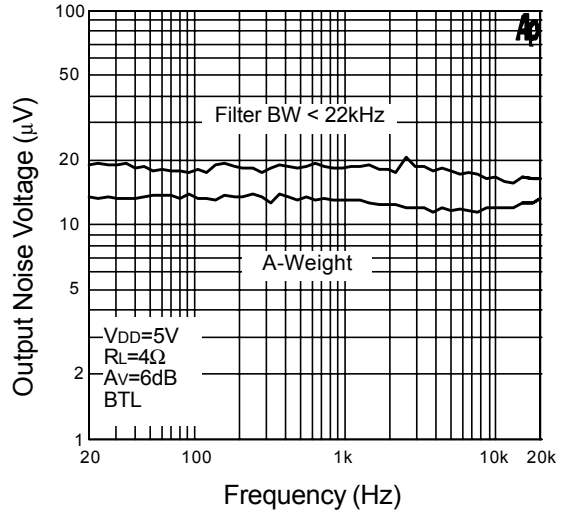
PSRR vs. Frequency



PSRR vs. Frequency



Output Noise Voltage vs. Frequency



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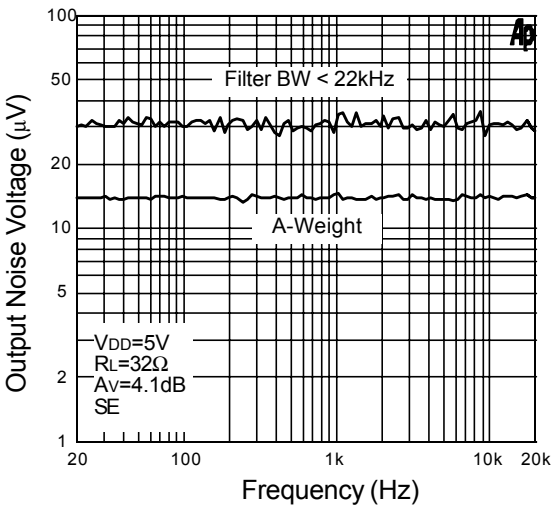
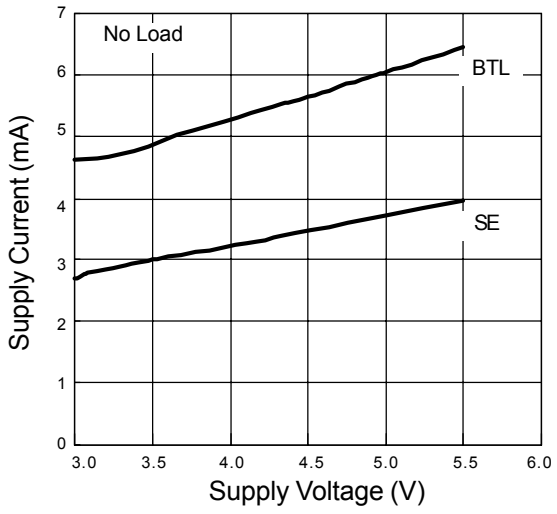
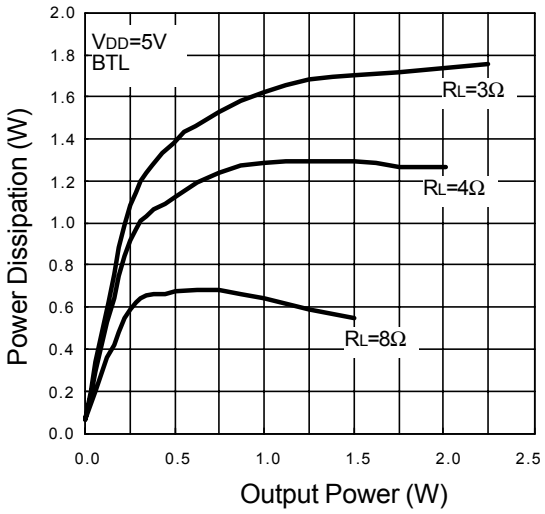


Typical Characteristics (Cont.)

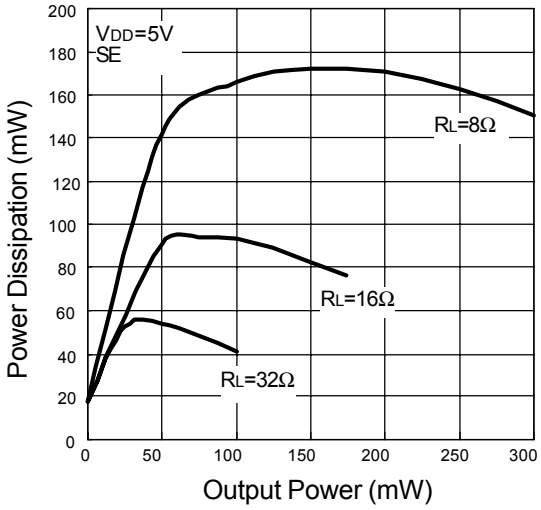
Supply Current vs. Supply Voltage



Power Dissipation vs. Output Power



Power Dissipation vs. Output Power



Application Descriptions

BTL Operation

The APA2030/1 has two pairs of operational amplifiers internally, allowed for different amplifier configurations.

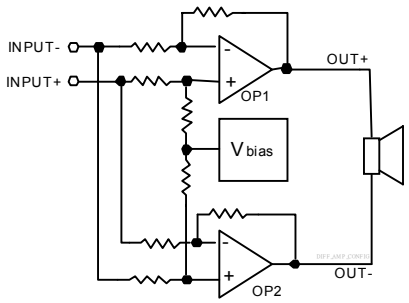


Figure 1: APA2030 internal configuration (each channel)

The OP1 and OP2 are all differential drive configuration, The differential drive configuration doubling the voltage swing on the load compare to the single-ending configuration, the differential gain for each channel is 2x(Gain of SE mode).

By driving the load differentially through outputs OUT+ and OUT-, an amplifier configuration commonly referred to as bridged mode is established. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus doubling the output swing for a specified supply voltage. Four times the output power is possible as compared to a SE amplifier under the same conditions. A BTL configuration, such as the one used in APA2030/1, also creates a second advantage over SE amplifiers. Since the differential outputs, ROUT+, ROUT-, LOUT+, and LOUT-, are biased at half-supply, no need DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

Single-Ended Operation (for APA2030 only)

Consider the single-supply SE configuration shown Application Circuit. A coupling capacitor is required to block the DC offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF) so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system (refer to the Output Coupling Capacitor).

The rules described should be following relationship:

$$\frac{1}{Cbypass \times 125k\Omega} \leq \frac{1}{R_i C_i} << \frac{1}{R_L C_C} \quad (1)$$

Output SE/$\overline{\text{BTL}}$ Operation (for APA2030 only)

The ability of the APA2030 to easily switch between BTL and SE modes is one of its most important costs saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated.

Internal to the APA2030, two separate amplifiers drive OUT+ and OUT- (see Figure 1). The SE/$\overline{\text{BTL}}$ input controls the operation of the follower amplifier that drives LOUT- and ROUT-.

- When SE/$\overline{\text{BTL}}$ is held low, the OP2 is actived and the APA2030 is in the BTL mode.
- When SE/$\overline{\text{BTL}}$ is held high, the OP2 is in a high output impedance state, which configures the APA2030 as SE driver from OUT+. I_{DD} is reduced by approximately one-half in SE mode.

Control of the SE/$\overline{\text{BTL}}$ input can be a logic-level TTL source or a resistor divider network or the stereo headphone jack with switch pin as shown in Application Circuit.

Application Descriptions

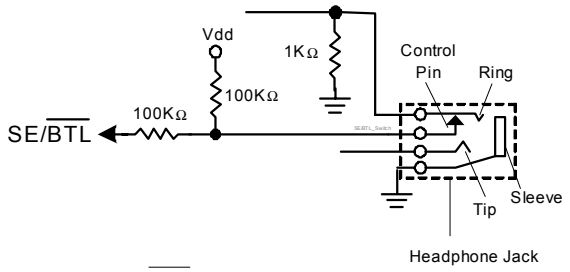


Figure 2: SE/$\overline{BTL}$ input selection by phonejack plug

In Figure 2, input SE/$\overline{BTL}$ operates as follows:

When the phonejack plug is inserted, the 1kΩ resistor is disconnected and the SE/BTL input is pulled high and enables the SE mode. When the input goes high level, the OUT- amplifier is shutdown causing the speaker to mute. The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

When there is no headphone plugged into the system, the contact pin of the headphone jack is connected from the signal pin, the voltage divider set up by resistors 100kΩ and 1kΩ. Resistor 1kΩ then pulls low the SE/BTL pin, enabling the BTL function.

Input HP/$\overline{LINE}$ Operation (for APA2030 only)

APA2030 amplifier has two separate inputs for each of the left and right stereo channels. An internal multiplexer selects which input will be connected to the amplifier based on the state of the HP/$\overline{LINE}$ pin on the IC.

- To select the line inputs, set HP/$\overline{LINE}$ pin tied to low level
- To enable the headphone inputs, set HP/ $\overline{LINE}$ pin tied to high level

Refer to the application circuit, the voltage divider of 100kΩ and 1kΩ sets the voltage at the HP/$\overline{LINE}$ pin to be approximately 50mV when there are no headphones plugged into the system. This logic low voltage at the HP/$\overline{LINE}$ pin enables the APA2030 and places it LINE input mode operation.

When a set of headphones is plugged into the system, the contact pin of the headphone jack is disconnected from the signal pin, interrupting the voltage divider set up by resistors 100kΩ. Resistor 100kΩ then pulls-up the HP/$\overline{LINE}$ pin, enabling the headphone input function.

Differential Input Operation

APA2030/1 can accepted the differential input signal, and it's can improve the CMRR (Common Mode Rejection ratio). For example: when apply differential input signals to APA2031, connect positive input signals to the IN+ (LIN+ and RIN+) of APA2031 and negative input signals to the IN- (LIN- and RIN-) of APA2031. When input signals are single-end, just connect IN+ (LIN+ and RIN+) to ground via a capacitor.

Input Resistance, Ri

The APA2030/1 provides four gain setting decided by GAIN0 and GAIN1 input ins in Differential mode and it become 4.1dB fixed gain when SE mode is selected (for APA2030). In table 1,internal resistors Ri and Rf according to BTL operation set the gain for each audio input of the APA2030/1.

GAIN0	GAIN1	Ri	Rf	SE/$\overline{BTL}$	Av
0	0	90KΩ	90KΩ	0	6dB
0	1	69KΩ	111KΩ	0	10dB
1	0	42KΩ	138KΩ	0	15.6dB
1	1	25.7KΩ	154.3KΩ	0	21.6dB
X	X	69KΩ	111KΩ	1	4.1dB

Table 1: The close loop gain setting resistance Ri/Rf

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. The input resistance has wide variation (+/-10%) caused by manufacture.

Input Capacitor, Ci

In the typical application an input capacitor, Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance Ri form a high-pass filter with the corner frequency determined in the follow equation:

Application Descriptions

$$f_C(\text{highpass}) = \frac{1}{2\pi Rimin \times Ci} \quad (2)$$

The value of Ci is important to consider as it directly affects the low frequency performance of the circuit. Consider the example where Ri is 90kΩ when 6dB gain is setting and the specification calls for a flat bass response down to 40Hz . Equation is reconfigured as follow:

$$Ci = \frac{1}{2\pi Rifc} \quad (3)$$

Consider to input resistance variation, the Ci is 0.04μF so one would likely choose a value in the range of 0.1μF to 1.0μF.

A further consideration for this capacitor is the leakage path from the input source through the input network (Ri+Rf, Ci) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level there is held at $V_{DD}/2$, which is likely higher that the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, Cbypass

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection.

The capacitor location on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger half supply bypass capacitor is improved PSRR due to increased half-supply stability. Typical applications employ a 5V regulator with 1.0μF and a 0.1μF bypass capacitors which aid in supply filtering. This does not eliminate the need for bypassing the supply nodes of the APA2030/1. The selection of bypass capacitors, especially Cb, is thus dependent upon desired PSRR requirements, click and pop performance.

To avoid start-up pop noise occurred, the bypass voltage should be rise slower then the input bias voltage and the relationship shown in equation should be maintained.

$$\frac{1}{Cbypass \times 125k\Omega} << \frac{1}{Ci \times 180k\Omega} \quad (4)$$

The capacitor is fed from a 125kΩ source inside the amplifier. Bypass capacitor, Cb, values of 3.3μF to 10μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

The bypass capacitance also effect to the start up time. It is determined in the follow equation:

$$Tstart\ up = 5x(Cbypass x 125k\Omega) \quad (5)$$

Output Coupling Capacitor, Cc (for APA2030 only)

In the typical single-supply SE configuration, an output coupling capacitor (Cc) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation.

$$fc(\text{highpass}) = \frac{1}{2\pi R_L C_C} \quad (6)$$

For example, a 330μF capacitor with an 8Ω speaker would attenuate low frequencies below 60.6Hz. The main disadvantage, from a performance standpoint, is the load impedance is typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load.

Power Supply Decoupling, Cs

The APA2030/1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible.

Application Descriptions

Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker.
The optimum decoupling is achieved by using two different type capacitors that target on different type of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance(ESR) ceramic capacitor, typically 0.1μF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10μF or greater placed near the audio power amplifier is recommended.

Shutdown Function

In order to reduce power consumption while not in use, the APA2030/1 contains a shutdown pin to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the SHUTDOWN pin. The trigger point between a logic high and logic low level is typically 2.0V. It is best to switch between ground and the supply V_{DD} to provide maximum device performance.

By switching the $\overline{\text{SHUTDOWN}}$ pin to low, the amplifier enters a low-current state, I_{DD}<50μA. APA2030 is in shutdown mode, except PC-BEEP detect circuit. On normal operating, SHUTDOWN pin pull to high level to keeping the IC out of the shutdown mode. The $\overline{\text{SHUTDOWN}}$ pin should be tied to a definite voltage to avoid unwanted state changes.

PC-BEEP Detection (for APA2030 only)

APA2030 integrates a PCBEEP detect circuit for NOTEBOOK PC used. When PC-BEEP signal drive to PCBEEP input pin, and PCBEEP mode is active. APA2030 will force to BTL mode and the internal gain fixed as -10dB. The PCBEEP signal becomes the amplifier input signal and play on the speaker without coupling capacitor. If the amplifier in the shutdown mode, it will out of shutdown mode whenever PCBEEP mode enable. The APA2030 will return to previous setting when it is out of PC-BEEP mode.

The input impedance is 100kΩ on PCBEEP input pin.

Optimizing Depop Circuitry

Circuitry has been included in the APA2030/1 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the click and pop circuitry. The value of Ci will also affect turn-on pops. (Refer to Effective Bypass Capacitance) The bypass voltage rise up should be slower than input bias voltage. Although the bypass pin current source cannot be modified, the size of Cb can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of Cb, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of Cb and the turn-on time.

In a SE(for APA2030) configuration, the output coupling capacitor, C_C, is of particular concern. This capacitor discharges through the internal 10kΩ resistors. Depending on the size of C_C, the time constant can be relatively large. To reduce transients in SE mode, an external 1kΩ resistor can be placed in parallel with the internal 10kΩ resistor. The tradeoff for using this resistor is an increase in quiescent current.

In the most cases, choosing a small value of Ci in the range of 0.33μF to 1μF, Cb being equal to 0.47μF and an external 1kΩ resistor should be placed in parallel with the internal 10kΩ resistor should produce a virtually clickless and popless turn-on.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. So it is advantageous to use low-gain configurations.

BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. The following equations are the basis for calculating amplifier efficiency.

Application Descriptions

$$\text{Efficiency} = \frac{P_O}{P_{SUP}} \quad (7)$$

Where:

$$P_O = \frac{V_O rms \times V_O rms}{R_L} = \frac{V_P \times V_P}{2R_L}$$

$$V_O rms = \frac{V_P}{\sqrt{2}} \quad (8)$$

$$Psup = V_{DD} * I_{DD}{}^{AVG} = \frac{2V_P}{\pi R_L}$$

Efficiency of a BTL configuration:

$$\frac{P_O}{P_{SUP}} = \left(\frac{V_P \times V_P}{2R_L}\right) / \left(V_{DD} \times \frac{2V_P}{\pi R_L}\right) = \frac{\pi V_P}{4V_{DD}} \quad (10)$$

Table 2 calculates efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1W audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 3W.

Po (W)	Efficiency (%)	I_{DD}(A)	V_{PP}(V)	P_D (W)
0.25	31.25	0.16	2.00	0.55
0.50	47.62	0.21	2.83	0.55
1.00	66.67	0.30	4.00	0.5
1.25	78.13	0.32	4.47	0.35

**High peak voltages cause the THD to increase.

Table 2. Efficiency Vs Output Power in 5V/8Ω BTL Systems

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage whenpossible. Note that in equation, V_{DD} is in the dominator. This indicates that as V_{DD} goes down,efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

Power Dissipation

Whether the power amplifier is operated in BTL or SE modes, power dissipation is a major concern. In equation11 states the maximum power dissipation point for a SE mode operating at a given supply voltage and driving a specified load.

$$\text{SE mode : } P_{D,MAX} = \frac{V_{DD}^2}{2\pi^2 R_L} \quad (11)$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL mode : } P_{D,MAX} = \frac{4V_{DD}^2}{2\pi^2 R_L} \quad (12)$$

Since the APA2030/1 is a dual channel power amplifier, the maximum internal power dissipation is 2 times that both of equations depending on the mode of operation. Even with this substantial increase in power dissipation, the APA2030/1 does not require extra heatsink. The power dissipation from equation12, assuming a 5V-power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation13:

$$P_{D,MAX} = \frac{T_{J.MAX} - T_A}{\theta_{JA}} \quad (13)$$

For TSSOP-24 (APA2030) and TSSOP-20 (APA2031) package with and without thermal pad, the thermal resistance (θ_{JA}) is equal to 45°C/W and 48°C/W, respectively.

Since the maximum junction temperature ($T_{J,MAX}$) of APA2030/1 is 150°C and the ambient temperature (T_A) is defined by the power system design, the maximum

Application Descriptions

power dissipation which the IC package is able to handle can be obtained from equation13. Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the supply voltage (V_{DD}) must bedecreased, the load impedance (R_L) must be increased or the ambient temperature should be reduced.

Thermal Pad Considerations

The thermal pad must be connected to ground. The package with thermal pad of the APA2030/1 requires special attention on thermal design. If the thermal design issues are not properly addressed, the APA2030/1 4Ω will go into thermal shutdown when driving a 4Ω load.

The thermal pad on the bottom of the APA2030/1 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 13 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane. For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the APA2030/1 junction temperature below the thermal shutdown temperature (150°C).

In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.

Thermal Considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions.

To calculate maximum ambient temperatures, first consideration is that the numbers from the **Power Dissipation vs. Output Power** graphs (page17) are per channel values, so the dissipation of the IC heat needs to be doubled for two-channel operation. Given θ_{JA}, the maximum allowable junction temperature ($T_{J,MAX}$), and the total internal dissipation (P_D), the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the APA2030/1 is 150°C. The internal dissipation figures are taken from the **Power Dissipation vs. Output Power** graphs. (Page17)

$$T_{A,Max} = T_{J,Max} - \theta_{\vartheta A} P_D \quad (14)$$

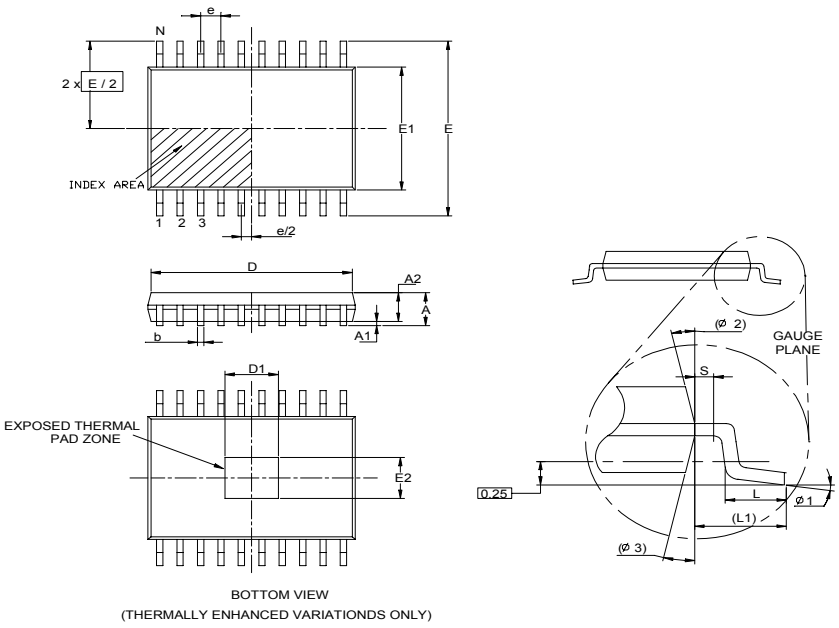
150 - 45(0.8*2) = 78°C (TSSOP-P24)

150 - 48(0.8*2) = 73.2°C (TSSOP-P20)

The APA2030/1 is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150°C to prevent damaging the IC.

Packaging Information

TSSOP/ TSSOP-P (Reference JEDEC Registration MO-153)

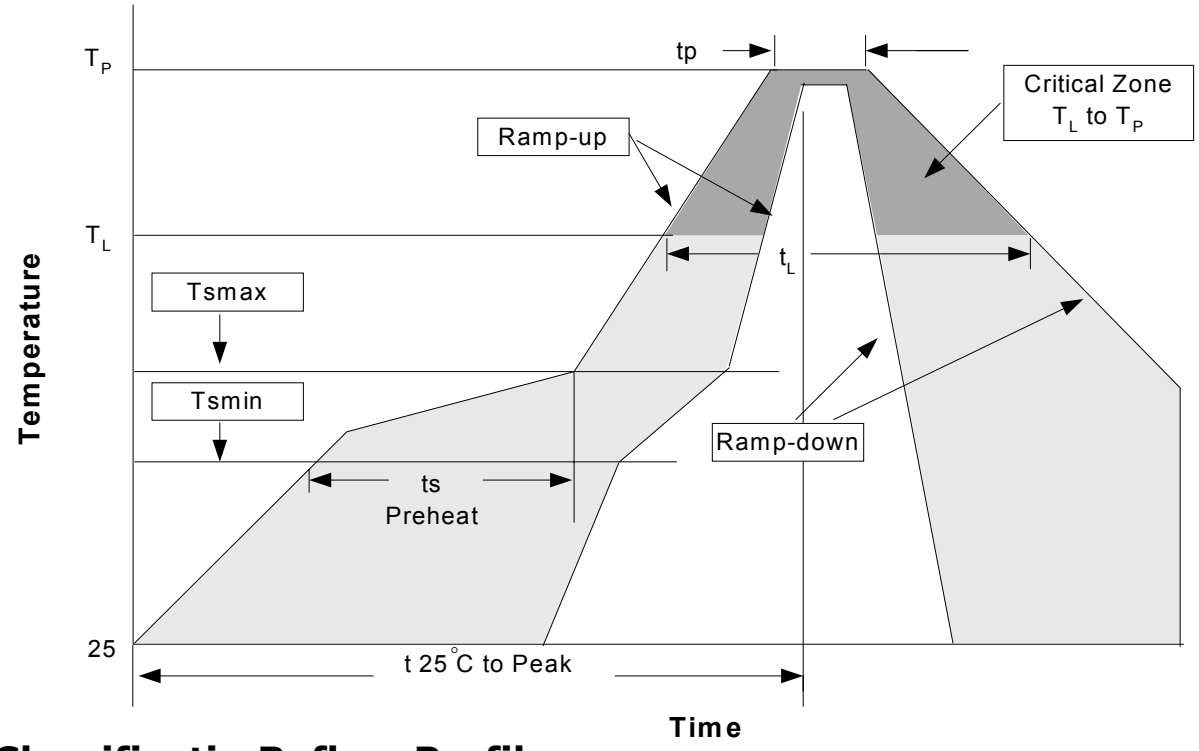


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A		1.2		0.047
A1	0.00	0.15	0.000	0.006
A2	0.80	1.05	0.031	0.041
D	6.4 (N=20PIN) 7.7 (N=24PIN) 9.6 (N=28PIN)	6.6 (N=20PIN) 7.9 (N=24PIN) 9.8 (N=28PIN)	0.252 (N=20PIN) 0.303 (N=24PIN) 0.378 (N=28PIN)	0.260 (N=20PIN) 0.311 (N=24PIN) 0.386 (N=28PIN)
D1	4.2 BSC (N=20PIN) 4.7 BSC (N=24PIN) 3.8 BSC (N=28PIN)		0.165 BSC (N=20PIN) 0.188 BSC (N=24PIN) 0.150 BSC (N=28PIN)	
e	0.65 BSC		0.026 BSC	
E	6.40 BSC		0.252 BSC	
E1	4.30	4.50	0.169	0.177
E2	3.0 BSC (N=20PIN) 3.2 BSC (N=24PIN) 2.8 BSC (N=28PIN)		0.118 BSC (N=20PIN) 0.127 BSC (N=24PIN) 0.110 BSC (N=28PIN)	
L	0.45	0.75	0.018	0.030
L1	1.0 REF		0.039REF	
R	0.09		0.004	
R1	0.09		0.004	
S	0.2		0.008	
ϕ1	0°	8°	0°	8°
ϕ2	12° REF		12° REF	
ϕ3	12° REF		12° REF	

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classificatin Reflow Profiles

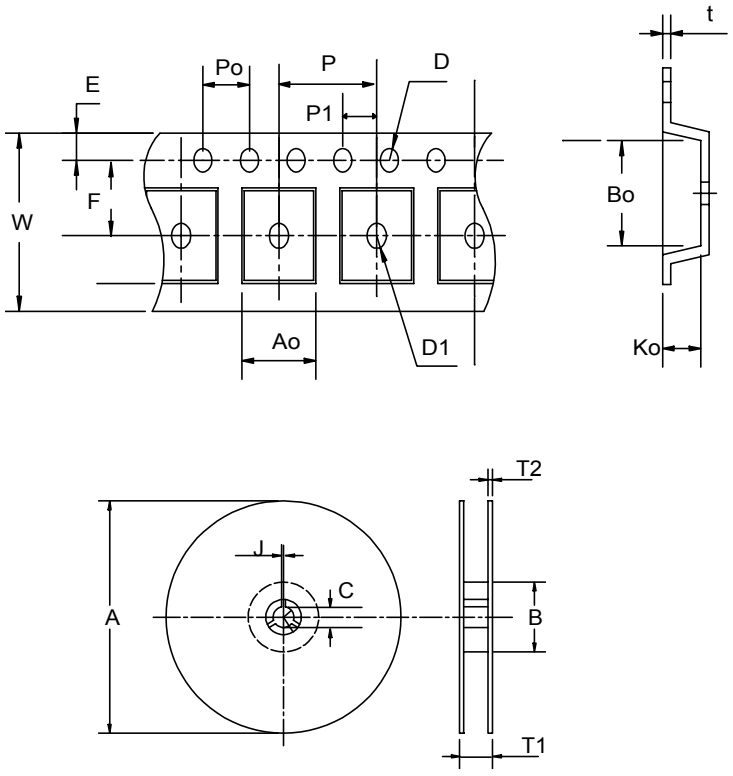
Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (T_L to T_P)	3°C/second max.		3°C/second max.	
Preheat - Temperature Min (Tsmin) - Temperature Mix (Tsmax) - Time (min to max)(ts)	100°C 150°C 60-120 seconds		150°C 200°C 60-180 seconds	
Tsmax to T_L - Ramp-up Rate			3°C/second max	
Tsmax to T_L - Temperature(T_L) - Time (t_L)	183°C 60-150 seconds		217°C 60-150 seconds	
Peak Temperature(Tp)	225 +0/-5°C	240 +0/-5°C	245 +0/-5°C	250 +0/-5°C
Time within 5°C of actual Peak Temperature(tp)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

Note: All temperatures refer to topside of the package. Measured on the body surface.

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Carrier Tape & Reel Dimensions



Application	A	B	C	J	T1	T2	W	P	E
TSSOP- 24	330 ±1	100 ref	13 ±0.5	2 ±0.5	16.4 ±0.2	2 ±0.2	16 ±0.3	12 ±0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	7.5 ±0.1	1.5 +0.1	1.5 min	4.0 ±0.1	2.0 ±0.1	6.9 ±0.1	8.3 ±0.1	1.5 ±0.1	0.3±0.05

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
TSSOP- 24	16	21.3	2000

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