

## X-band GaInP HBT High Power Amplifier

### GaAs Monolithic Microwave IC

*preliminary*

#### Description

The **CHA7010** is a monolithic two stage GaAs high power amplifier designed for X band applications.

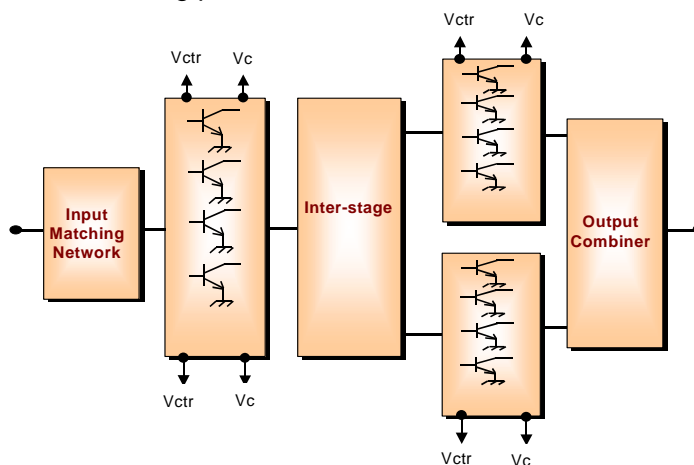
This device is manufactured using a GaInP HBT process, including, via holes through the substrate and air bridges. A nitride layer protects the transistors and the passive components. Special heat removal techniques are implemented to guarantee high reliability.

To simplify the assembly process;

- the backside of the chip is both RF and DC grounded
- bond pads and back side are gold plated for compatibility with eutectic die attach method and thermo-sonic or thermo-compression bonding process.

#### Main Features

- 10W output power
- High gain : > 18dB @ 10GHz
- High PAE : > 35% @ 10GHz
- On-chip bias control
- Linear collector current control
- High impedance interface for pulse mode
- Temperature compensated
- Chip size: 4.74 x 4.36 x 0.1 mm



#### Main Characteristics

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_op	Operating frequency range	8.4	9.4	10.4	GHz
P_sat	Saturated output power		10		W
P_1dBc	Output power @ 1dBc		8		W
G_lin	Linear gain		18		dB

ESD Protections : Electrostatic discharge sensitive device observe handling precautions !

## Electrical Characteristics

*preliminary*

Tamb = 25°C, Vc=9V, Vctr=5.5V, Pulse width=80µs, Duty cycle = 30%

Symbol	Parameter	Min	Typ	Max	Unit
F_op	Operating frequency	8.4	9.4	10.4	GHz
G_lin_1	Linear gain (8.4 to 9.4GHz)	14	16		dB
G_lin_2	Linear gain (9.4 to 10.4GHz)	16	18		dB
G_lin_T	Linear gain variation versus temperature		-0.035		dB/°C
RL_in	Input Return Loss	8	12		dB
RL_out	Output Return Loss	6	12		dB
P_sat_1	Saturated output power (8.4 to 9.8GHz)	39	40		dBm
P_sat_2	Saturated output power (9.8 to 10.4GHz)	38	39		dBm
P_sat_T	Saturated output power variation versus temperature		-0.01		dB/°C
P_1dBc_1	Output power @ 1dBc (8.4 to 9.8GHz)	38	39		dBm
P_1dBc_2	Output power @ 1dBc (9.8 to 10.4GHz)	37	38		dBm
PAE_sat	Power Added Efficiency in saturation	30	35		%
PAE_1dBc	Power Added Efficiency @ 1dBc	27	32		%
Vc	Power supply voltage		9		V
Ic	Power supply quiescent current (1)		2.4		A
Vctr	Collector current control voltage		5.5		V
Zctr	Vctr input port impedance (2)		350		Ohm
Top	Operating temperature range (3)	-30		+80	°C

- (1) This parameter is fixed by Vctr
- (2) This value corresponds to the 4 ports in parallel (Pin 4, 9, 17, 22)
- (3) The reference is the back-side of the chip

## Absolute Maximum Ratings (1)

Tamb = 25°C

Symbol	Parameter	Values	Unit
Cmp	Compression level	6	dB
Vc	Power supply voltage	10	V
Ic	Power supply quiescent current	2.8	A
Ic_sat	Power supply current in saturation	3.5	A
Vctr	Collector current control voltage	6.5	V
Tstg	Storage temperature range	-55 to +125	°C

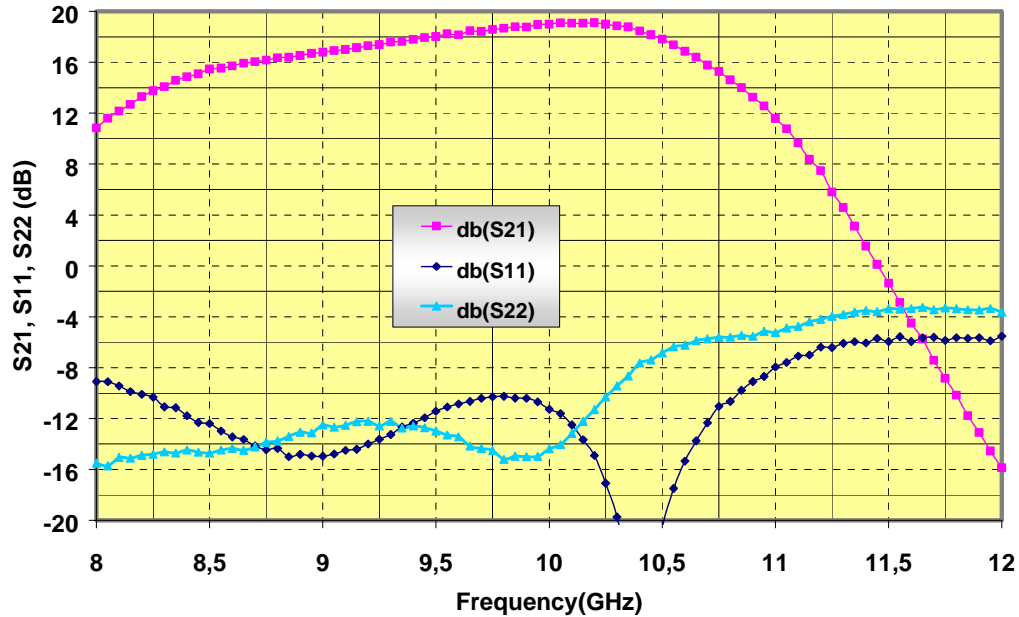
- (1) Operation of this device above any one of these parameters may cause permanent damage.

## Typical measured characteristics

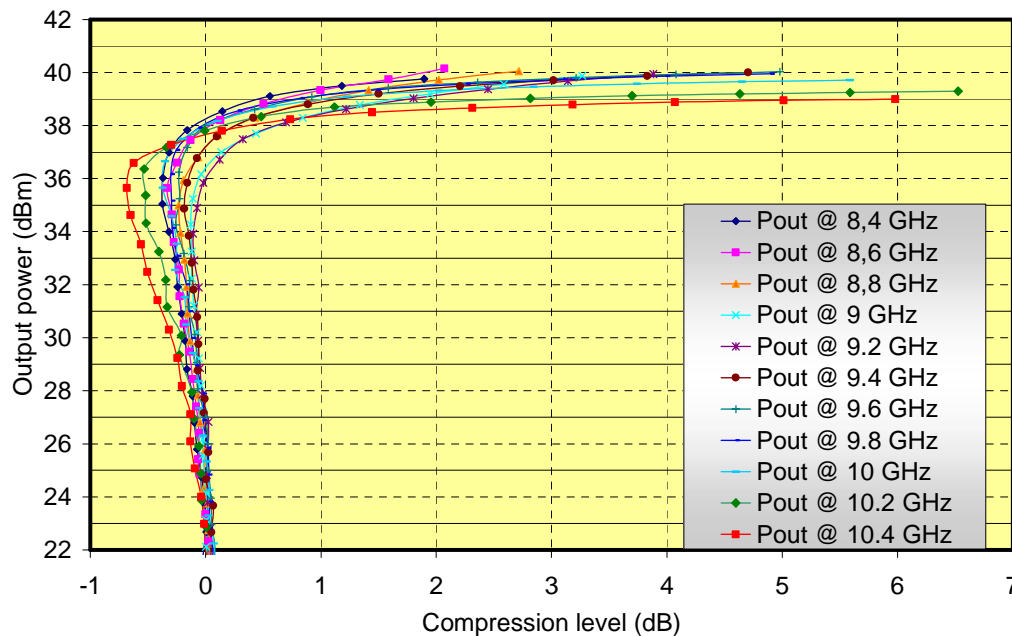
*preliminary*

Measurements in test fixture :

Tamb=25°C, Vc=9V, Vctr=5.5V, Pulse width=80µs , Duty cycle = 30%



**S-parameters**



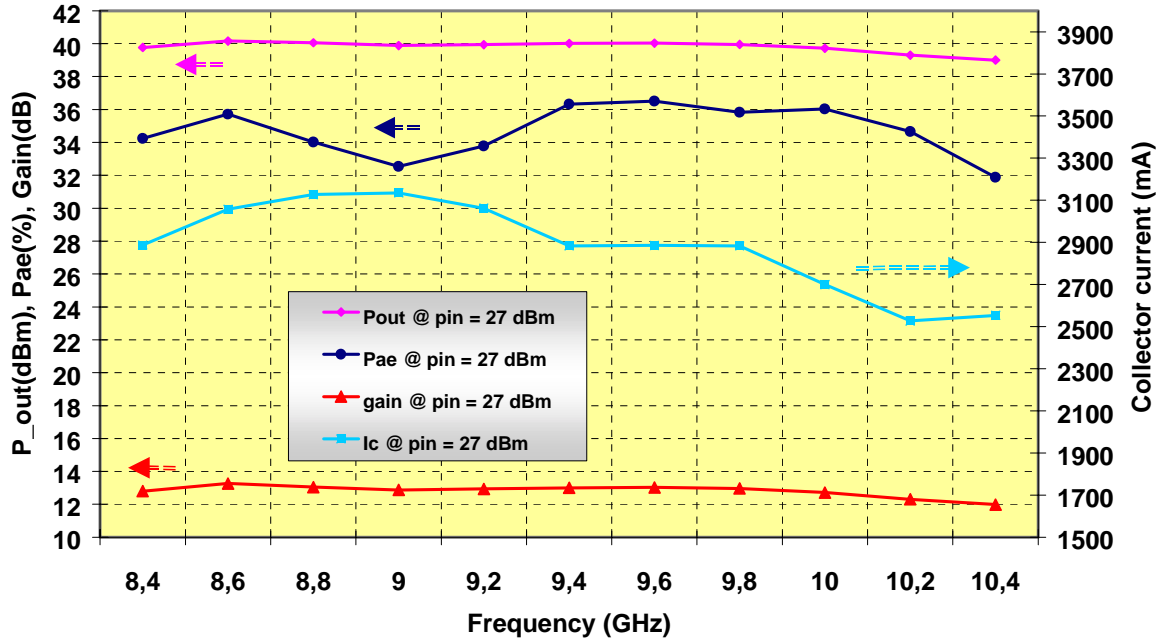
**Output power versus compression level : F= 8.4 to 10.4GHz**

## Typical measured characteristics

*preliminary*

Measurements in test fixture :

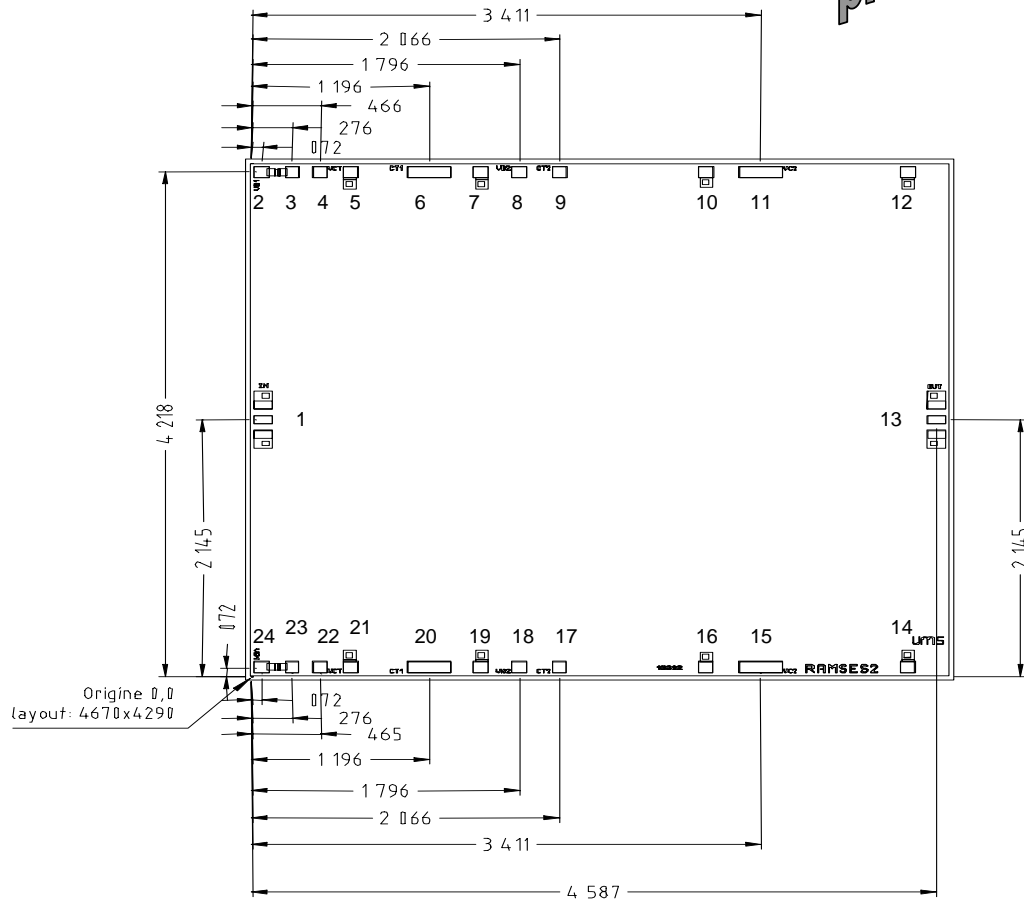
Tamb=25°C, Vc=9V, Vctr=5.5V, Pulse width=80µs , Duty cycle = 30%



**Saturated output power, PAE, Gain and collector current versus frequency**

## Dimensions and Pad allocation

*preliminary*



Unit =  $\mu\text{m}$

External chip size (including saw streets) = 4740 x 4360 +/- 35

Chip thickness = 100 +/- 10

HF pads (1, 13) = 118 x 68

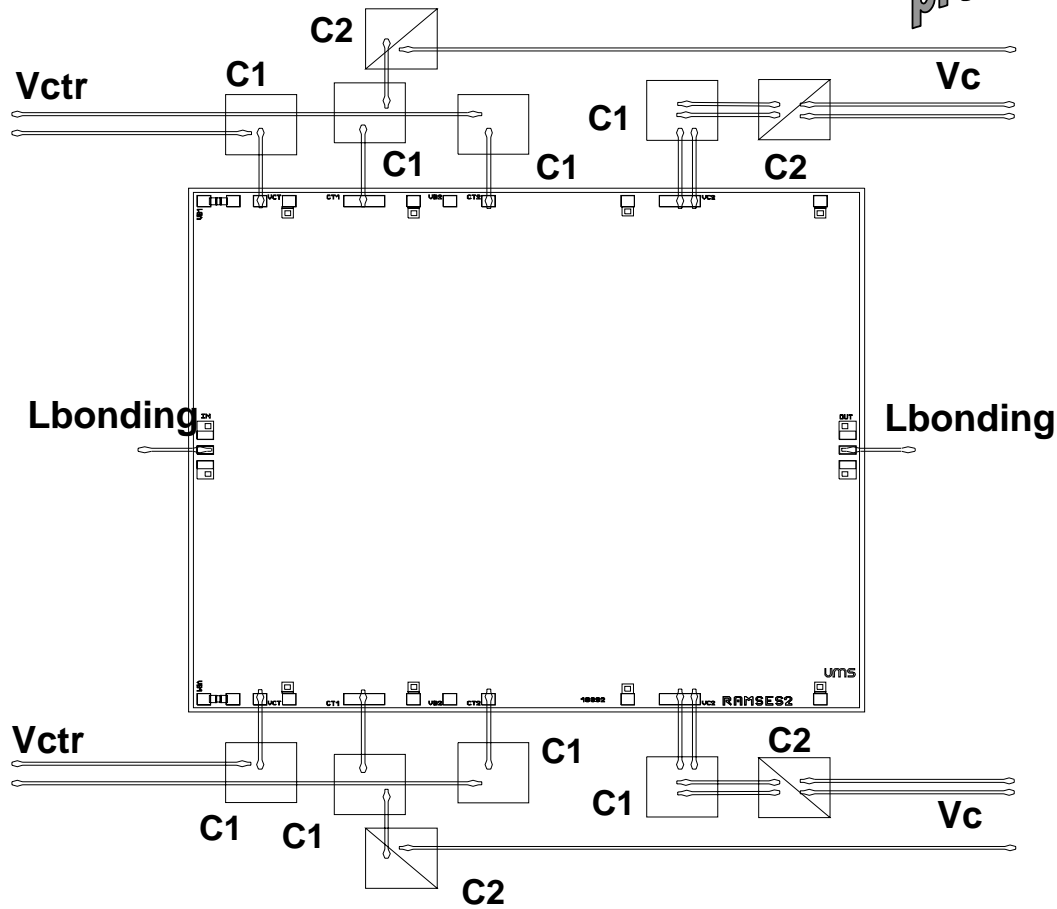
DC pads (4, 9, 17, 22) = 96 x 96

DC pads (6, 11, 15, 20) = 288 x 96

Pin number	Pin name	Description
1	IN	Input RF port
2, 3, 8, 18, 23, 24		NC
4, 9, 17, 22	Vctr	Collector control current port
5, 7, 10, 12, 14, 19, 16, 21	GND	Ground (NC)
6, 11, 15, 20	Vc	Power supply voltage
13	OUT	Output RF port

Assembly recommendations

*preliminary*



For thermal and electrical considerations, the chip should be brazed on a metal base plate.  
 The RF, DC and modulation port inter-connections should be done according to the following table:

Port	Connection	External capacitor
IN (1)	Inductance (Lbonding) = 0.4nH	
OUT (13)	Inductance (Lbonding) = 0.4nH	
Vc (6, 11, 15, 20))	Inductance ~ 1nH	C1 ~ 100pF C2 ~ 10nF
Vctr (4, 9, 17, 22)	Inductance ~ 1nH	C1 ~ 100pF

*preliminary*

## Ordering Information

Chip form : CHA7010-99F/00

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