

Features

- 12-Bit Linearity 0.01%
- Pretrimmed Gain
- Low Gain and Linearity Tempcos
- Full Temperature Range Operation
- Full Input Static Protection
- TTL/CMOS Compatible
- +5V to +15V Supply Range
- 20mW Low Power Dissipation
- Current Settling Time 1 μ s to 0.01% of FSR
- Four Quadrant Multiplication

Description

The AD7541 is a monolithic, low cost, high performance, 12-bit accurate, multiplying digital-to-analog converter (DAC).

Intersil' wafer level laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity with TTL/CMOS compatible operation.

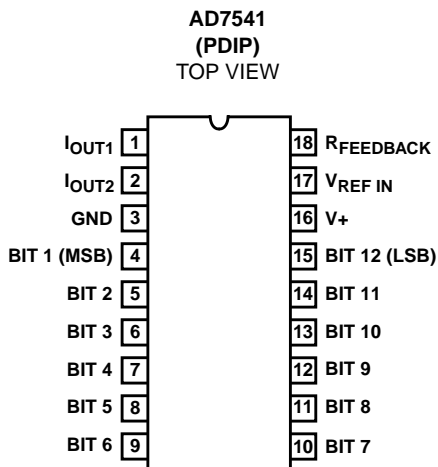
Special tabbed-resistor geometries (improving time stability), full input protection from damage due to static discharge by diode clamps to V+ and ground, large I_{OUT1} and I_{OUT2} bus lines (improving superposition errors) are some of the features offered by Intersil AD7541.

Pin compatible with AD7521, this DAC provides accurate four quadrant multiplication over the full military temperature range.

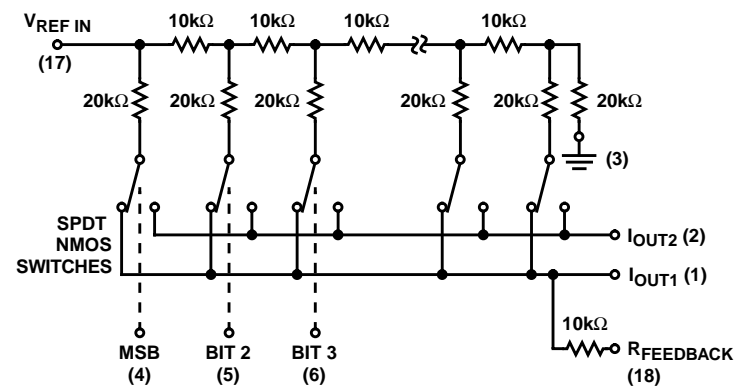
Ordering Information

| PART NUMBER | NONLINEARITY | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|-------------|-------------------------------------|------------------|------------|----------|
| AD7541JN | 0.02% (11-Bit) | 0 to 70 | 18 Ld PDIP | E18.3 |
| AD7541KN | 0.01% (12-Bit) | 0 to 70 | 18 Ld PDIP | E18.3 |
| AD7541LN | 0.01% (12-Bit) Guaranteed Monotonic | 0 to 70 | 18 Ld PDIP | E18.3 |

Pinout



Functional Block Diagram



NOTE: Switches shown for digital inputs "High".

AD7541

Absolute Maximum Ratings

| | |
|-----------------------------|--------------|
| Supply Voltage (V+ to GND) | +17V |
| V _{REF} | ±25V |
| Digital Input Voltage Range | V+ to GND |
| Output Voltage Compliance | -100mV to V+ |

Thermal Information

| | |
|--|------------------------|
| Thermal Resistance (Typical, Note 1) | θ _{JA} (°C/W) |
| PDIP Package | 90 |
| Maximum Junction Temperature | 150°C |
| Maximum Storage Temperature | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C |

Operating Conditions

| | |
|---------------------|--------------|
| Temperature Range | |
| JN, KN, LN Versions | .0°C to 70°C |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V+ = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V, T_A = 25°C, Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | T _A = 25°C | | | T _A MIN-MAX | | UNITS | |
|--|--|--|-------------------|--------|------------------------|-------|-------------------|----------|
| | | MIN | TYP | MAX | MIN | MAX | | |
| SYSTEM PERFORMANCE | | | | | | | | |
| Resolution | | 12 | - | - | 12 | - | Bits | |
| Nonlinearity | A, S, J | -10V ≤ V _{REF} ≤ +10V V _{OUT1} = V _{OUT2} = 0V See Figure 3 (Note 5) | - | - | ±0.024 | - | ±0.024 | % of FSR |
| | B, T, K | | - | - | ±0.012 | - | ±0.012 | % of FSR |
| | L | | - | - | ±0.012 | - | ±0.012 | % of FSR |
| Monotonicity | | Guaranteed | | | | | | |
| Gain Error | -10V ≤ V _{REF} ≤ +10V (Note 5) | - | - | ±0.3 | - | ±0.4 | % of FSR | |
| Output Leakage Current (Either Output) | V _{OUT1} = V _{OUT2} = 0 | - | - | ±50 | - | ±200 | nA | |
| DYNAMIC CHARACTERISTICS | | | | | | | | |
| Power Supply Rejection | V+ = 14.5V to 15.5V See Figure 5 (Note 5) | - | - | ±0.005 | - | ±0.01 | % of FSR/% of ΔV+ | |
| Output Current Settling Time | To 0.1% of FSR See Figure 9 (Note 6) | - | - | 1 | - | 1 | μs | |
| Feedthrough Error | V _{REF} = 20V _{p-p} , 10kHz All Digital Inputs Low See Figure 8 (Note 6) | - | - | 1 | - | 1 | mV _{p-p} | |
| REFERENCE INPUTS | | | | | | | | |
| Input Resistance | All Digital Inputs High I _{OUT1} at Ground | 5 | 10 | 20 | 5 | 20 | kΩ | |
| ANALOG OUTPUT | | | | | | | | |
| Voltage Compliance | Both Outputs, See Maximum Ratings (Note 7) | -100mV to V+ | | | | | | |
| Output Capacitance | C _{OUT1} | All Digital Inputs High See Figure 7 (Note 6) | - | - | 200 | - | 200 | pF |
| | | | C _{OUT2} | - | - | 60 | - | 60 |
| | C _{OUT1} | All Digital Inputs Low See Figure 7 (Note 6) | - | - | 60 | - | 60 | pF |
| | | | C _{OUT2} | - | - | 200 | - | 200 |
| Output Noise (Both Outputs) | See Figure 6 | Equivalent to 10kΩ Johnson Noise | | | | | | |
| DIGITAL INPUTS | | | | | | | | |
| Low State Threshold, V _{IL} | (Notes 2, 6) | - | - | 0.8 | - | 0.8 | V | |
| High State Threshold, V _{IH} | | 2.4 | - | - | 2.4 | - | V | |

Electrical Specifications $V_+ = +15V$, $V_{REF} = +10V$, $V_{OUT1} = V_{OUT2} = 0V$, $T_A = 25^\circ C$, Unless Otherwise Specified (Continued)

| PARAMETER | TEST CONDITIONS | $T_A = 25^\circ C$ | | | T_A MIN-MAX | | UNITS |
|-------------------------------------|---|----------------------|-----|---------|---------------|---------|---------|
| | | MIN | TYP | MAX | MIN | MAX | |
| Input Current | $V_{IN} = 0V$ or V_+ (Note 6) | - | - | ± 1 | - | ± 1 | μA |
| Input Coding | See Tables 1 and 2 (Note 6) | Binary/Offset Binary | | | | | |
| Input Capacitance | (Note 6) | - | - | 8 | - | 8 | pF |
| POWER SUPPLY CHARACTERISTICS | | | | | | | |
| Power Supply Voltage Range | Accuracy Is Not Guaranteed Over This Range | +5 to +16 | | | | | V |
| I+ | All Digital Inputs High or Low (Excluding Ladder Network) | - | - | 2.0 | - | 2.5 | mA |
| Total Power Dissipation | (Including Ladder Network) | - | 20 | - | - | - | mW |

NOTES:

- The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
- Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and $R_{FEEDBACK}$.
- Full scale range (FSR) is 10V for unipolar and $\pm 10V$ for bipolar modes.
- Using internal feedback resistor, $R_{FEEDBACK}$.
- Guaranteed by design or characterization and not production tested.
- Accuracy not guaranteed unless outputs at ground potential.

Definition of Terms

Nonlinearity: Error contributed by deviation of the DAC transfer function from a "best fit straight line" function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

Resolution: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $LSB = (V_{REF})/2^{N-1}$. A bipolar converter of n bits has a resolution of $LSB = (V_{REF})/2^{(N-1)}$. Resolution in no way implies linearity.

Settling Time: Time required for the output function of the DAC to settle to within $1/2$ LSB for a given digital input stimulus, i.e., 0 to Full Scale.

Gain Error: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

Feedthrough Error: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

Output Capacitance: Capacitance from I_{OUT1} , and I_{OUT2} terminals to ground.

Output Leakage Current: Current which appears on I_{OUT1} , terminal when all digital inputs are LOW or on I_{OUT2} terminal when all inputs are HIGH.

Detailed Description

The AD7541 is a 12-bit, monolithic, multiplying D/A converter. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit. CMOS level shifters provide low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications. A simplified equivalent circuit of the DAC is shown on page 1, (Functional Diagram). The NMOS SPDT switches steer the ladder leg currents between I_{OUT1} and I_{OUT2} buses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code. Converter errors are further eliminated by using wider metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

Each circuit is laser-trimmed, at the wafer level, to better than 12-bits linearity. For the first four bits of the ladder, special trim-tabbed geometries are used to keep the body of the resistors, carrying the majority of the output current, undisturbed. The resultant time stability of the trimmed circuits is comparable to that of untrimmed units.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to first (Figure 1). This configuration results in TTL/COMS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binary weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistor, resulting in accurate leg currents.

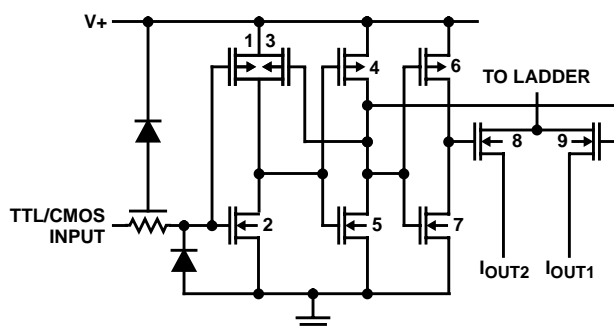


FIGURE 1. CMOS SWITCH

Typical Applications

General Recommendations

Static performance of the AD7541 depends on I_{OUT1} and I_{OUT2} (pin 1 and pin 2) potentials being exactly equal to GND (pin 3).

The output amplifier should be selected to have a low input bias current (typically less than 75nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than $\pm 200\mu\text{V}$).

The bias current compensation resistor in the amplifier's non-inverting input can cause a variable offset. Non-inverting input should be connected to GND with a low resistance wire.

Ground-loops must be avoided by taking all pins going to GND to a common point, using separate connections.

The V+ (pin 18) power supply should have a low noise level and should not have any transients exceeding +17V.

Unused digital inputs must be connected to GND or V_{DD} for proper operation.

A high value resistor ($\sim 1\text{M}\Omega$) can be used to prevent static charge accumulation, when the inputs are open-circuited for any reason.

When gain adjustment is required, low tempco (approximately $50\text{ppm}/^\circ\text{C}$) resistors or trim-pots should be selected.

Unipolar Binary Operation

The circuit configuration for operating the AD7541 in unipolar mode is shown in Figure 2. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1. A Schottky diode (HP5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

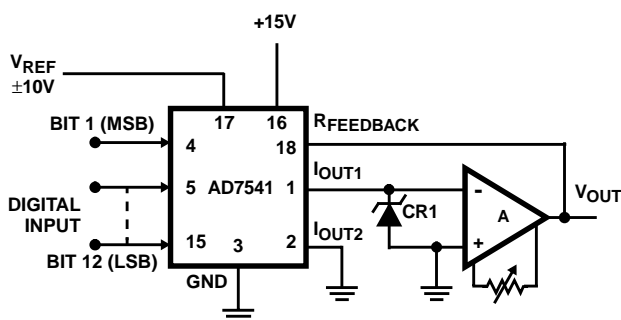


FIGURE 2. UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for $0\text{V} \pm 0.5\text{mV}$ (Max) at V_{OUT} .

Gain Adjustment

1. Connect all digital inputs to V_{DD} .
2. Monitor V_{OUT} for a $-V_{REF}$ ($1\frac{1}{2}^{12}$) reading.
3. To increase V_{OUT} , connect a series resistor, (0Ω to 250Ω), in the I_{OUT1} amplifier feedback loop.
4. To decrease V_{OUT} , connect a series resistor, (0Ω to 250Ω), between the reference voltage and the V_{REF} terminal.

TABLE 1. CODE TABLE - UNIPOLAR BINARY OPERATION

| DIGITAL INPUT | ANALOG OUTPUT |
|---------------|-----------------------------|
| 111111111111 | $-V_{REF} (1 - 1/2^{12})$ |
| 100000000001 | $-V_{REF} (1/2 + 1/2^{12})$ |
| 100000000000 | $-V_{REF}/2$ |
| 011111111111 | $-V_{REF} (1/2 - 1/2^{12})$ |
| 000000000001 | $-V_{REF} (1/2^{12})$ |
| 000000000000 | 0 |

Bipolar (Offset Binary) Operation

The circuit configuration for operating the AD7541 in the bipolar mode is given in Figure 3. Using offset binary digital input codes and positive and negative reference voltage values Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistive divider, from V_{REF} to I_{OUT2} .

Offset Adjustment

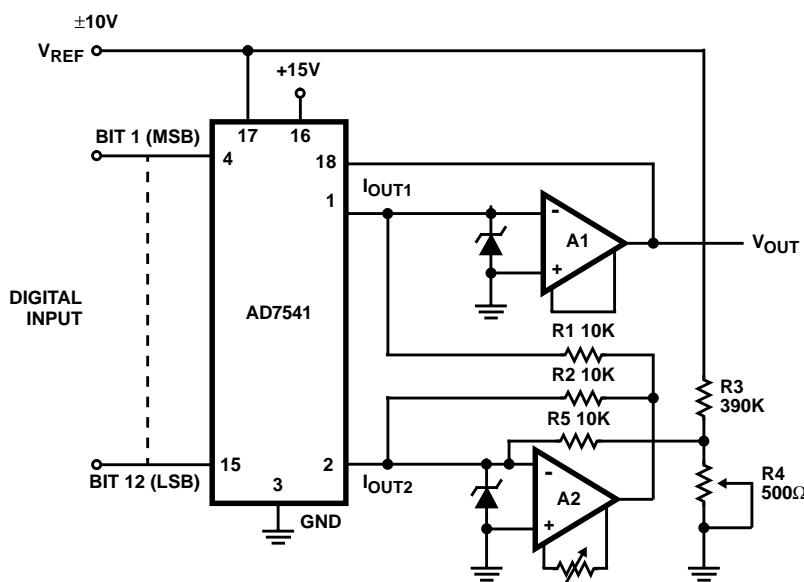
1. Adjust V_{REF} to approximately +10V.
2. Set R4 to zero.
3. Connect all digital inputs to "Logic 1".
4. Adjust I_{OUT1} amplifier offset zero adjust trimpot for $0V \pm 0.1mV$ at I_{OUT2} amplifier output.
5. Connect a short circuit across R2.
6. Connect all digital inputs to "Logic 0".
7. Adjust I_{OUT2} amplifier offset zero adjust trimpot for $0V \pm 0.1mV$ at I_{OUT1} amplifier output.
8. Remove short circuit across R2.
9. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
10. Adjust R4 for $0V \pm 0.2mV$ at V_{OUT} .

Gain Adjustment

1. Connect all digital inputs to V_{DD} .
2. Monitor V_{OUT} for a $-V_{REF} (1 - 1/2^{11})$ volts reading.
3. To increase V_{OUT} , connect a series resistor, (0Ω to 250Ω), in the I_{OUT1} amplifier feedback loop.
4. To decrease V_{OUT} , connect a series resistor, (0Ω to 250Ω), between the reference voltage and the V_{REF} terminal.

TABLE 2. CODE TABLE - BIPOLAR (OFFSET BINARY) OPERATION

| DIGITAL INPUT | ANALOG OUTPUT |
|---------------|---------------------------|
| 111111111111 | $-V_{REF} (1 - 1/2^{11})$ |
| 100000000001 | $-V_{REF} (1/2^{11})$ |
| 100000000000 | 0 |
| 011111111111 | $V_{REF} (1/2^{11})$ |
| 000000000001 | $V_{REF} (1 - 1/2^{11})$ |
| 000000000000 | V_{REF} |



NOTE: R1 and R2 should be 0.01%, low-TCR resistors.

FIGURE 3. BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Test Circuits

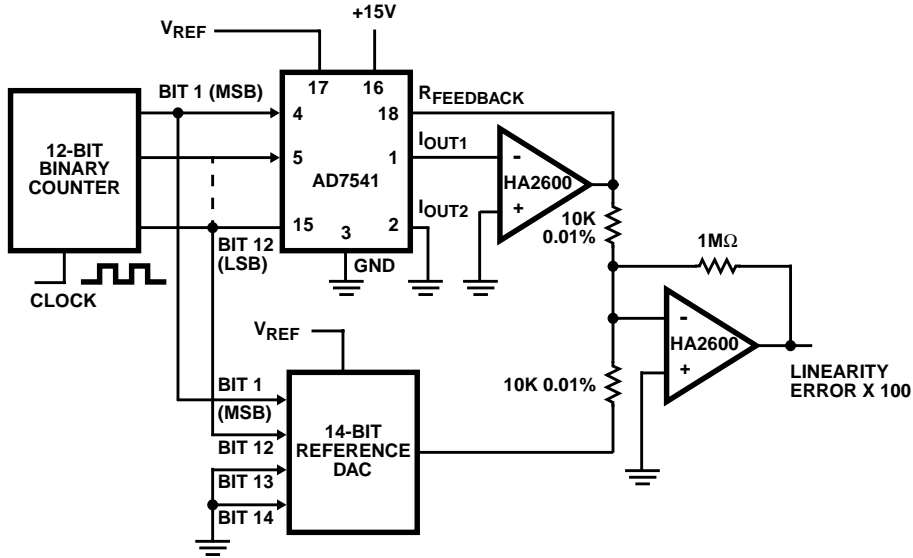


FIGURE 4. NONLINEARITY TEST CIRCUIT

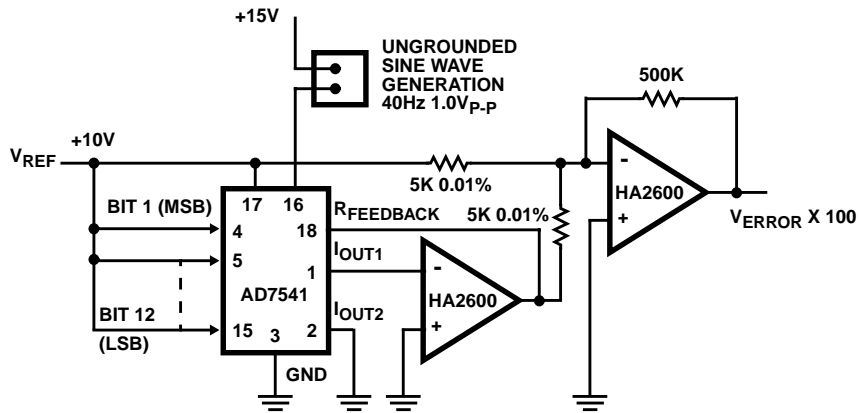


FIGURE 5. POWER SUPPLY REJECTION TEST CIRCUIT

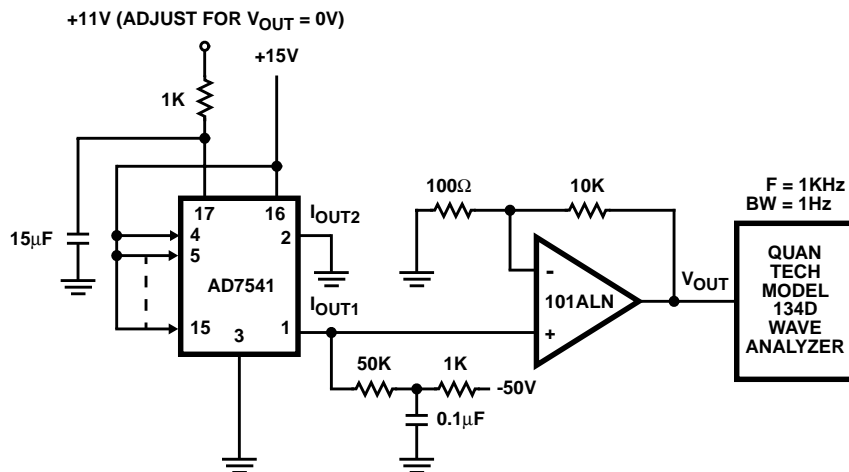


FIGURE 6. NOISE TEST CIRCUIT

Test Circuits (Continued)

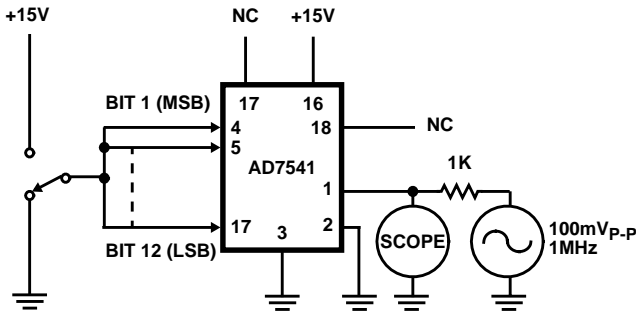


FIGURE 7. OUTPUT CAPACITANCE TEST CIRCUIT

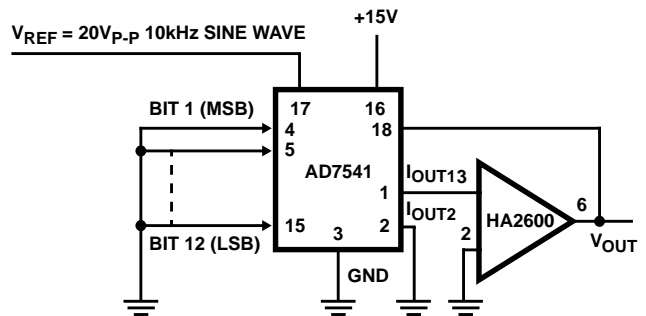


FIGURE 8. FEEDTHROUGH ERROR TEST CIRCUIT

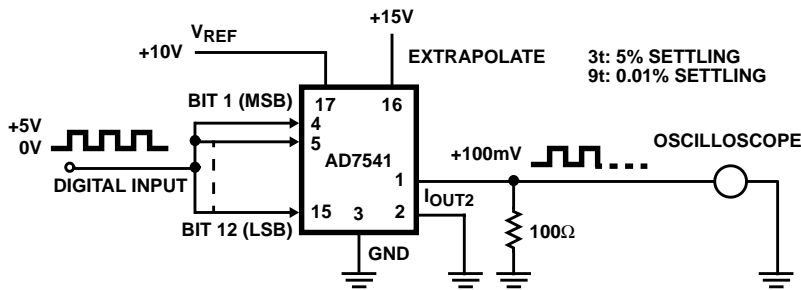


FIGURE 9. OUTPUT CURRENT SETTLING TIME TEST CIRCUIT

Dynamic Performance

The dynamic performance of the DAC, also depends on the output amplifier selection. For low speed or static applications, AC specifications of the amplifier are not very critical. For high-speed applications slew-rate, settling-time, openloop gain and gain/phase-margin specifications of the amplifier should be selected for the desired performance.

The output impedance of the AD7541 looking into I_{OUT1} varies between $10k\Omega$ ($R_{FEEDBACK}$ alone) and $5k\Omega$ ($R_{FEEDBACK}$ in parallel with the ladder resistance).

Similarly the output capacitance varies between the minimum and the maximum values depending on the input

code. These variations necessitate the use of compensation capacitors, when high speed amplifiers are used.

A capacitor in parallel with the feedback resistor (as shown in Figure 10) provides the necessary phase compensation to critically damp the output.

A small capacitor connected to the compensation pin of the amplifier may be required for unstable situations causing oscillations. Careful PC board layout, minimizing parasitic capacitances, is also vital.

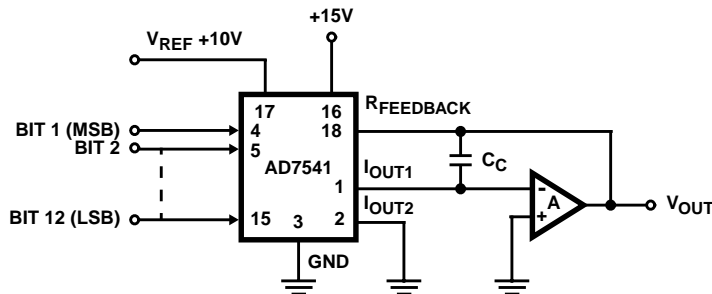


FIGURE 10. GENERAL DAC CIRCUIT WITH COMPENSATION CAPACITOR, C_C

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029