

ERRATA DATA SHEET



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Quality • Performance • Service

T-46-23-15

1 MEG DRAM

(1 MEG PAGE MODE DRAM)

MT4C1024E **1 MEG x 1 BIT DYNAMIC RAM**
MT4C4256E **256K x 4 BIT DYNAMIC RAM**

PIN ASSIGNMENT (TOP VIEW)

FEATURES

- Industry standard x1 or x4 pin-out, functions and packages
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Low power, 5mw standby, 175 mw active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: $\overline{\text{RAS}}$ only, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ and Hidden
- Optional Page Mode access cycle

OPTIONS

- Timing
 - 100ns access
 - 120ns access
 - 150ns access

- Organization
 - 1 MEG x 1
 - 256K x 4

- Packages
 - Plastic DIP
 - Ceramic DIP
 - Plastic ZIP
 - Plastic SOJ

- Order Examples:

1 MEG x 1, 120ns access, in Plastic DIP = MT4C1024E-12

MARKING

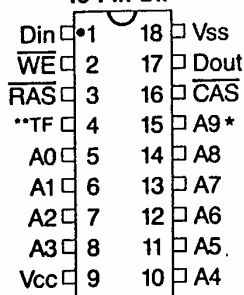
x1,x4
-10
-12
-15

MT4C1024E
MT4C4256E

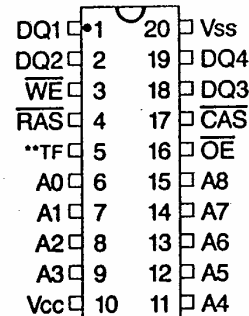
None
C
Z
DJ

*Address not used for $\overline{\text{RAS}}$ only refresh
**TF = Test Function, ground or leave as a no-connect for normal device operation.

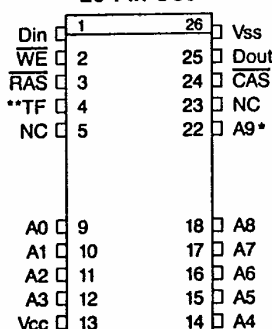
MT4C1024E
18 Pin DIP



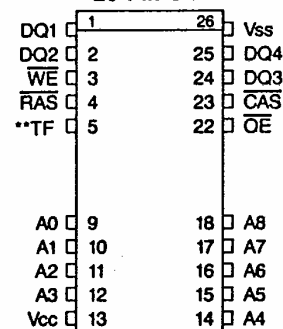
MT4C4256E
20 Pin DIP



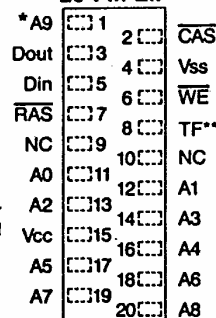
MT4C1024E
20 Pin SOJ



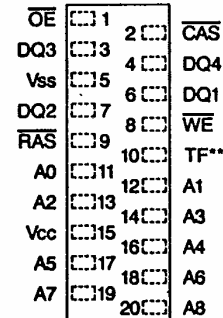
MT4C4256E
20 Pin SOJ



MT4C1024E
20 Pin ZIP



MT4C4256E
20 Pin ZIP



The Micron 1 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacturer's products meeting JEDEC standards. Several parameters are sampled; however, functionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. The success of our memory business depends on the success of your application.

ERRATA DATA SHEET
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C < TA < +70°C, V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	t _{RC}	190		220		260		ns	
Read-Modify-Write cycle time	t _{RWC}	220		255		295		ns	
Page mode cycle time	t _{PC}	75		90		110		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		100		120		150	ns	
Access time from $\overline{\text{CAS}}$	t _{CAC}		50		60		75	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{\text{RAS}}$ pulse width (Page Mode)	t _{RASP}	100	100,000	120	100,000	150	100,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	50		60		75		ns	
$\overline{\text{RAS}}$ precharge time	t _{RP}	80		90		100		ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	50	10,000	60	10,000	75	10,000	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	100		120		150		ns	
$\overline{\text{CAS}}$ precharge time	t _{CPN}	15		20		25		ns	
$\overline{\text{CAS}}$ precharge time (page mode)	t _{CP}	15		20		25		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	t _{RCD}	10	50	15	60	15	75	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	10		10		10		ns	
Row address set-up time	t _{ASR}	5		5		5		ns	
Row address hold time	t _{RAH}	10		15		15		ns	
Column address set-up time	t _{ASC}	5		5		5		ns	
Column address hold time	t _{CAH}	20		20		25		ns	
Column address hold time (referenced to $\overline{\text{RAS}}$)	t _{AR}	60		70		80		ns	
Read command set-up time	t _{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{\text{CAS}}$)	t _{RCH}	0		0		0		ns	
Read command hold time (referenced to $\overline{\text{RAS}}$)	t _{RRH}	0		0		0		ns	
$\overline{\text{CAS}}$ to output in low-Z	t _{CLZ}	5		5		5		ns	
Output buffer turn-off delay	t _{OFF}	0	25	0	25	0	30	ns	
$\overline{\text{WE}}$ command set-up time	t _{WCS}	0		0		0		ns	
Write command hold time	t _{WCH}	20		25		30		ns	
Write command hold time (referenced to $\overline{\text{RAS}}$)	t _{WCR}	70		80		90		ns	
Write command pulse width	t _{WP}	20		25		30		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	25		30		35		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	25		30		35		ns	
Data-in set-up time	t _{DS}	5		5		5		ns	
Data-in hold time	t _{DH}	15		20		25		ns	
Data-in hold time (referenced to $\overline{\text{RAS}}$)	t _{DHR}	70		80		90		ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay	t _{CWD}	35		40		45		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay	t _{RWD}	90		110		135		ns	
Transition time (rise and fall)	t _T	3	50	3	50	3	50	ns	
Refresh Period (512 cycles)	t _{REF}		8		8		8	ms	
$\overline{\text{CAS}}$ set-up time (CAS-before-RAS refresh)	t _{CSR}	10		10		10		ns	
$\overline{\text{CAS}}$ hold time (CAS-before-RAS refresh)	t _{CHR}	20		25		30		ns	

MT4C4256E ONLY:

Output Enable	t _{OE}		25		25		30	ns	
Output Disable	t _{OD}		25		25		30	ns	