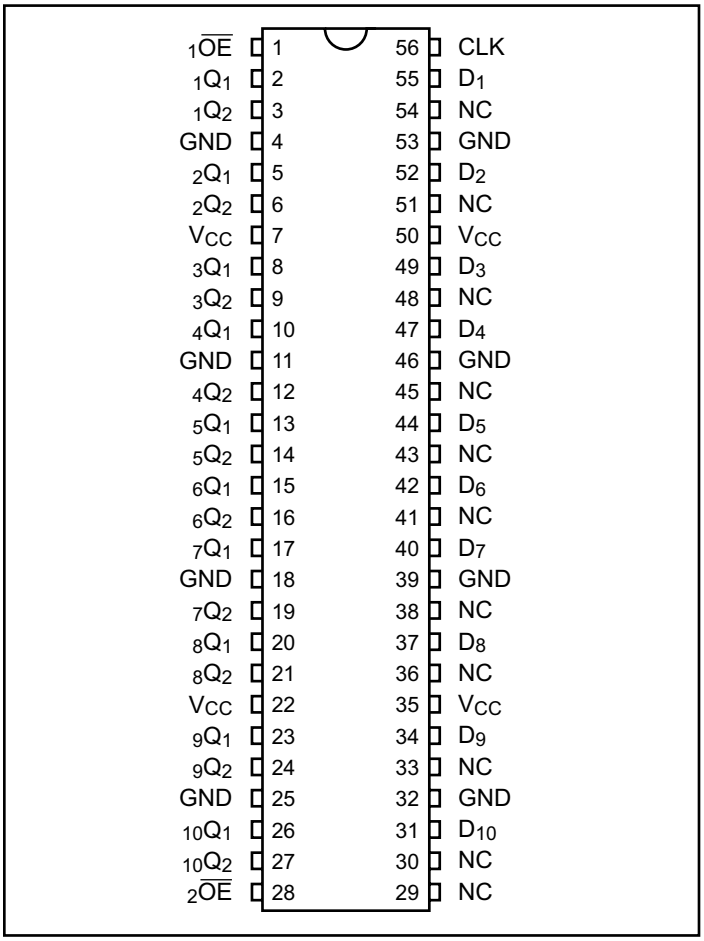
2.5V 10-Bit Flip-Flop with Dual and 3-State Outputs

Features

- PI74AVC+16820 is designed for low-voltage operation, V_{CC} = 1.65V to 3.6V
- True ±24mA Balanced Drive @ 3.3V
- I_{OFF} supports Partial power-down operation
- 3.6V I/O Tolerant inputs and outputs
- All outputs contain a patented DDC (Dynamic Drive-Control) circuit that reduces noise without degrading propagation delay.
- Industrial operation: –40°C to +85°C
- Packaging (Pb-free & Green available):
  – 56-pin 240-mil wide plastic TSSOP (A)
  – 56-pin 173-mil wide plastic TVSOP (K)

Pin Configuration



Description

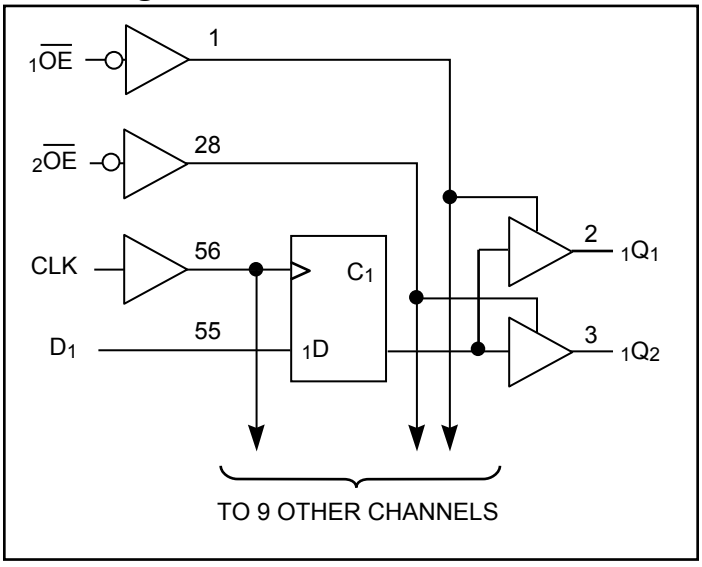
Pericom Semiconductor's PI74AVC+16820, a 10-bit flip-flop designed for 1.65V to 3.6V V_{CC} operation. It is designed with edge-triggered D-type flip- flops. On the positive transition of clock (CLK) input. The device provides true data at the Q outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (HIGH or LOW level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capacity to drive bus lines without the need for interface or pullup components.

$\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor whose minimum value is determined by the current sinking capability of the driver.

Block Diagram



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply voltage range, V_{CC}	–0.5V to +4.6V
Input voltage range, V_I	–0.5V to +4.6V
Voltage range applied to any output in the high-impedance or power-off state, V_O(1)	–0.5V to +4.6V
Voltage range applied to any output in the high or low state, V_O(1,2)	–0.5V to V_{CC} +0.5V
Input clamp current, I_{IK} (V_I <0)	–50mA
Output clamp current, I_{OK} (V_O <0)	–50mA
Continuous output current, I_O	±50mA
Continuous current through each V_{CC} or GND	±100mA
Package thermal impedance, θ_{JA}(3): package A	64°C/W
package K	48°C/W
Storage Temperature range, T_{stg}	–65°C to 150°C

Notes:

1. Input & output negative-voltage ratings may be exceeded if the input and output curent rating are observed.
2. Output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51.
4. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth Table each Flip-Flop(1)

Inputs			Outputs
$\overline{OE}_n$	CLK	D_n	Q_n
L	↑	H	H
L	↑	L	L
L	L	X	Qo
H	X	X	Z

Notes:

1. H = High Signal Level, L = Low Signal Level, X = Irrelevant; Z = High Impedance, Qo = Output Level before the indicated steady-state conditions were established.

Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
CLK	Clock Input (Active HIGH)
Q_n	3-State Outputs
D_n	Data Inputs
GND	Ground
V_{CC}	Power

Recommended Operating Conditions(1)

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{CC}	Supply Voltage	Operating	1.65	3.6	V
		Data retention only	1.2		
V_{IH}	High-level Input Voltage	V_{CC} = 1.2V	V_{CC}		
		V_{CC} = 1.65V to 1.95V	0.65 x V_{CC}		
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 3V to 3.6V	2		
V_{IL}	Low-level Input Voltage	V_{CC} = 1.2V		GND	
		V_{CC} = 1.65V to 1.95V		0.35 x V_{CC}	
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 3V to 3.6V		0.8	
V_I	Input Voltage		0	3.6	
V_O	Output Voltage	Active State	0	V_{CC}	
		3-State	0	3.6	
I_{OH}	High-level output current	V_{CC} = 1.65V to 1.95V		– 6	mA
		V_{CC} = 2.3V to 2.7V		– 12	
		V_{CC} = 3V to 3.6V		– 24	
I_{OL}	Low-level output current	V_{CC} = 1.65V to 1.95V		6	
		V_{CC} = 2.3V to 2.7V		12	
		V_{CC} = 3V to 3.6V		24	
$\Delta_T\Delta_V$	Input transition rise or fall rate	V_{CC} = 1.65V to 3.6V		5	ns/V
T_A	Operating free-air temperature		–40	85	C°

Notes:
1. All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C +85°C)

Parameters		Test Conditions[1]	V_{CC}	Min.	Typ.	Max.	Units
V_{OH}		I_{OH} = –100µA	1.65V to 3.6V	V_{CC} –0.2V			V
		I_{OH} = –6mA, V_{IH} = 1.07V	1.65V	1.2			
		I_{OH} = –12mA, V_{IH} = 1.7V	2.3V	1.75			
		I_{OH} = –24mA, V_{IH} = 2V	3V	2			
V_{OL}		I_{OL} = 100µA	1.65V to 3.6V			0.2	
		I_{OL} = 6mA, V_{IH} = 0.57V	1.65V			0.45	
		I_{OL} = 12mA, V_{IH} = 0.7V	2.3V			0.55	
		I_{OL} = 24mA, V_{IH} = 0.8V	3V			0.8	
I_I		V_I = V_{CC} or GND	3.6V			±2.5	mA
I_{OFF}		V_I or V_O = 3.6V	0			±10	
I_{OZ}		V_I = V_{CC} or GND	3.6V			±10	
I_{CC}		V_O = V_{CC} or GND, V_O = 0	3.6V		40		
C_I	Control Inputs	V_I = V_{CC} or GND	2.5V		4		pF
			3.3V		4		
	Data Inputs		2.5V		6		
			3.3V		6		
C_O	Outputs	V_O = V_{CC} or GND	2.5V		8		
			3.3V		8		

Note:
1. Typical values are measured at T_A = 25°C.

Timing Requirements

(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

	V_{CC} = 1.2V		V_{CC} = 1.5V ± 0.1V		V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK} Clock Frequency						150		180		180	MHz
t_W Pulse duration, CLK high or low					6		3		3		ns
t_{SU} Setup time, data before CLK					5.7		3.5		2.5		
t_H Hold time, data after CLK					1.2		1		1		

Switching Characteristics

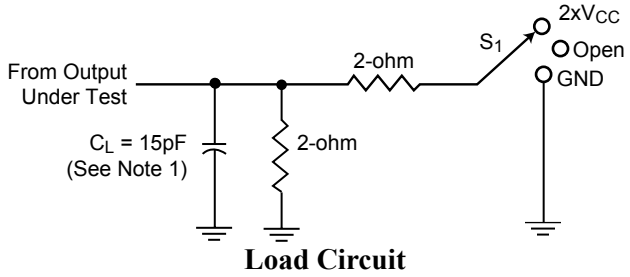
(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

Parameters	From (Input)	To (Output)	V_{CC} = 1.2V		V_{CC} = 1.5V ± 0.1V		V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}							150		180		180		MHz
t_{PD}	CLK	Q						4		3.2		2.7	ns
t_{EN}	$\overline{OE}$	Q						5.8		5.1		4.5	
t_{DIS}	$\overline{OE}$	Q						5		4.6		4.2	

Operating Characteristics, T_A= 25°C

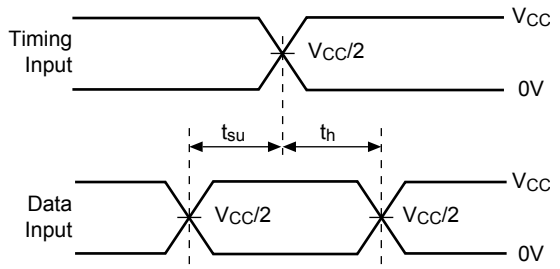
Parameters		Test Conditions	V_{CC} = 1.8V ± 0.15V	V_{CC} = 2.5V ± 0.2V	V_{CC} = 3.3V ± 0.3V	Units
			Typical	Typical	Typical	
Cpd Power Dissipation Capacitance	Outputs Enabled	C_L = 0pF, f = 10 MHz, 2 outputs switching	40	48	55	pF
	Outputs Disabled		23	27	32	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.2V and 1.5V ± 0.1V

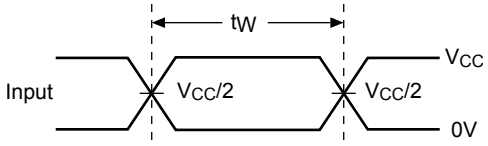


Load Circuit

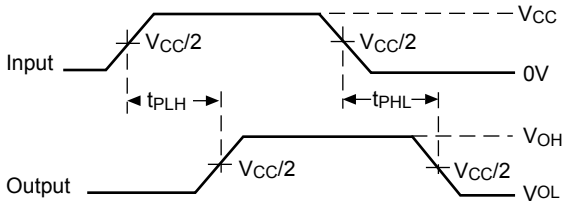
Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND



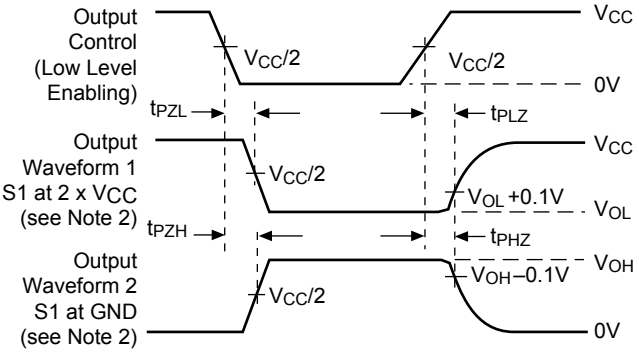
Voltage Waveforms Setup and Hold Times



Voltage Waveforms Pulse Duration



Voltage Waveforms Propagation Delay Times



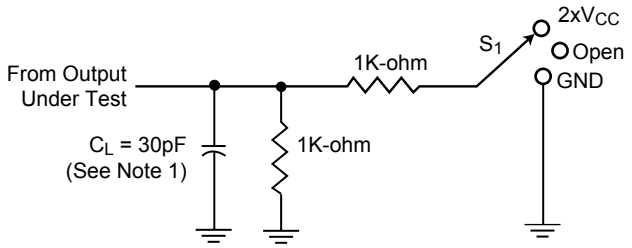
Voltage Waveforms Enable and Disable Times

Figure 1. Load Circuit and Voltage Waveforms

Notes:

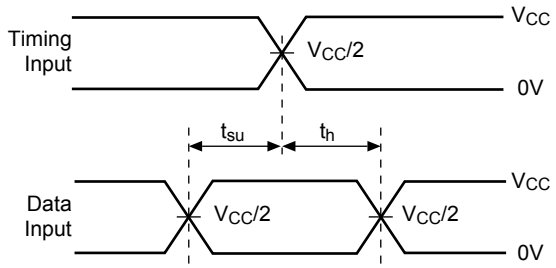
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}
6. t_{PZL} and t_{PZH} are the same as t_{en}
7. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.8V ±0.15V

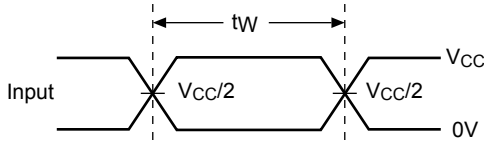


Load Circuit

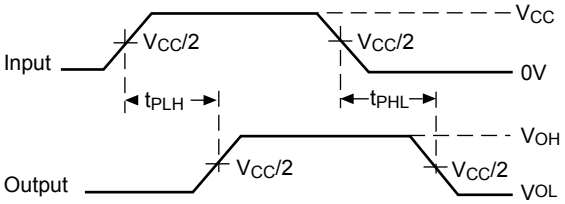
Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND



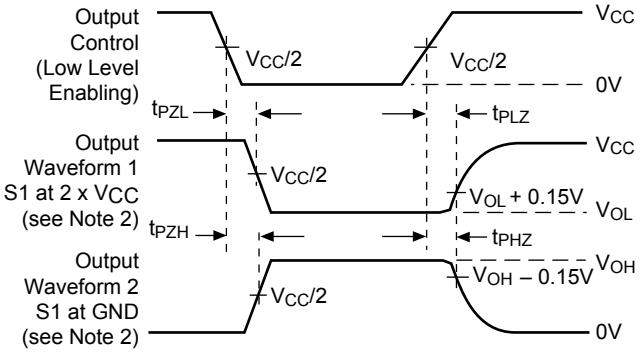
Voltage Waveforms Setup and Hold Times



Voltage Waveforms Pulse Duration



Voltage Waveforms Propagation Delay Times



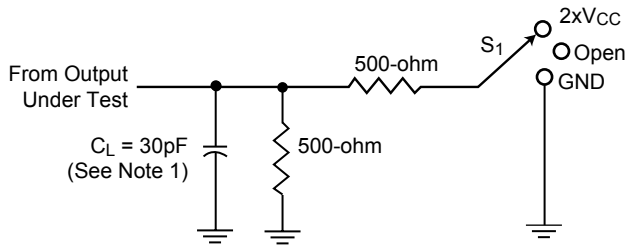
Voltage Waveforms Enable and Disable Times

Figure 2. Load Circuit and Voltage Waveforms

Notes:

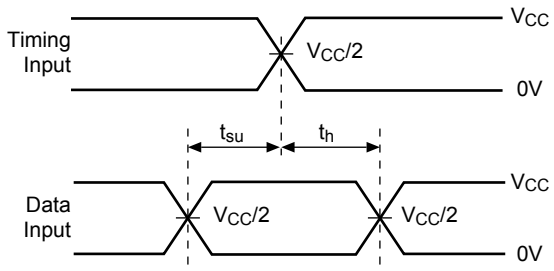
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}
6. t_{PZL} and t_{PZH} are the same as t_{en}
7. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5V ±0.2V

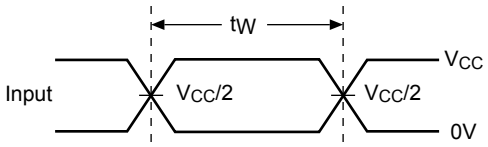


Load Circuit

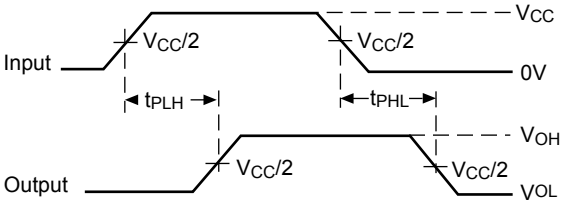
Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND



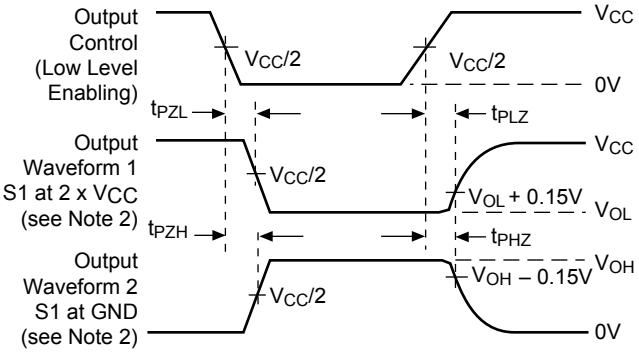
Voltage Waveforms Setup and Hold Times



Voltage Waveforms Pulse Duration



Voltage Waveforms Propagation Delay Times



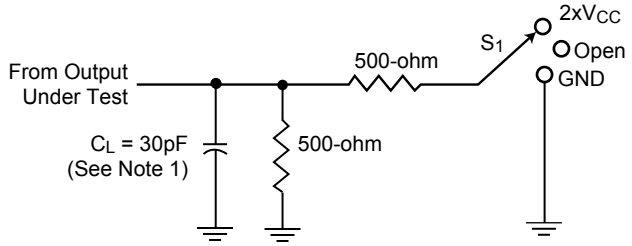
Voltage Waveforms Enable and Disable Times

Figure 3. Load Circuit and Voltage Waveforms

Notes:

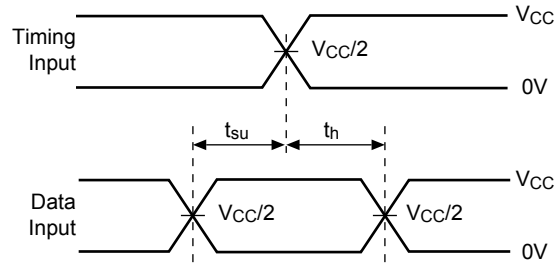
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}
6. t_{PZL} and t_{PZH} are the same as t_{en}
7. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3V ±0.3V

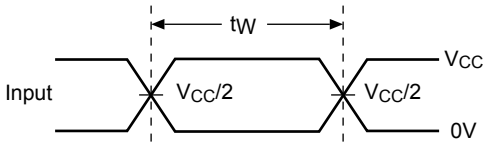


Load Circuit

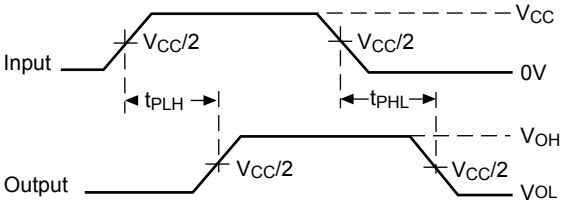
Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND



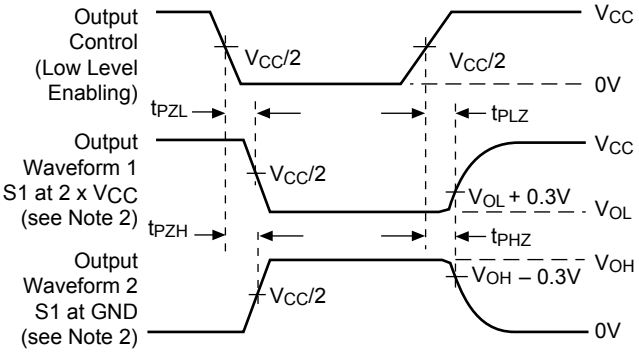
Voltage Waveforms Setup and Hold Times



Voltage Waveforms Pulse Duration



Voltage Waveforms Propagation Delay Times



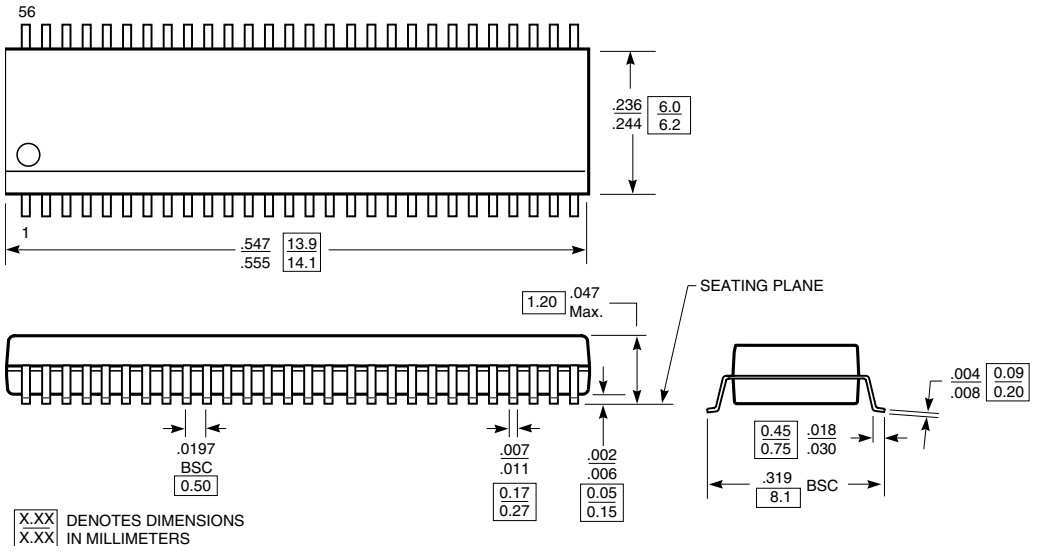
Voltage Waveforms Enable and Disable Times

Figure 4. Load Circuit and Voltage Waveforms

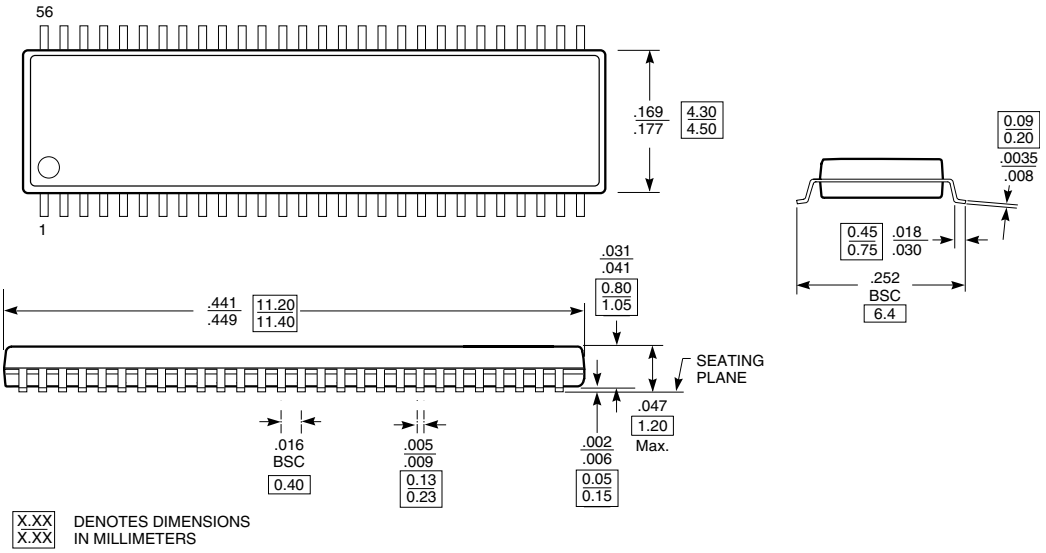
Notes:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}
6. t_{PZL} and t_{PZH} are the same as t_{en}
7. t_{PLH} and t_{PHL} are the same as t_{pd}

Packaging Mechanical: 56-pin TSSOP (A)



Packaging Mechanical: 56-pin TVSOP (K)



Ordering Information

Ordering Code	Package Code	Package Description
PI74AVC+16820A	A	56-pin, 240-mil wide plastic TSSOP
PI74AVC+16820AE	A	Pb-free & Green, 56-pin, 240-mil wide plastic TSSOP
PI74AVC+16820K	K	56-pin, 173-mil wide plastic TSSOP
PI74AVC+16820KE	K	Pb-free & Green, 56-pin, 173-mil wide plastic TSSOP

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/