

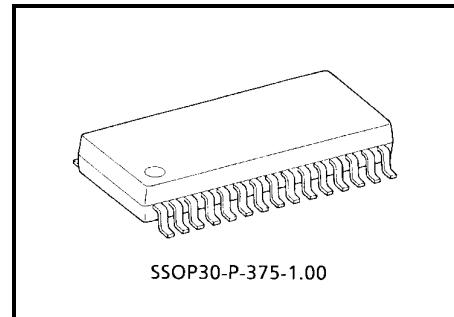
TA8696F

γ Correction IC for LCD TV

TA8696F operates with a power supply voltage of 3.3 to 7.5 V and can be directly driven with a dry battery.

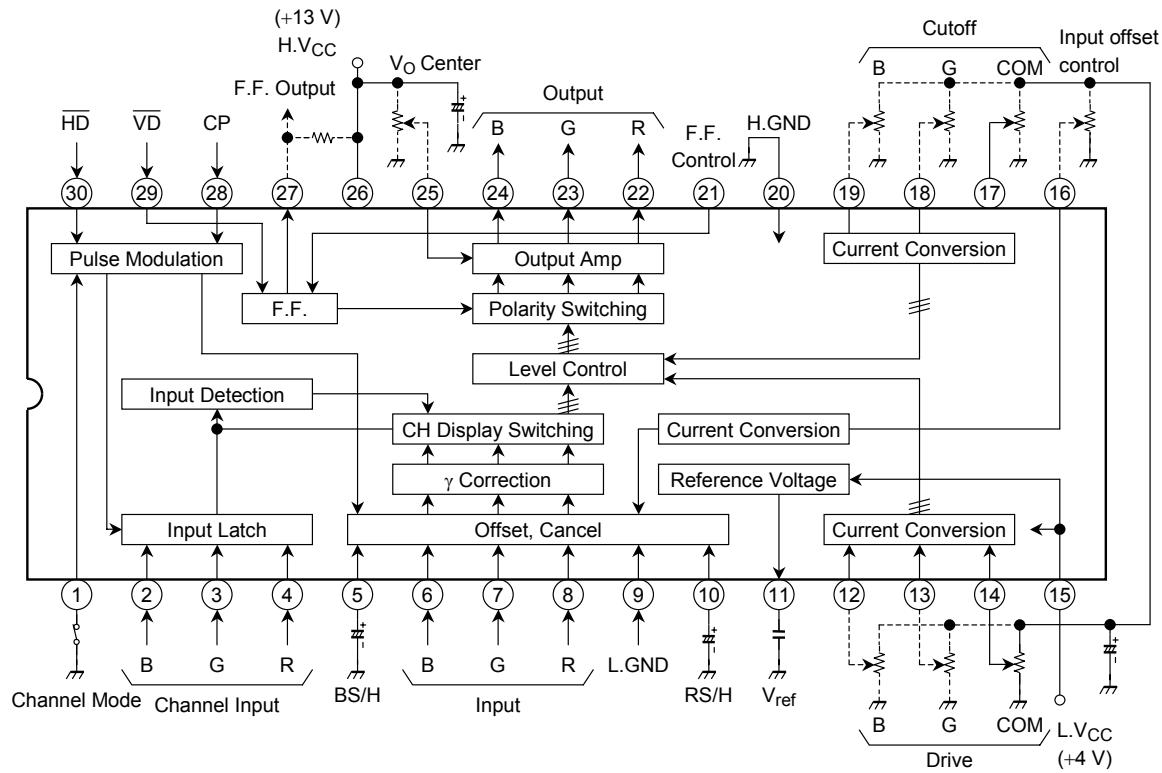
Features

- Enables high-precision γ correction using logarithmic compression.
- γ correction for normally white LCD panel is possible.
- Offset/cancel input circuit enables high-quality γ correction without distorting the primary color input signals.
- Cut-off voltage and drive voltage can be independently controlled.
- Unsusceptible to negative effects of fluctuation of power supply voltage.
- Either latch mode or through mode can be selected using the CH display mode switching pin.



Weight: 0.63 g (typ.)

Block Diagram

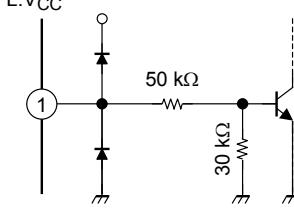
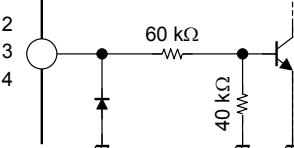
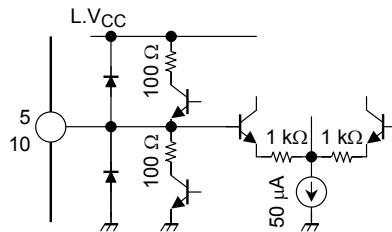
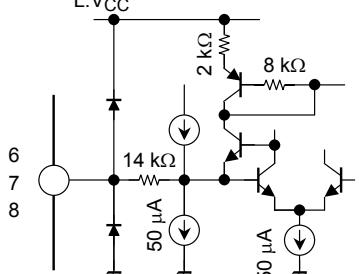
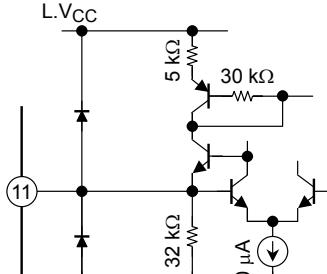


Pin Function

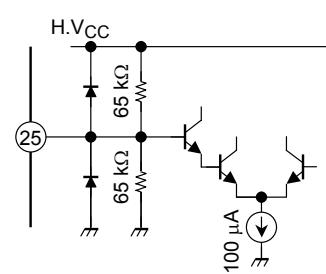
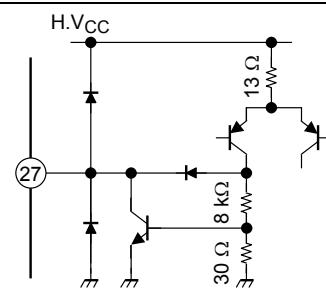
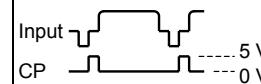
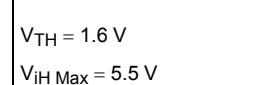
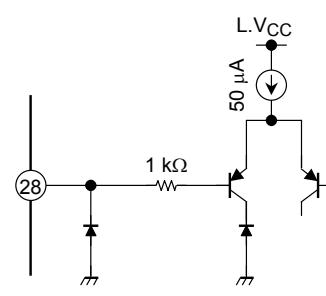
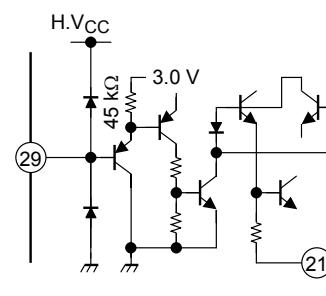
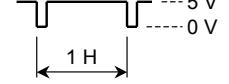
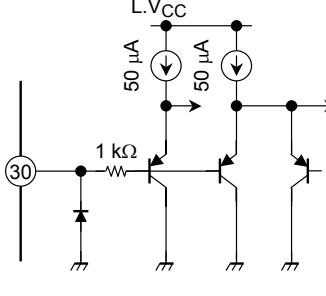
Pin No.	Pin Name	Reference Voltage (V)	Reference Current (mA)	Function
1	Mode Switch	0	0	CH display mode switching (latch mode/through mode)
2	CH B Input	0	0	CH display signal blue input
3	CH G Input	0	0	CH display signal green input
4	CH R Input	0	0	CH display signal red input
5	BS/H	1.6	0	Blue input signal sample and hold capacitor
6	B Input	1.6	0	Blue primary color input
7	G Input	1.6	0	Green primary color input
8	R Input	1.6	0	Red primary color input
9	L.GND	0	-8.1	Low-voltage signal GND
10	RS/H	1.6	0	Red input signal sample and hold capacitor
11	V _{ref}	1.6	0	Internal reference voltage
12	B Drive	2	0	B-axis drive control
13	R Drive	2	0	R-axis drive control
14	COM Drive	2	0	Common drive control
15	L.VCC	4.0	8.1	Low-voltage signal VCC
16	γ Offset	2	0	γ correction starting point control
17	COM Cut-off	2	0	Common cut-off control
18	R Cut-off	2	0	R-axis cut-off control
19	B Cut-off	2	0	B-axis cut-off control
20	H.GND	0	-4.6	High-voltage signal GND
21	F.F. CONT.	1.4	—	—
22	R Output	6.5	0	Red signal input
23	G Output	6.5	0	Green signal input
24	B Output	6.5	0	Blue signal input
25	V _O Center	6.5	0	Signal output center voltage control
26	H.VCC	13.0	4.6	High-voltage signal VCC
27	F.F. Output	0.2	0	Flip-flop output
28	CP	0.9	0	Clamp pulse input
29	VD	1.4	0	Vertical drive pulse input
30	HD	0.9	0	Horizontal drive pulse input

Note 1: Reference voltage and reference current are for DC bias with no signal.

The current which flows into the IC considered to be positive current.

Pin No.	Pin Name and Function	Typical Signal Level	Interface Current
1	Mode switch Switches channel indication mode High level: Character mode Low level: Latch mode (synchronized with HD)	Internal bias 0 V $V_{iH} = L.V_{CC}$ $V_{iL} = GND$ $V_{TH} = 1.9 V$ $V_{iH\ Max} = L.V_{CC}$ $V_{iL\ Min} = GND$ Clamped on $L.V_{CC}$ and GND	
2	CH B input	Internal bias 0 V	
3	CH G input	0 V	
4	CH R input	$V_{TH} = 1.7 V$	
	Channel indication signal	$V_{iH\ Max} = 5.5 V$	
	Input pin	$V_{iL\ Min} = GND$	
		Clamped on GND	
5	BS/H	Internal bias 1.6 V	
10	RS/H	External capacitance 1 μF	
	Regenerate B/R-axis direct current voltage	Permissible load current 0	
	Capacitor pin	Clamped on $L.V_{CC}$ and GND	
6	B input	Internal bias 1.6 V	
7	G input	White signal level 1.6 V	
8	R input	Black signal level 0.9 V	
	Primary color input pins	Maximum input level 1.4 V _{p-p}	
		Clamped on $L.V_{CC}$ and GND	
11	V_{ref}	Internal standard voltage reference pin	
		Permissible load current 0	
		Clamped on $L.V_{CC}$ and GND	

Pin No.	Pin Name and Function	Typical Signal Level	Interface Current
12 13 18 19	B drive R drive R cut-off B cut-off	Internal bias L.VCC/2 V_{iH} Max = L.VCC V_{iL} Min = GND Clamped on L.VCC and GND	<p>This diagram shows the interface circuit for pins 12, 13, 18, and 19. It consists of a 40 kΩ pull-up resistor from pin 13 to L.VCC. Pin 12 is connected to the base of a PNP transistor, which has its collector connected to the base of another PNP transistor. The collector of this second PNP transistor is connected to the base of a third PNP transistor, whose collector is connected to pin 18. The collector of the third PNP transistor is connected to the base of a fourth PNP transistor, whose collector is connected to pin 19. The collectors of the first three PNP transistors are connected to ground through 5 kΩ resistors. The collector of the fourth PNP transistor is connected to L.VCC through a 150 μA current source. The emitters of all four PNP transistors are connected to ground.</p>
14 17	COM drive COM cut-off	Internal bias L.VCC/2 V_{iH} Max = L.VCC V_{iL} Min = GND Clamped on L.VCC and GND	<p>This diagram shows the interface circuit for pins 14 and 17. It consists of a 40 kΩ pull-up resistor from pin 17 to L.VCC. Pin 14 is connected to the base of a PNP transistor, which has its collector connected to the base of another PNP transistor. The collector of this second PNP transistor is connected to the base of a third PNP transistor, whose collector is connected to pin 17. The collector of the third PNP transistor is connected to the base of a fourth PNP transistor, whose collector is connected to pin 14. The collectors of the first three PNP transistors are connected to ground through 5 kΩ resistors. The collector of the fourth PNP transistor is connected to L.VCC through a 20 kΩ resistor. The emitters of all four PNP transistors are connected to ground.</p>
16	γ off-set	Internal bias L.VCC/2 V_{iH} Max = L.VCC V_{iL} Min = GND Clamped on L.VCC and GND	<p>This diagram shows the interface circuit for pin 16. It consists of a 40 kΩ pull-up resistor from pin 16 to L.VCC. Pin 16 is connected to the base of a PNP transistor, which has its collector connected to the base of another PNP transistor. The collector of this second PNP transistor is connected to the base of a third PNP transistor, whose collector is connected to pin 16. The collector of the third PNP transistor is connected to the base of a fourth PNP transistor, whose collector is connected to L.VCC. The collectors of the first three PNP transistors are connected to ground through 5 kΩ resistors. The collector of the fourth PNP transistor is connected to L.VCC through a 100 μA current source. The emitters of all four PNP transistors are connected to ground.</p>
22 23 24	R output G output B output	Inverted in sync with VD <p>The timing diagram shows the inverted signal levels for the R, G, and B outputs relative to the VD signal. The levels are: 11.5 Black, 8.5 White, 6.5, 4.5 White, and 1.5 Black. The outputs are clamped on H.VCC and GND.</p> <p>Clamped on H.VCC and GND</p>	<p>This diagram shows the interface circuit for pins 22, 23, and 24. It consists of a 50 kΩ pull-up resistor from pin 24 to H.VCC. Pin 22 is connected to the base of a PNP transistor, which has its collector connected to the base of another PNP transistor. The collector of this second PNP transistor is connected to the base of a third PNP transistor, whose collector is connected to pin 24. The collector of the third PNP transistor is connected to the base of a fourth PNP transistor, whose collector is connected to pin 23. The collectors of the first three PNP transistors are connected to ground through 50 kΩ resistors. The collector of the fourth PNP transistor is connected to H.VCC through a 6.5 kΩ resistor. The emitters of all four PNP transistors are connected to ground. A 100 μA current source is also connected between the collector of the fourth PNP transistor and H.VCC.</p>

Pin No.	Pin Name and Function	Typical Signal Level	Interface Current
25	V _O center	Internal bias H.V _{CC} /2 V _{iH Max} = H.V _{CC} V _{iL Min} = GND Clamped on H.V _{CC} and GND	
27	F.F. output	Desaturated open collector output Maximum sink current 0.5 mA (V _{oL Max} = 0.3 V) V _{oH Max} = H.V _{CC} Clamped on H.V _{CC} and GND	
28	CP Clamp pulse input	Be sure CP is correspondent to the back porch of primary color input signal. Input:  CP:  V _{TH} = 1.6 V V _{iH Max} = 5.5 V V _{iL Min} = GND Clamped on H.V _{CC} and GND	
29	\overline{VD} input Vertical drive pulse input	Be sure \overline{VD} falls within the vertical blanking period of primary color input signal. Input:  V _{TH} = V _{iH Max} = 5.5 V V _{iL Min} = GND Clamped on H.V _{CC} and GND	
30	\overline{HD} input	Be sure \overline{HD} falls within the horizontal blanking period of primary color input signal. Input:  V _{TH} = 0.9 V V _{iH Max} = 5.5 V V _{iL Min} = GND Clamped on GND	

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	L.V _{CC}	8	V
Power supply voltage	H.V _{CC}	14.5	V
Power dissipation	P _D	890	mW
Power dissipation lowering rate	θ _{ja}	7.2	mW/°C
Operating temperature	T _{opr}	-20 to +75	°C
Storage temperature	T _{stg}	-55 to 150	°C

Note 2: When the IC is operated at 25°C or higher, reduce power dissipation by 12.8 mW per degree.

Recommended Power Supply Voltage

Pin No.	Pin Name	Min	Typ.	Max	Unit
15	L.V _{CC}	3.3	5.0	7.5	V
26	H.V _{CC}	10.0	13.0	14.0	

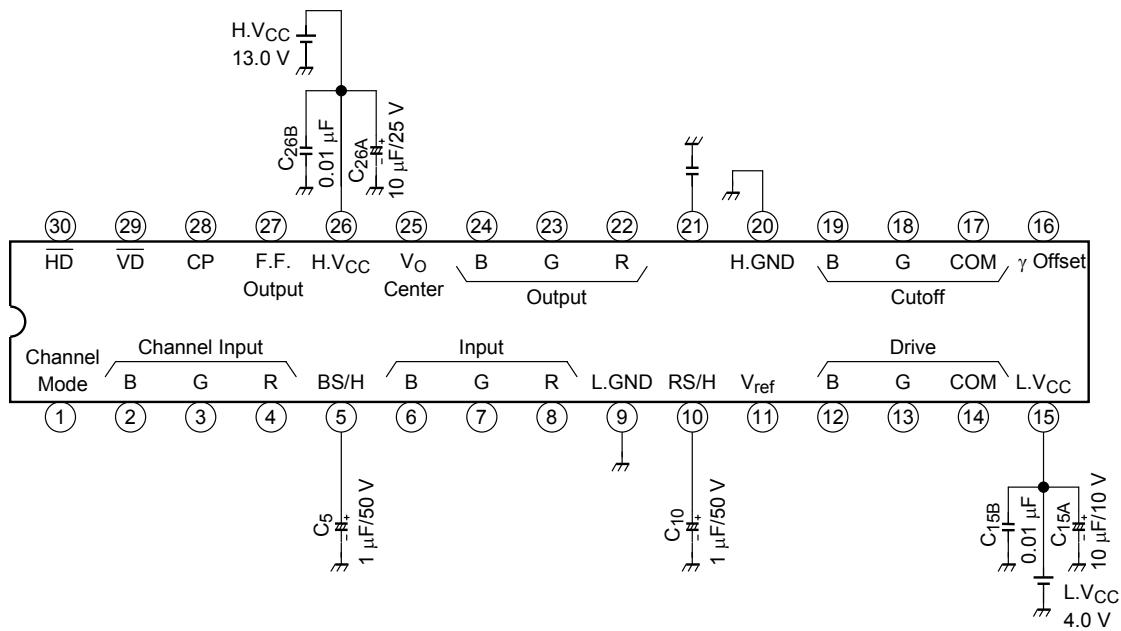
Electrical Characteristics (unless otherwise specified, V_{CC} = 4 V, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
[1] Operating range							
Primary color input white signal level	—	2	The same conditions are given to R/G/B-axis.	—	1.6	—	V
Primary color input black signal level	—	2	The same conditions are given to R/G/B-axis.	—	0.9	—	V
CH indication signal level	—	2	The same conditions are given to R/G/B-axis.	3	5	5.5	V
Timing pulse level	—	2	HD, VD, LD	3	5	5.5	V
[2] Electrical characteristics							
Operating power supply current (1)	—	2	Pin 15.L.V _{CC} = 4 V No load.	5.8	8.4	10.9	mA
Operating power supply current (2)	—	2	Pin 26.H.V _{CC} = 13 V No load.	3.2	4.6	6.0	mA
Input signal dynamic range	—	2	—	1.2	1.4	1.6	V
Input signal pin resistor	R _{IN}	2	—	10.5	14.0	17.5	kΩ
Input signal pin capacity	C _{IN}	2	—	—	1	3	pF
Black signal level off-set	—	2	γ off-set open	—	100	200	mV
Black signal level off-set difference in the axes	—	2	—	—	50	100	mV
Black signal level off-set adjustment amount	—	2	—	—	0.3	—	V
Black signal level off-set adjustment sensitivity	—	2	—	—	300	—	mV/V
Input off-set elimination capacity	—	2	—	20	26	—	dB
Off-set cancel difference in the axes	—	2	—	—	50	—	mV
Typical gain	—	2	Drive adjustment open	9.4	12.4	15.4	dB
Typical gain difference in the axes	—	2	Drive adjustment open	—	0.5	—	dB
Typical gain difference in the polarity	—	2	Drive adjustment open	—	0.5	—	dB
Maximum gain	—	2	—	15.4	18.4	—	dB
Minimum gain	—	2	—	—	-20	-10	dB

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Gain control sensitivity	—	2	—	—	6	—	dB/V
Polarity reverse center voltage	—	2	V _O center pin open	6.3	6.5	6.7	V
Polarity reverse center voltage difference in the axes	—	2	—	—	50	100	mV
Polarity reverse center voltage variable range	—	2	—	—	2	—	V
Polarity reverse center voltage controlling sensitivity	—	2	—	—	1	—	V/V
Typical cut-off level (N.W)	—	2	Difference from V _O center voltage	±4.8	±5	±5.2	V
Cut-off level difference in the axes	—	2	—	—	50	100	mV
Cut-off level variable amount	—	2	—	—	±4	—	V
Cut-off level controlling sensitivity	—	2	—	—	2	—	V/V
Output dynamic range	—	2	—	—	10	—	V _{p-p}
Output impedance	—	2	—	—	10	—	Ω
Frequency characteristic	—	2	Loaded amount 120 pF, -3dB point	3	4	—	MHz
Frequency characteristic difference in the axes	—	2	Loaded amount 120 pF, -3dB point	—	0.1	0.3	MHz
Slew rate	—	2	Loaded amount 120 pF	—	4	—	V/μs
Slew rate difference in the axes	—	2	Loaded amount 120 pF	—	—	10	%
Crosstalk in the axes	—	2	—	—	50	40	dB
Direct current transmission rate	—	2	—	—	100	—	%
S/N N	—	2	—	40	50	—	dB
CH indication signal threshold	—	2	—	—	2.2	—	V
CH indication mode switch threshold	—	2	—	—	2.2	—	V
CH indication output delay (line mode)	—	2	—	—	1	—	μs
CH indication output delay (dot mode)	—	2	—	—	0.1	—	μs
CH indication latch minimum operation voltage	—	2	—	—	—	3	V
HD pulse threshold	—	2	—	1.3	1.6	1.9	V
LD pulse threshold	—	2	—	1.3	1.6	1.9	V
VD pulse threshold	—	2	—	1.3	1.6	1.9	V
F.F. minimum operation voltage	—	2	—	—	—	10	V
F.F. phase delay	—	2	—	—	3	—	μs
F.F. response frequency	—	2	—	20	—	—	kHz
F.F. output high level	—	2	—	11.0	13.0	—	V
F.F. output low level	—	2	—	0.1	0.3	0.5	V
γ correction value (1) NW	—	2	—	—	0.35	—	—
γ correction value (2) NW	—	2	—	—	20	—	—
γ correction value difference in the axes (1)	—	2	—	—	—	10	%
γ correction value difference in the axes (2)	—	2	—	—	—	10	%

Test Circuit 1

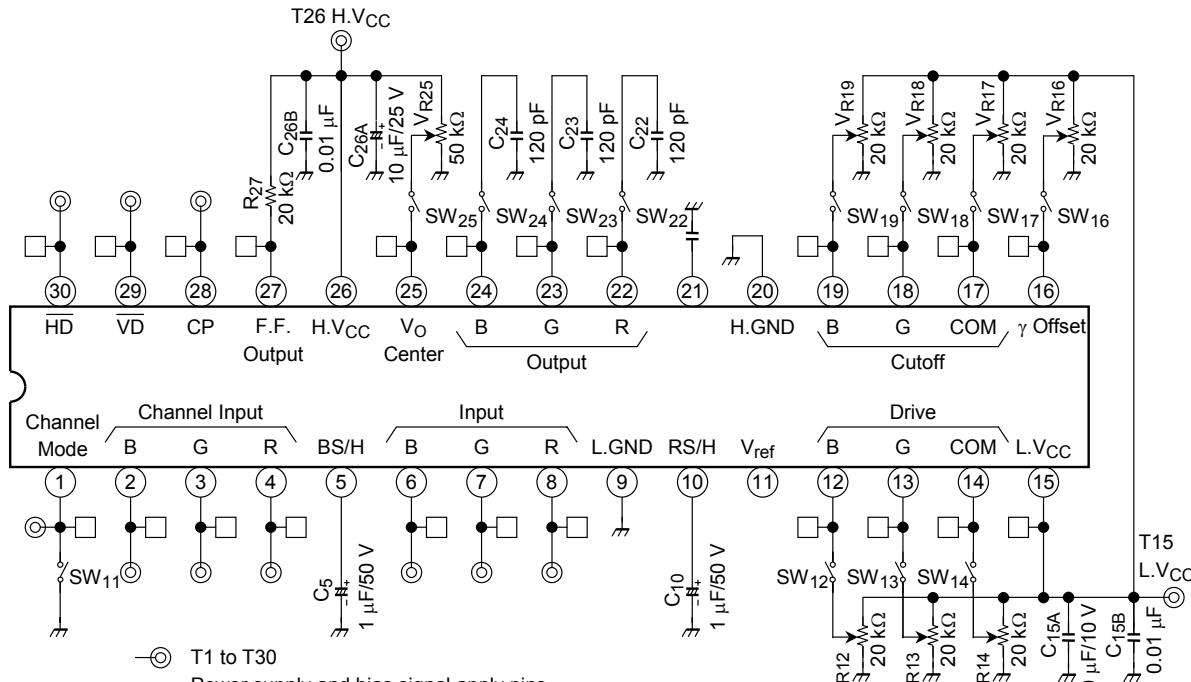
Direct Current Characteristic



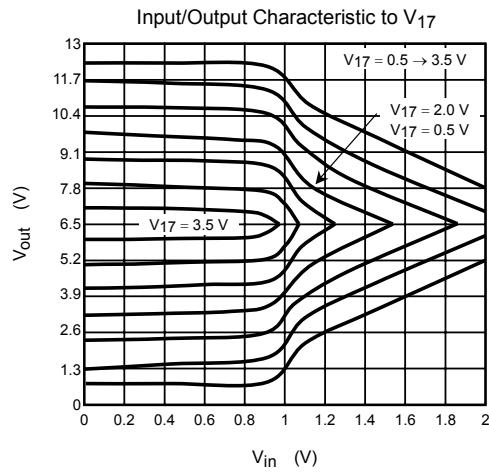
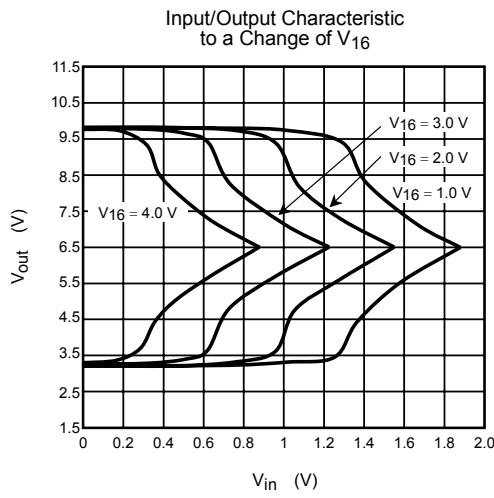
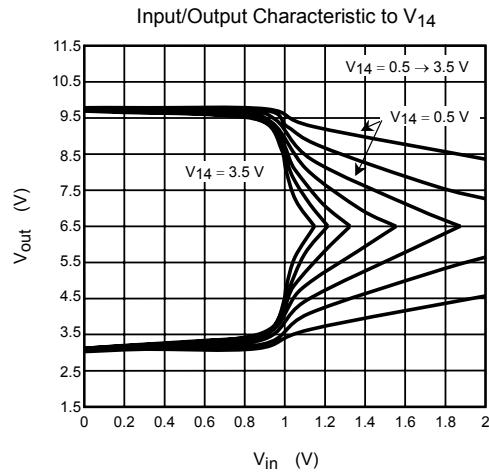
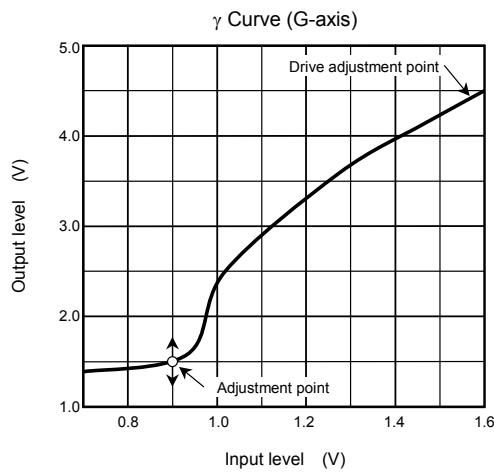
Note 3: Connect test pins directly to IC pins. (not shown above.)
Test value is written as V.1 to V.30.

Test Circuit 2

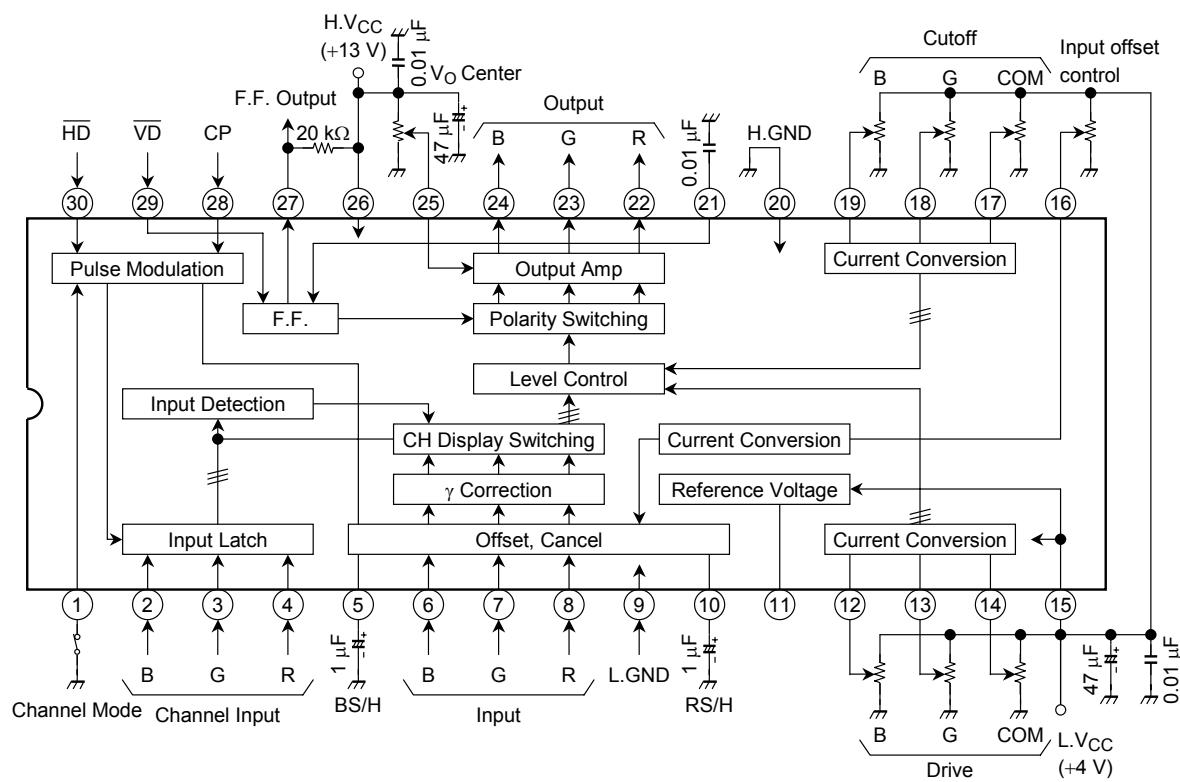
Alternating Current Characteristic



Note 4: The numbers of testing pins are not shown above because they are the same as IC pin numbers.



Typical Application Circuits

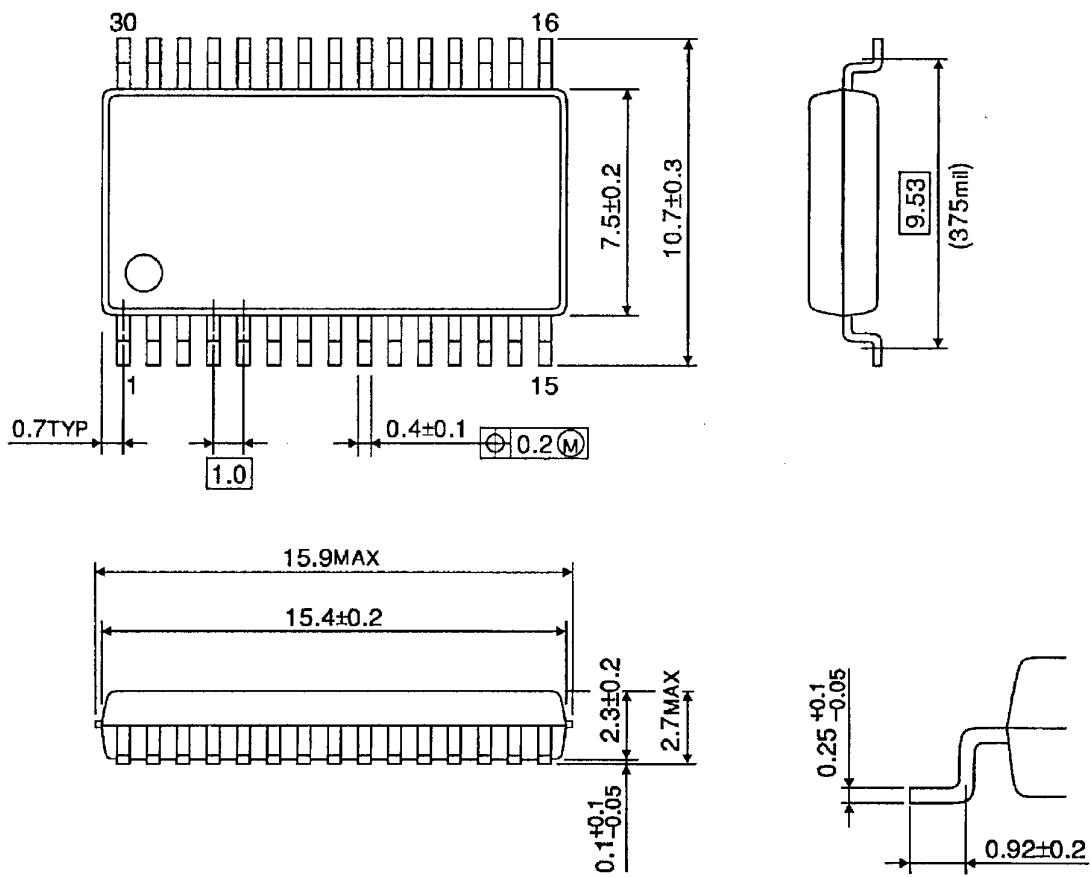


- All control VRs are 20 kΩ. Connect 0.01 μF close to each control pin.

Package Dimensions

SSOP30-P-375-1.00

Unit : mm



Weight: 0.63 g (typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

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