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GEC PLESSEY
SEMICONDUCTORS

SEPTEMBER 1995
PRELIMINARY INFORMATION
DS3112-2.0

P1480

LAN CAM 1kx64-BIT CMOS CONTENT-ADDRESSABLE MEMORY

(Supersedes February 1992 edition - version 1)

The P1480 LAN CAM is a 1K X 64-bit fixed-width CMOS Content-addressable Memory (CAM) aimed at address filtering applications in Local-area Network (LAN) bridges and routers. The architecture of the LAN CAM allows a network station list of any length to be searched in a single memory transaction. This device is also well-suited for other applications that require high-speed data searching such as optical and magnetic disk caches and data base accelerators.

Although the internal data path of the P1480 is 64-bits wide, the external interface is multiplexed four ways to allow communication with the device over a 16-bit bus. Vertical cascading and system flag generation require no external logic. The LAN CAM is synchronously controlled by four wires in much the same way as standard memories are controlled. A powerful instruction set increases the control flexibility and minimizes software overhead in typical systems. A data translation facility converts between IEEE 802.3 (CSMA/CD) and 802.5 (Token Ring) address formats on command. Both random access and associative operations are supported by this device. Flexible bit- and word-masking facilities enhance the associative operations. These and other features make the P1480 a powerful, yet easy to use, associative memory which drastically reduces data search delays.

FEATURES

- 1K X 64-bit CMOS Content-addressable Memory (CAM)
- 64-bit internal data path multiplexed four ways over a 16-bit I/O interface
- Simple four-wire synchronous control directly usable in conventional memory subsystems
- Extensive instruction set adds control flexibility Memory Array width can be configured as a mixture of CAM and RAM on 16-bit boundaries
- Memory operations allow random access, associative access, and write-at-next-free-address cycles
- Vertical cascading and system flag generation require no external logic
- Two Mask registers allow masking of individual bits for both writing and comparing
- Priority encoder returns highest-priority match address
- Device gives status information after each operation
- Two validity bits per location provide a word masking facility and valid or empty information

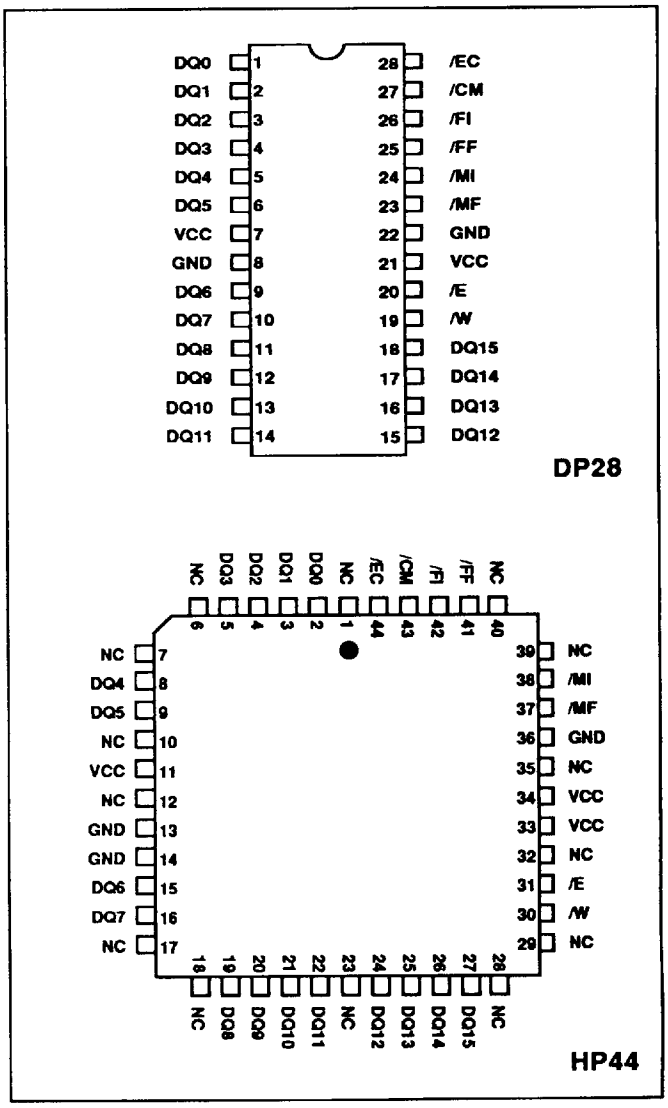


Fig.1 Pin connections (top view)

- Programmable data translation facility converts between IEEE 802.3 and 802.5 formats
- Manufactured in CMOS technology with TTL-compatible inputs and outputs
- Packaged in industry-standard 28-pin PDIP and 44-pin PLCC packages

ORDERING INFORMATION

PART NUMBER	CYCLE TIME	PACKAGE	TEMPERATURE RANGE
P1480-12CGDPAS	120ns	28-PIN PDIP	0-70°C
P1480-12CGHPAS	120ns	44-PIN PLCC	0-70°C
P1480-15CGDPAS	150ns	28-PIN PDIP	0-70°C
P1480-15CGHPAS	150ns	44-PIN PLCC	0-70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0.5 to 7.0 Volts
Voltage on all Other Pins	–0.5 to VCC+0.5 Volts (-2.0 Volts for 10 ns, measured at the 50% point)
Temperature Under Bias	–40°C to +85°C
Storage Temperature	–55°C to +125°C
DC Output Current	20 mA (per Output, one at a time, one second duration)

Notes
1. Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.
2. All voltages are referenced to GND.

OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{CC}	Operating Supply Voltage	4.5	5.0	5.5	Volts	
V_{IH}	Input Voltage Logic "1"	2.0		V_{CC}+0.5	Volts	
V_{IL}	Input Voltage Logic "0"	-0.5		0.8	Volts	see notes 2 and 3 below
T_A	Ambient Operating Temperature	0		70	°C	Still Air

Notes
1. All voltages referenced to GND at the device pin.
2. -1.0V for a duration of 10ns measured at 50% amplitude for Input-only lines (see Fig.9).
3. Common I/O lines are clamped so that signal transients cannot fall below -0.5V.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Conditions
I_{CC}	Average Power Supply Current		200	mA	
V_{OH}	Output Voltage Logic "1"	2.4		Volts	I_{OH} = -2.0 mA
V_{OL}	Output Voltage Logic "0"		0.4	Volts	I_{OL} = 4.0 mA
I_{IZ}	Input Leakage Current	-2	2	µA	$V_{SS} \leq$ VIN $\leq$ VCC
I_{OZ}	Output Leakage Current	-10	10	µA	$V_{SS} \leq$ VIN $\leq$ VCC; DQ_n = High Impedance

CAPACITANCE

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Input Capacitance	6	pF	f=1MHz, V_{IN}=0V.
C_{OUT}	Output Capacitance	7	pF	f=1MHz, V_{IN}=0V.

AC TEST CONDITIONS

Input Signal Transitions	0.0 to 3.0 volts
Input Signal Rise Time	< 3 ns
Input Signal Fall Time	< 3 ns
Input Timing Reference Level	1.5 volts
Output Timing Reference Level	0.8 to 2.4 volts

PIN DESCRIPTIONS

DQ0-DQ15 (Data Bus, Common I/O, TTL)
The DQ0-DQ15 lines convey data, commands and status to and from the P1480. The direction and nature of the information that flows to or from the device is controlled by the states of /CM and /W.

/E (Chip Enable, Input, TTL)
The /E input, the main clock control, enables the LAN CAM while LOW, latches the control signals /W, /CM, /EC on its falling edge and releases them on the rising edge, and clocks the Destination or Source Segment counter on its rising edge.

/W (Write Enable, Input, TTL)
The /W input selects the direction of data flow during a memory cycle. /W LOW selects a Write cycle, and /W HIGH selects a Read cycle.

/CM (Data/Command Select, Input, TTL)
The /CM input selects whether the inputs on the DQ0-DQ15 lines are data or commands. /CM LOW selects Command cycles and /CM HIGH Data cycles.

/EC (Enable Comparison, Input, TTL)
The /EC input enables the /MF output to show the results of a comparison. If /EC is LOW at the falling edge of /E in a given cycle, the /MF output is enabled. Otherwise, the /MF output is held HIGH.

/MF (Match Flag, Output, TTL)
The /MF output goes LOW when a valid match occurs during a Comparison cycle if the /EC line was latched LOW by the falling edge of /E at the start of the cycle.

/MI (Match Input, Input, TTL)
The /MI input is used in vertically cascaded systems to prioritize devices. In a daisy-chained system, the /MF output of one device is connected to the /MI input of the next lower-priority device in the chain.

/FF (Full Flag, Output, TTL)
The /FF output indicates that all the memory locations within the device contain valid contents. /FF LOW indicates the Full condition.

/FI (Full Input, Input, TTL)
The /FI input is used in vertically cascaded systems to generate CAM Memory System Full indication. In a daisy-chained system, the /FF output of one device is connected to the /FI input of the next-lower priority device in the chain.

VCC, GND (Positive Power Supply and Ground)
These pins are the main power supply connections to the P1480. VCC must be held at +5V + 10% relative to the GND pin, which is at 0V (system reference potential), for correct operation of the device.

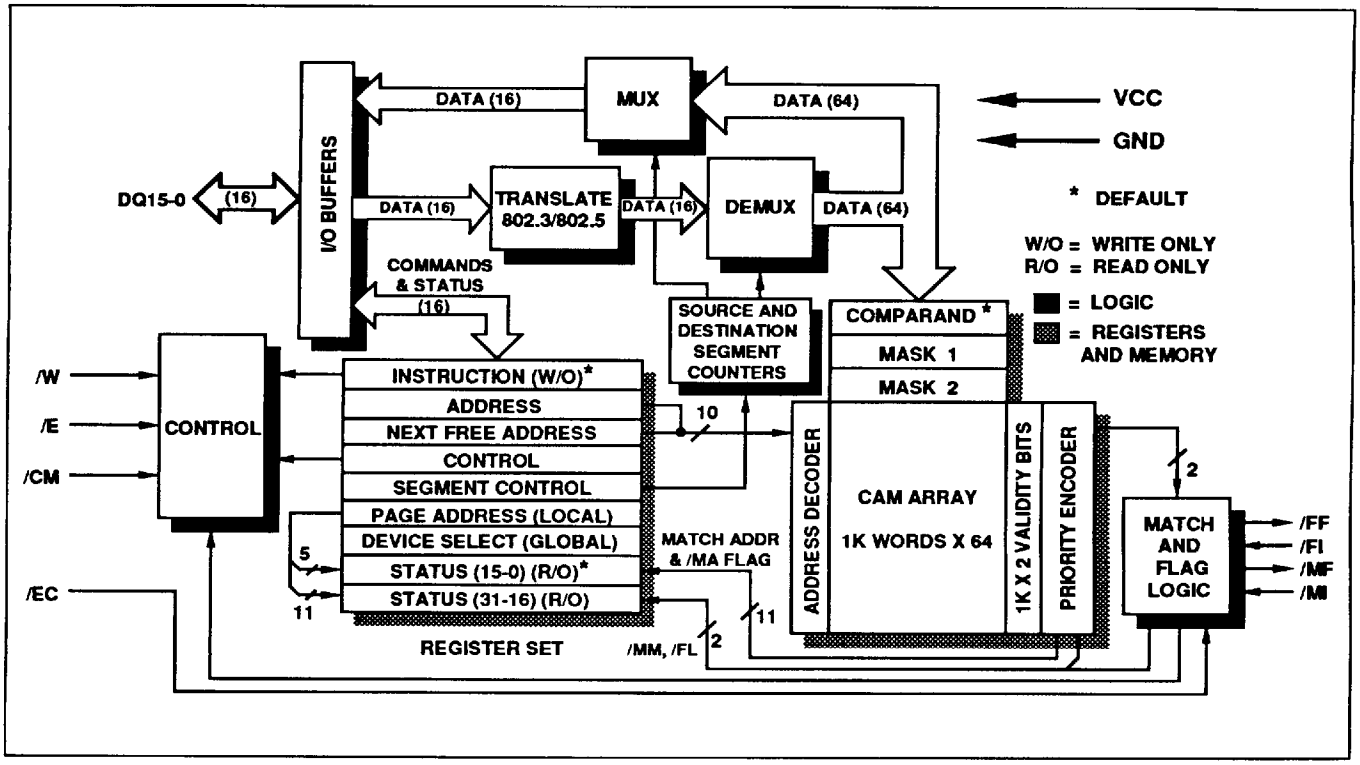


Fig.2 Block Diagram

FUNCTIONAL DESCRIPTION

The GEC Plessey Semiconductors' P1480 is a 1K x 64-bit CAM targeted at address filtering applications in Local-area Network (LAN) Bridges and Routers. The device is designed to hold the station list in the Bridge, allowing single-transaction decisions on whether to pass a data packet from one segment across the Bridge to another.

The P1480 is designed to minimize the external logic needed for expansion and control. It is controlled via four synchronous control signals and by commands loaded into an Instruction register. One of the control signals is used to indicate whether information present on the 16-bit input bus is to be interpreted as a Data or a Command field. During a Random Access cycle, the Address field is loaded into the Instruction Address register during a second Command Write cycle.

The data inputs and outputs of the P1480 are multiplexed four ways over a 16-bit I/O bus. This multiplexing increases the transaction time but allows the device to reside in a 28-pin package. The speed penalty related to the multiplexing is insignificant in the LAN Bridge environment because the address bits to be compared in the CAM are received serially from the network, so the loading is pipelined.

The P1480 contains 65,536 bits of static CAM, organized as 1024 64-bit Data fields. Each Data field can be partitioned into a CAM and a RAM subfield on 16-bit boundaries. In LAN Bridges, the RAM subfield could hold port-address and time-out information, or other data associated with the Destination Address held in the CAM subfield of the location.

Appended to each 64-bit data field are two bits of CAM storage to indicate the validity of the location. These two bits are encoded to render four validity conditions: Valid data, Skip, Empty and Random access only.

The contents of the memory can be randomly accessed or associatively accessed. During a Data Comparison cycle, data is assembled in a Comparand register and is compared with the CAM section of the memory array. Only the locations whose Validity bits are set Valid will enter into comparison with the Comparand. Comparisons can also be done on the Validity bits themselves. Random access to the memory array, using an address to define a unique location, is independent of the state of the Validity bits.

The station list can be held in either the IEEE 802.3 or IEEE 802.5 format. When data is received from the network in other than the selected default storage format, the data bits can be translated during the loading process. This facility simplifies bridging between CSMA/CD and Token Ring networks.

Two Mask registers on the device can be selected to mask comparison or data writes. For comparison masking, data held in the selected Mask register determines which bits of the Comparand are compared against the valid contents. During a Write cycle, data in the designated Mask register selects which bits in the destination are written.

The Match line associated with each location is fed into a Priority encoder where multiple responses are resolved and the address of the highest-priority responder (lowest numbered physical address) is generated. In the LAN Bridge application a multiple response might indicate the existence of an error, whereas, in other applications, the existence of multiple responders may be a valid condition.

After a Comparison cycle, the Status register contains the address of the highest-priority responding location, along with flags indicating Match, Multiple Match and Full. The Match and Full flags are also available directly as output signals. These flags can be daisy-chained independently to provide system Match and Full indication without external logic.

A Page Address register simplifies vertical expansion in systems using more than one P1480. This register is loaded with upper-order address information during system initialization. During a Comparison cycle, the lower-order 10 bits of the Match address are fed to the Status register from the Priority encoder and are concatenated with the upper-order address bits from the Page Address register. The Device Select register is used to access a particular device in a vertically cascaded LAN CAM array. The address of the desired device is broadcast to all Device Select registers. Only the device whose Page Address register contains this address will respond to subsequent transactions.

A Control register sets up operating conditions within the P1480, such as Reset, enable or disable Match Flag, enable or disable Full Flag, set default data translation, CAM/RAM partitioning, disable or select masking condition, and disable or select address auto-increment or auto-decrement.

Source and Destination Segment counters within the P1480 control reading and writing 64-bit data. A Segment Control register sets the count limits for the Source and Destination Segment counters, and allows loading of values into each respective counter.

The P1480 is controlled by a combination of hardware signals and instructions loaded into the Instruction register. The instruction set offers a powerful, symmetrical control mechanism for causing the LAN CAM to perform the tasks commonly encountered in LAN Bridges and Routers. To facilitate the repetitive operations that are often desired, several instructions have persistent sources and/or destinations. In this way much of the software overhead that would otherwise be suffered is removed because operations done in a batch can be set up once and left in a given configuration until changed.

Larger LANs are commonly divided into more manageable segments that are joined by a Bridge to prevent excessive local traffic from degrading the overall network performance as shown in Fig.3 below. Segments can all be of the same protocol or can be of mixed protocols. The two major protocols of interest are IEEE 802.3 (Ethernet) and IEEE 802.5 (Token Ring).

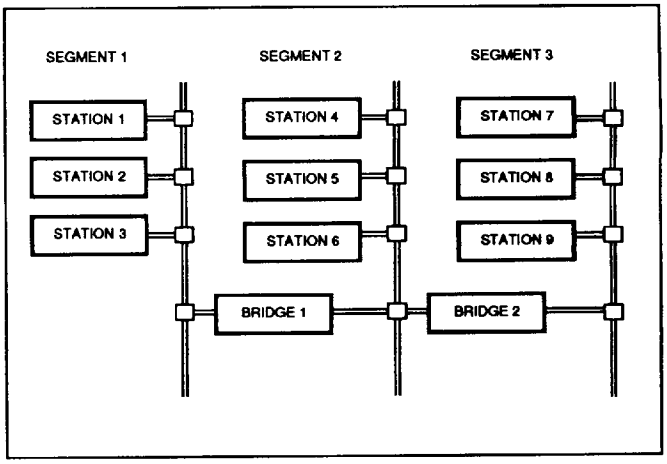


Fig.3 - LAN segments connected by bridges

The Bridge monitors the traffic on all of its segments to determine to which port a particular packet is aimed. This determination requires searching the destination address field (six bytes) in the packet and comparing it to those stored in the station list. A match provides associated information which the Bridge uses to route the packet correctly. A generic block diagram of a Bridge which would utilize one or more LAN CAMs to store and search the station list is shown in Fig.4. Using the LAN CAM radically reduces the search time and improves the Bridge's performance.

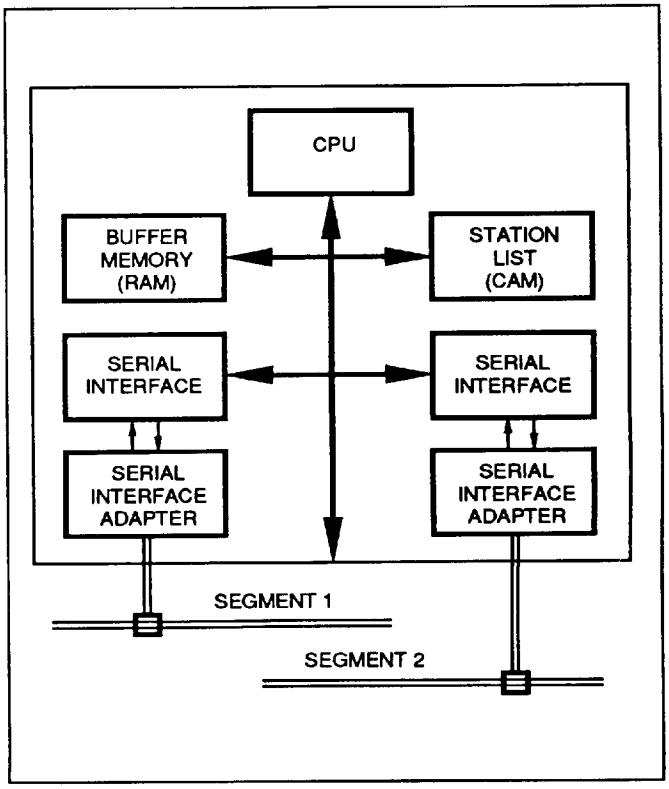


Fig.4 - Generic bridge block diagram

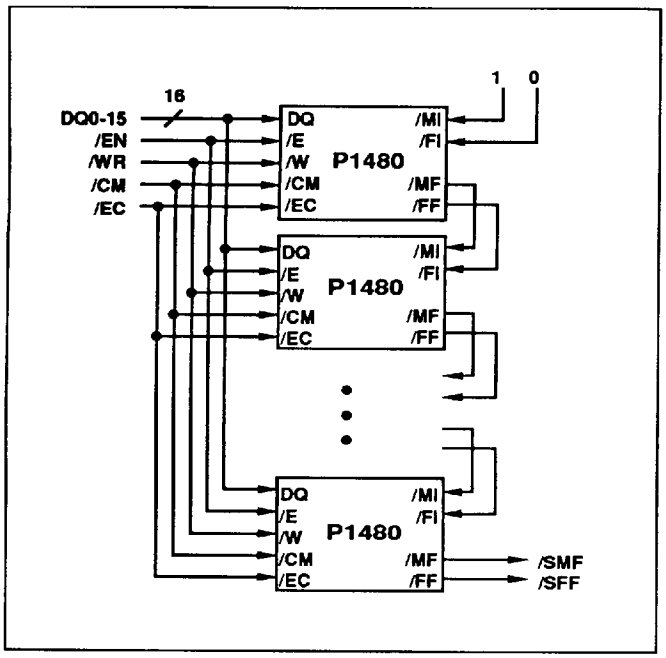


Fig.5 - Vertically cascading the LAN CAM

One P1480 can contain up to 1024 station list entries. For applications that require a larger station list, the LAN CAM is easily cascaded vertically without the need for external logic. Fig.5 below shows the connection scheme. Note that the flags are daisy-chained to generate the system flags without the need for external logic. Further, the Page register facility on the LAN CAM allows each device in the vertically cascaded chain to attach its own address in the event of a match in that device. This feature removes the need to construct an external priority encoder to calculate the complete match address. The fullness indication is also daisy-chained to permit the use of Associative writes which do not require a specific address. The P1480 can be instructed to Write at Next Free Address, even in a cascaded environment.

Table 1 illustrates the flow of a simple Compare operation assuming the LAN CAM is configured as 48 bits of CAM and 16 bits of RAM, any masking on the Compare and the Segment counters is already set up, Associated data is to be read back, and the Match address and the Match flag are to be read back through the Status register (the Associated Data and Status reads are optional and can be in either order). This search operation takes 270 ns to get a hardware flag indication and 450 ns to obtain both a Match address and Associated data, regardless of the length of the Station List. Fig.6 shows the cycle-to-cycle timing with the Match flag valid at the end of the third load cycle if /EC is LOW at the start of the third cycle. The fourth cycle reads status or associated data, depending on the state of /CM.

Duration	Operation	Controls and Flag /W	/CM	/EC	/MF
90ns	Load S1 COMPARAND	L	H	H	H
90ns	Load S2 COMPARAND	L	H	H	H
90ns	Load S3 COMPARAND	L	H	L	L
90ns	Read Associated Data*	H	H	H	H
90ns	Read Status Register*	H	L	H	H
450ns	Total	*sequence is arbitrary			

Table 1 - Station list search flow chart

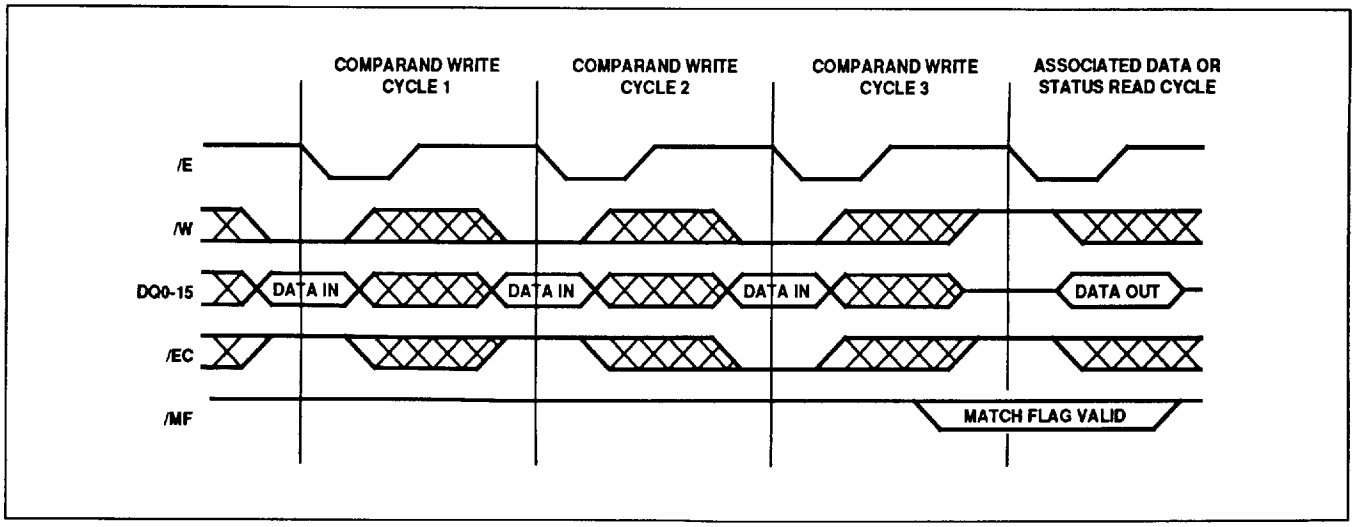


Fig.6 - Cycle-to-cycle timing

INSTRUCTION SET DESCRIPTIONS

A more complete description of the Instruction Set can be obtained in the P1480 LAN CAM Handbook (3113-1.3).

SELECT PERSISTENT SOURCE (SPS)

Binary Op Code	0000 f000 0000 0sss
f	Address Field Flag
sss	Selected Source

The SPS instruction selects a source for Data Reads. After instruction execution, the selected source persistently remains the source for Data Reads until another SPS instruction is executed or until a Reset occurs. The Comparand register is the default persistent source after power up or Reset.

SELECT PERSISTENT DESTINATION (SPD)

Binary Op Code	0000 f001 mmdd dvvv
f	Address Flag
mm	Mask Register Select
ddd	Selected Destination
vvv	Validity Setting if destination is a memory location

The SPD instruction selects a destination for Data Writes. Once this instruction is executed, the selected destination persistently remains the destination for Data Writes until another SPD instruction is executed or until a Reset. The Comparand register is the default destination for Data Writes.

When the selected destination is the Comparand register or the Memory array, the writing of data may be masked by the selected Mask register, Mask Register 1 or Mask Register 2. When the writing of data is masked, only those bits in the destination that correspond to bits containing 0's in the selected Mask register will be modified. Bits in the destination corresponding to bits containing 1's in the selected Mask register will remain unchanged.

Writing to the Comparand register or a Mask register causes a comparison to occur. Writing to the Memory array does not cause a comparison to occur. The next free address is generated when any instruction that could potentially affect the Validity bits is executed.

TEMPORARY COMMAND OVERIDE (TCO)

Binary Op-Code	0000 0010 00dd d000
ddd	Register selected as sourceor destination for only the next Command Read or Write cycle.

When a TCO instruction is executed, the temporarily selected register becomes the source or destination for only the next Command Read or Write cycle, respectively. Once either of those cycles occurs, subsequent Command Read or Write cycles revert to reading the Status register and writing the Instruction register during Command Reads or Writes. The special TCO PS or TCO PD instructions allow the user to read which persistent source or destination has been selected in the next Command Read cycle. If either of these instructions is followed by a Command Write cycle, no actionooccurs. Note that the TCO instruction permits access to the Instruction Address register for diagnostic purposes. Also, the Next Free Address register is Read Only, and Writes to the Page Address register invalidate the contents of the Status register.

DATA MOVE (MOV)

Binary Op-code	0000 f011 mmdd dsss or 0000 f011 mmdd dvss
f	Address Field Flag
mm	Mask Register select
ddd	Destination of Data
sss	Source of Data
v	Validity setting if destination is a memory location

The MOV instruction transfers the data in the selected source to the selected destination. Data transfers between the Memory array and the Comparand register may be masked by the selected Mask register, Mask Register 1 or Mask Register 2. If the transfer is masked, only those bits in the destination which correspond to bits containing 0's in the selected Mask register will be altered. Destination bits which correspond to bits containing 1's in the selected Mask register will remain unchanged.

The Validity bits of a Memory location used as a destination for a MOV instruction will be set to the Valid state or left unchanged, depending on the nature of the operation. If the source and destination are selected to be the same register in register-to-register operations, no net change to the state of the LAN CAM occurs. This operation would be equivalent to a NOOP.

VALIDITY BIT CONTROL (VBC)

Binary Op-code	0000 f100 00dd dvvv
f	Address Field Flag
ddd	Destination of data
vvv	Validity setting for Memory location

The VBC instruction sets the Validity bits to the selected state at the selected Memory location or locations. Validity bits can be accessed randomly or associatively. The VBC instruction can be used in conjunction with the appropriate Compare instruction to compare on any Validity condition. Hence, skipped locations can be returned to the Valid state after processing multiple matches by repeating the Compare operation using the Skip condition as the Validity field search criterion.

COMPARE (CMP)

Binary Op-code	0000 0101 0000 0vvv
vvv	Validity condition

The CMP instruction forces a Comparison after a cycle, such as a Memory Write cycle, which does not automatically result in a Comparison. Destinations to which Write cycles cause an automatic Comparison are the Comparand register, the Mask registers, the Control register.

The CMP E instruction forces the generation of the next free address. The Memory array at the next free address does not need to be a Persistent Destination. The CMP S instruction is used in conjunction with the VBC instruction to return all skipped locations to the Valid state after processing multiple matches. The CMP R instruction permits associative access to any Random-access-only Memory locations.

SET FULL FLAG (SFF)

Binary Op-code 0000 0111 0000 0000

The SFF instruction is a special instruction used to force the Full flag LOW for a device whose /FI input is LOW, but whose /FF output is HIGH. SFF is used in vertically cascaded systems for selecting each device in turn to initialize the Page Address register.

INSTRUCTION SET SUMMARY

MNEMONIC FORMAT: INS dst,src[msk],val

INS: Instruction mnemonic.
dst: Destination of the data.
src: Source of the data.
msk: Mask register used.
val: Validity condition set at the location written.

SELECT PERSISTANT SOURCE

Operation	Mnemonic	Op Code
Comparand Register	SPS CR	0000H
Mask Register 1	SPS MR1	0001H
Mask Register 2	SPS MR2	0002H
Memory Array at Address Reg	SPS M@[AR]	0004H
Memory Array at Address	SPS M@aaaH	0804H
Memory at Highest-priority Match	SPS M@HM	0005H

TEMPORARY COMMAND OVERIDE

Operation	Mnemonic	Op Code
Control Register	TCO CT	0200H
Page Address Register	TCO PA	0208H
Segment Control Register	TCO SC	0210H
Next Free Address Register	TCO NF	0218H
Instruction Address Register	TCO AR	0220H
Device Select Register	TCO DS	0228H
Read Persistent Source	TCO PS	0230H
Read Persistent Destination	TCO PD	0238H

VALIDITY BIT CONTROL

Operation	Mnemonic	Op Code
Set Validity bits at Address Register		
Set Valid	VBC [AR],V	0424H
Set Empty	VBC [AR],E	0425H
Set Skip	VBC [AR],S	0426H
Set Random Access	VBC [AR],R	0427H
Set Validity bits at Address		
Set Valid	VBC aaaH,V	0C24H
Set Empty	VBC aaaH,E	0C25H
Set Skip	VBC aaaH,S	0C26H
Set Random Access	VBC aaaH,R	0C27H
Set Validity bits at Highest-priority Match		
Set Valid	VBC HM,V	042CH
Set Empty	VBC HM,E	042DH
Set Skip	VBC HM,S	042EH
Set Random Access	VBC HM,R	042FH
Set Validity bits at All Matching Locations		
Set Valid	VBC ALM,V	043CH
Set Empty	VBC ALM,E	043DH
Set Skip	VBC ALM,S	043EH
Set Random Access	VBC ALM,R	043FH

SELECT PERSISTANT DESTINATION

Operation	Mnemonic	Op Code
Comparand Register	SPD CR	0100H
Masked by MR1	SPD CR[MR1]	0140H
Masked by MR2	SPD CR[MR2]	0180H
Mask Register 1	SPD MR1	0108H
MaskRegister 2	SPD MR2	0110H
Memory at Address Reg set Valid	SPD M@AR,V	0124H
Masked by MR1	SPD M@AR[MR1],V	0164H
Masked by MR2	SPD M@AR[MR2],V	01A4H
Memory at Address Reg set Empty	SPD M@[AR],E	0125H
Masked by MR1	SPD M@[AR][MR1],E	0165H
Masked by MR2	SPD M@[AR][MR2],E	01A5H
Memory at Address Reg set Skip	SPD M@[AR],S	0126H
Masked by MR1	SPD M@[AR][MR1],S	0166H
Masked by MR2	SPD M@[AR][MR2],S	01A6H
Memory at Address Reg set Random	SPD M@[AR],R	0127H
Masked by MR1	SPD M@[AR][MR1],R	0167H
Masked by MR2	SPD M@[AR][MR2],R	01A7H
Memory at Address set Valid	SPD M@aaaH,V	0924H
Masked by MR1	SPD M@aaaH[MR1],V	0964H
Masked by MR2	SPD M@aaaH[MR2],V	09A4H
Memory at Address set Empty	SPD M@aaaH,E	0925H
Masked by MR1	SPD M@aaaH[MR1],E	0965H
Masked by MR2	SPD M@aaaH[MR2],E	09A5H
Memory at Address set Skip	SPD M@aaaH,S	0926H
Masked by MR1	SPD M@aaaH[MR1],S	0966H
Masked by MR2	SPD M@aaaH[MR2],S	09A6H
Memory at Address set Random	SPD M@aaaH,R	0927H
Masked by MR1	SPD M@aaaH[MR1],R	0967H
Masked by MR2	SPD M@aaaH[MR2],R	09A7H
Memory at Highest-prio. Match,Valid	SPD M@HM,V	012CH
Masked by MR1	SPD M@HM[MR1],V	016CH
Masked by MR2	SPD M@HM[MR2],V	01ACH
Memory at Highest-prio. Match,Emp.	SPD M@HM,E	012DH
Masked by MR1	SPD M@HM[MR1],E	016DH
Masked by MR2	SPD M@HM[MR2],E	01ADH
Memory at Highest-prio. Match, Skip	SPD M@HM,S	012EH
Masked by MR1	SPD M@HM[MR1],S	016EH
Masked by MR2	SPD M@HM[MR2],S	01AEH
Memory at High-prio. Match, Random	SPD M@HM,R	012FH
Masked by MR1	SPD M@HM[MR1],R	016FH
Masked by MR2	SPD M@HM[MR2],R	01AFH
Memory at Next Free Addr., Valid	SPD M@NF,V	0134H
Masked by MR1	SPD M@NF[MR1],V	0174H
Masked by MR2	SPD M@NF[MR2],V	01B4H
Memory at Next Free Addr.,Empty	SPD M@NF,E	0135H
Masked by MR1	SPD M@NF[MR1],E	0175H
Masked by MR2	SPD M@NF[MR2],E	01B5H
Memory at Next Free Addr., Skip	SPD M@NF,S	0136H
Masked by MR1	SPD M@NF[MR1],S	0176H
Masked by MR2	SPD M@NF[MR2],S	01B6H
Memory at Next Free Addr., Random	SPD M@NF,R	0137H
Masked by MR1	SPD M@NF[MR1],R	0177H
Masked by MR2	SPD M@NF[MR2],R	01B7H

DATA MOVE

Operation	Mnemonic	Op Code
Comparand Register from:		
No Operation	NOP	0300H
Mask Register 1	MOV CR,MR1	0301H
Mask Register 2	MOV CR,MR2	0302H
Memory at Address Reg	MOV CR,[AR]	0304H
Masked by MR1	MOV CR,[AR][MR1]	0344H
Masked by MR2	MOV CR,[AR][MR2]	0384H
Memory at Address	MOV CR,aaaH	0B04H
Masked by MR1	MOV CR,aaaH[MR1]	0B44H
Masked by MR2	MOV CR,aaaH[MR2]	0B84H
Memory at Highest-prio Match	MOV CR,HM	0305H
Masked by MR1	MOV CR,HM[MR1]	0345H
Masked by MR2	MOV CR,HM[MR2]	0385H
Mask Register 1 from:		
Comparand Register	MOV MR1,CR	0308H
No Operation	NOP	0309H
Mask Register 2	MOV MR1,MR2	030AH
Memory at Address Reg	MOV MR1,[AR]	030CH
Memory at Address	MOV MR1,aaaH	0B0CH
Memory at Highest-prio Match	MOV MR1,HP	030DH
Mask Register 2 from:		
Comparand Register	MOV MR2,CR	0310H
Mask Register 1	MOV MR2,MR1	0311H
No Operation	NOP	0312H
Memory at Address Reg	MOV MR2,[AR]	0314H
Memory at Address	MOV MR2,aaaH	0B14H
Memory at Highest-prio Match	MOV MR2,HP	0315H
Memory at Address Register, No Change to Validity bits, from:		
Comparand Register	MOV [AR],CR	0320H
Masked by MR1	MOV [AR],CR[MR1]	0360H
Masked by MR2	MOV [AR],CR[MR2]	03A0H
Mask Register 1	MOV [AR],MR1	0321H
Mask Register 2	MOV [AR],MR2	0322H
Memory at Address Register, Location set Valid, from:		
Comparand Register	MOV [AR],CR,V	0324H
Masked by MR1	MOV [AR],CR[MR1],V	0364H
Masked by MR2	MOV [AR],CR[MR2],V	03A4H
Mask Register 1	MOV [AR],MR1,V	0325H
Mask Register 2	MOV [AR],MR2,V	0326H
Memory at Address, No Change to Validity bits, from:		
Comparand Register	MOV aaaH,CR	0B20H
Masked by MR1	MOV aaaH,CR[MR1]	0B60H
Masked by MR2	MOV aaaH,CR[MR2]	0BA0H
Mask Register 1	MOV aaaH,MR1	0B21H
Mask Register 2	MOV aaaH,MR2	0B22H
Memory at Address, Location set Valid, from:		
Comparand Register	MOV aaaH,CR,V	0B24H
Masked by MR1	MOV aaaH,CR[MR1],V	0B64H
Masked by MR2	MOV aaaH,CR[MR2],V	0BA4H
Mask Register 1	MOV aaaH,MR1,V	0B25H
Mask Register 2	MOV aaaH,MR2,V	0B26H

DATA MOVE (continued)

Operation	Mnemonic	Op Code
Memory at Highest-priority Match, No Change to Validity bits, from:		
Comparand Register	MOV HM,CR	0328H
Masked by MR1	MOV HM,CR[MR1]	0368H
Masked by MR2	MOV HM,CR[MR2]	03A8H
Mask Register 1	MOV HM,MR1	0329H
Mask Register 2	MOV HM,MR2	032AH
Memory at Highest-priority Match, Location set Valid, from:		
Comparand Register	MOV HM,CR,V	032CH
Masked by MR1	MOV HM,CR[MR1],V	036CH
Masked by MR2	MOV HM,CR[MR2],V	03ACH
Mask Register 1	MOV HM,MR1,V	032DH
Mask Register 2	MOV HM,MR2,V	032EH
Memory at Next Free Address, No Change to Validity bits, from:		
Comparand Register	MOV NF,CR	0330H
Masked by MR1	MOV NF,CR[MR1]	0370H
Masked by MR2	MOV NF,CR[MR2]	03B0H
Mask Register 1	MOV NF,MR1	0331H
Mask Register 2	MOV NF,MR2	0332H
Memory at Next Free Address, Location set Valid, from:		
Comparand Register	MOV NF,CR,V	0334H
Masked by MR1	MOV NF,CR[MR1],V	0374H
Masked by MR2	MOV NF,CR[MR2],V	03B4H
Mask Register 1	MOV NF,MR1,V	0335H
Mask Register 2	MOV NF,MR2,V	0336H

COMPARE

Operation	Mnemonic	Op Code
Compare Valid Locations	CMP V	0504H
Compare Empty Locations	CMP E	0505H
Compare Skipped Locations	CMP S	0506H
Compare Random Access Locations	CMP R	0507H

SPECIAL INSTRUCTIONS

Operation	Mnemonic	Op Code
Set Full Flag	SFF	0700H

SWITCHING CHARACTERISTICS

Note 4 (using AC test conditions)

No.	Symbol	Parameter	-120		-150		Units	Notes
			Min	Max	Min	Max		
1	tELE	Compare Cycle Time	120		150		ns	
2	tELEH	Chip Enable LOW Compare Pulse Width	100		120		ns	
3	tEHEL	Chip Enable High Pulse Width	20		30		ns	
4	tWHEL	Write Enable HIGH to Chip Enable LOW	0		0		ns	
5	tELWX1	Chip Enable LOW to Write Don't Care	15		15		ns	
6	tWLEL	Write LOW to Chip Enable Low	0		0		ns	
7	tELWX2	Chip Enable LOW to Write Don't Care	15		15		ns	
8	tCMVEL	Command Valid to Chip Enable LOW	0		0		ns	
9	tELCMX	Chip Enable LOW to Command Don't Care	15		15		ns	
10	tECVEL	Enable Comparison Valid to Chip Enable LOW	0		0		ns	
11	tELECX1	Chip Enable LOW to Enable Compare Don't Care	15		15		ns	
12	tELQX	Chip Enable LOW to Outputs Active	3		3		ns	2
13	tELQV	Chip Enable LOW to Data Valid		85		105	ns	2
14	tELQZ	Chip Enable HIGH to Outputs High-Z	3	20	3	25	ns	3
15	tDVEL	Data Valid to Chip Enable LOW	0		0		ns	
16	tELDX	Chip Enable LOW to Data Don't Care	15		15		ns	
17	tELFFV	Chip Enable LOW to Full Flag Valid		90		110	ns	
18	tFIVFFV	Full Input Valid to Full Flag Valid		7		7	ns	
19	tWVEL	Write Valid to Chip Enable LOW	0		0		ns	
20	tELWX3	Chip Enable LOW to Write Don't Care	15		15		ns	
21	tECLEL	Comparison Enable LOW to Chip Enable LOW	0		0		ns	
22	tELECX2	Chip Enable LOW to Enable Compare Don't Care	15		15		ns	
23	tEHMFV	Chip Enable HIGH to Match Flag Valid		30		35	ns	
24	tMIVMFV	Match in Valid to Match Flag Valid		7		7	ns	
25	tEHMFX	Chip Enable HIGH to Match Flag Invalid	0		0		ns	
26	tELELRW	Read/Write Cycle Time	95		105		ns	
27	tELEHRW	Chip Enable LOW Read/Write Pulse Width LOW	75		75		ns	

Notes:
1. Common I/O lines are clamped, so that signal transients cannot fall below -0.5V.
2. With load specified in Fig.7.
3. With load specified in Fig.8.
4. Over the operating temperature and voltage ranges.

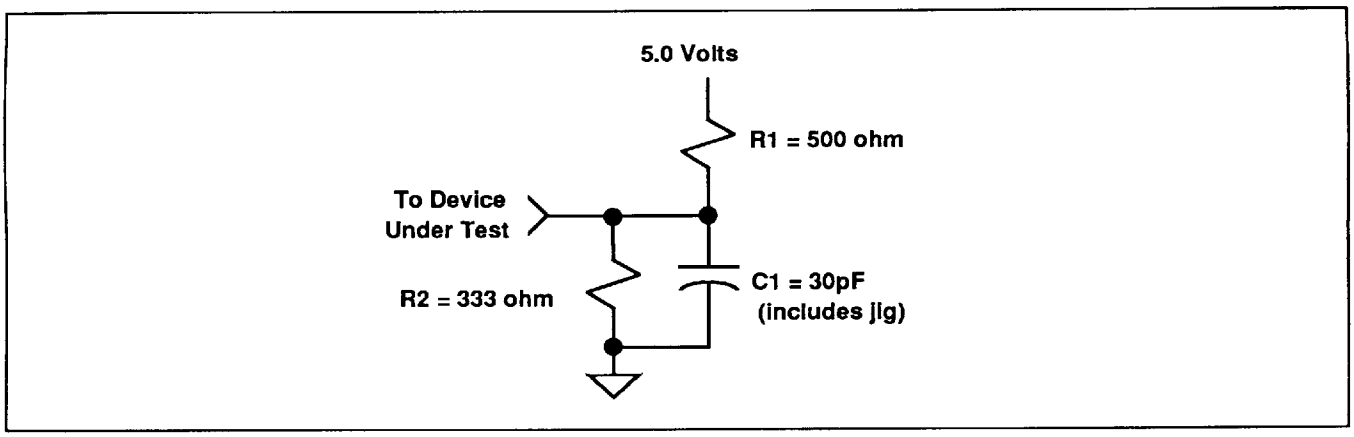


Fig.7 - AC test load

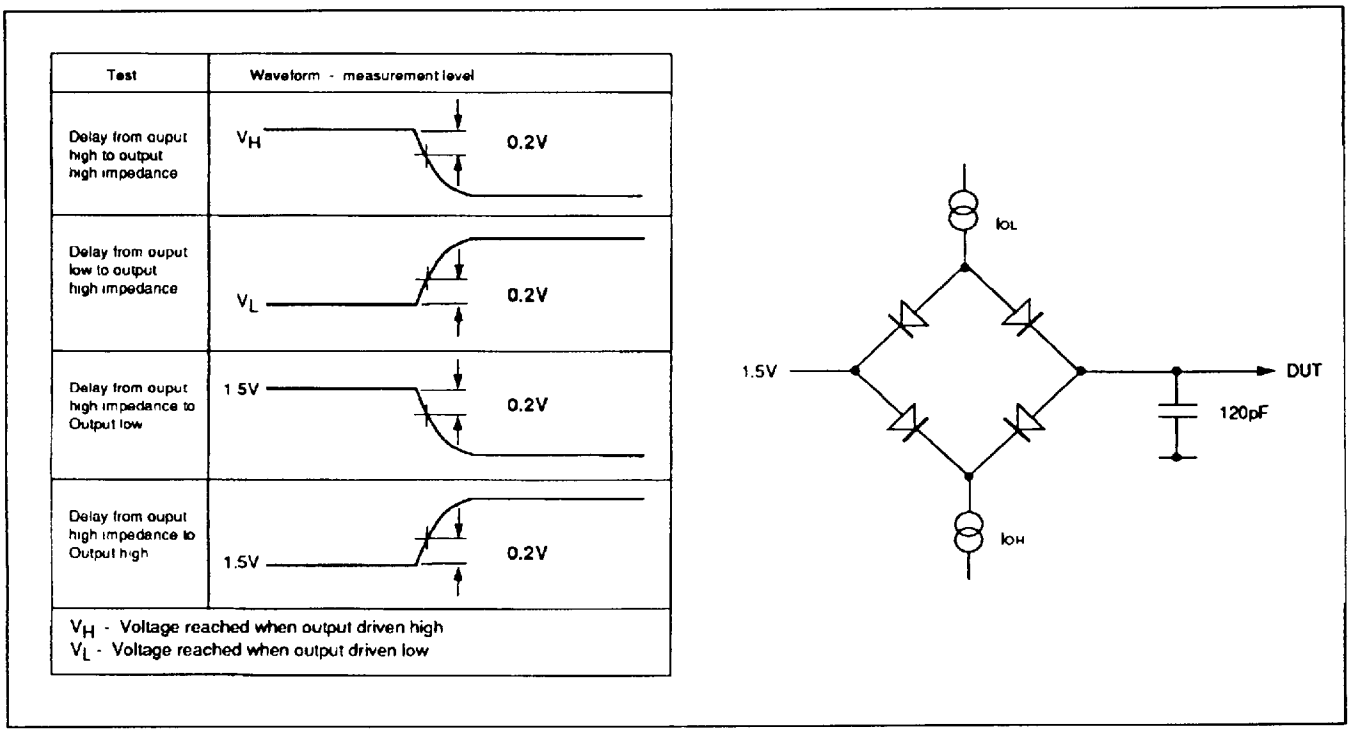


Fig.8 - Three state delay measurement

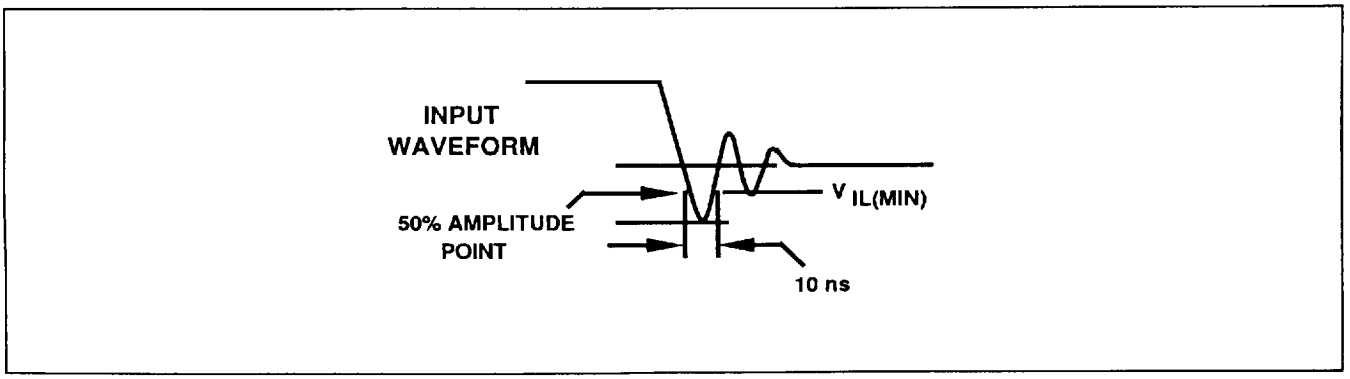


Fig.9 - Input signal waveform

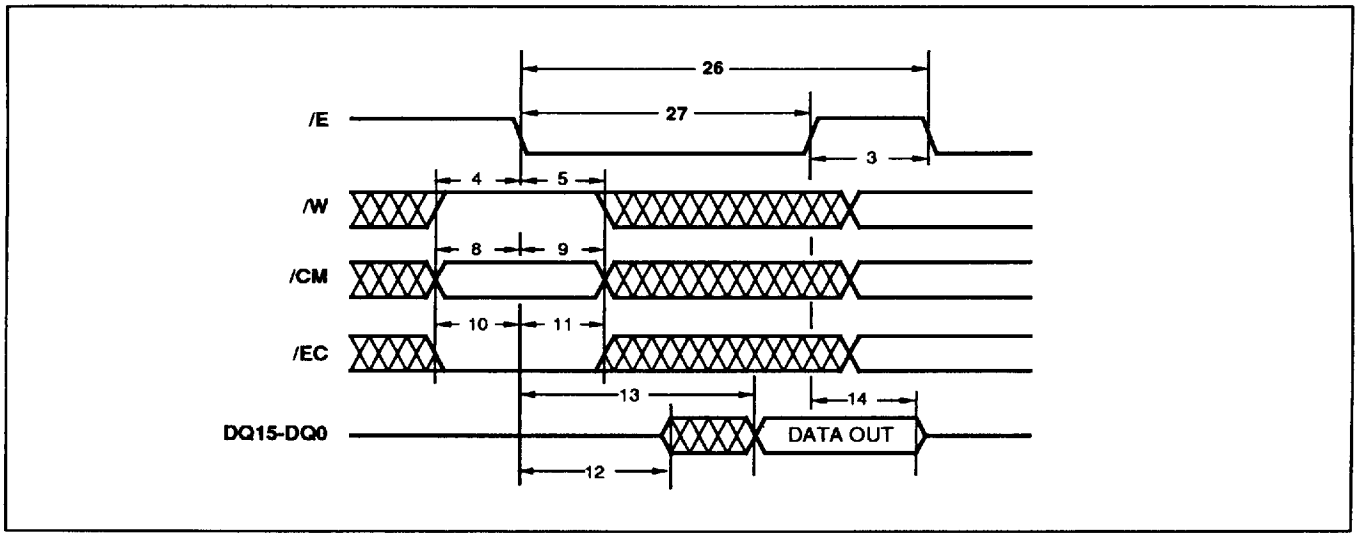


Fig.10 P1480 read cycle

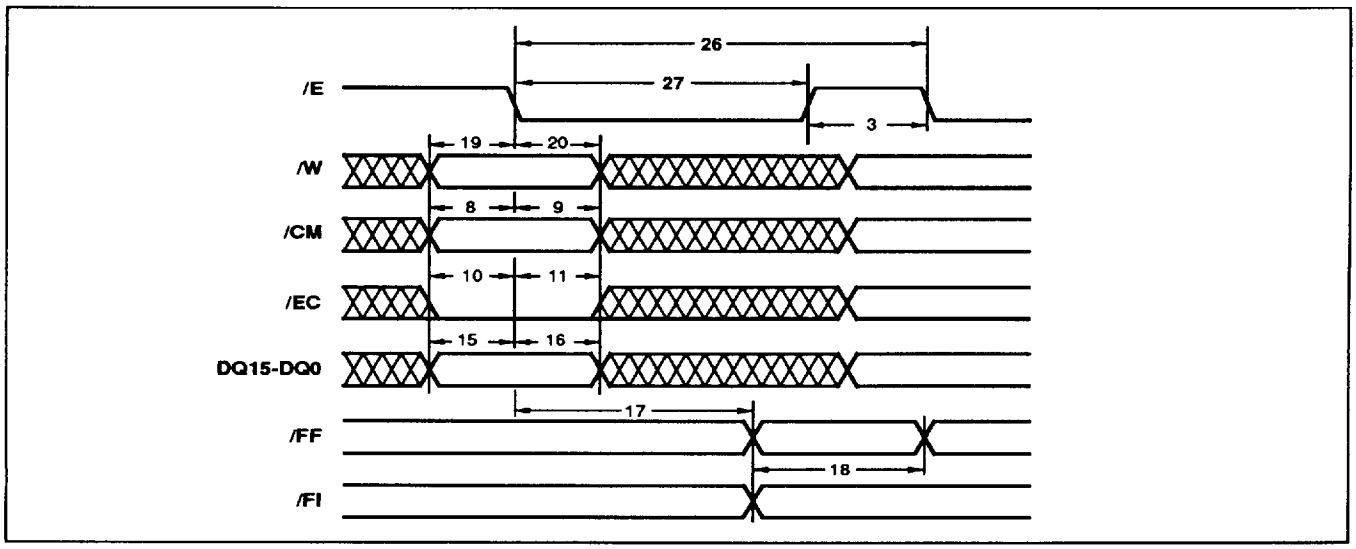


Fig.11 P1480 write cycle

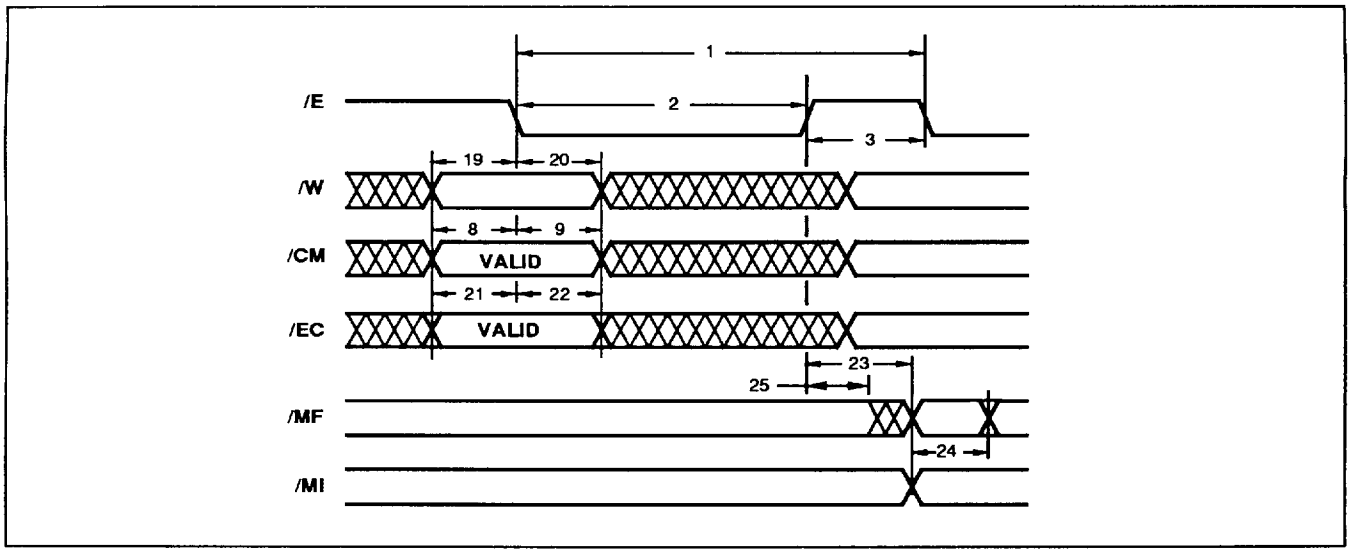
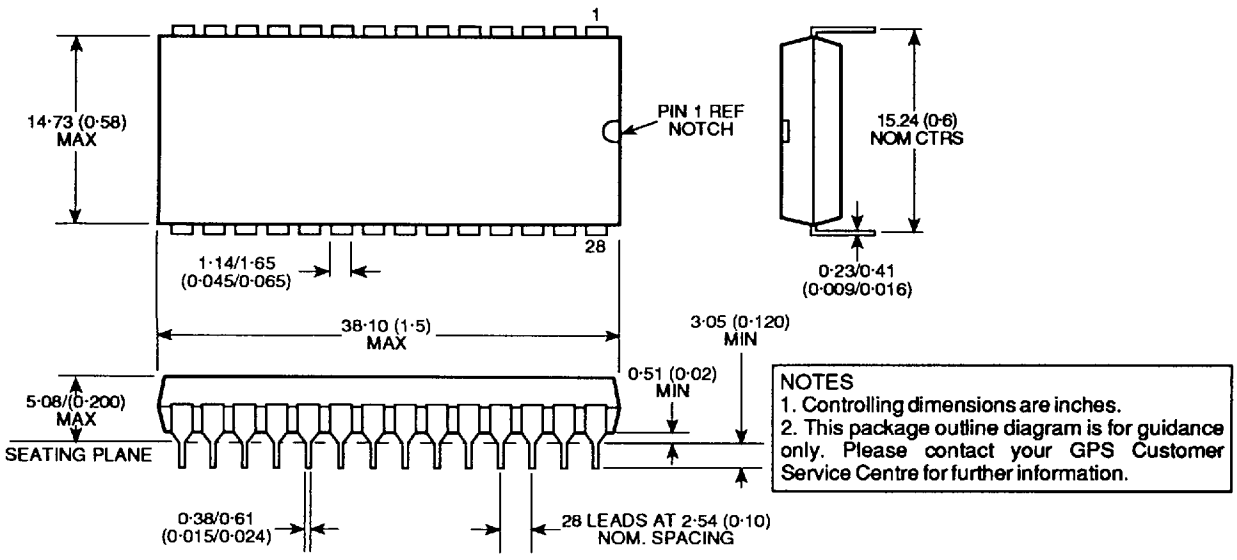


Fig.12 P1480 match flag response

PACKAGE DETAILS

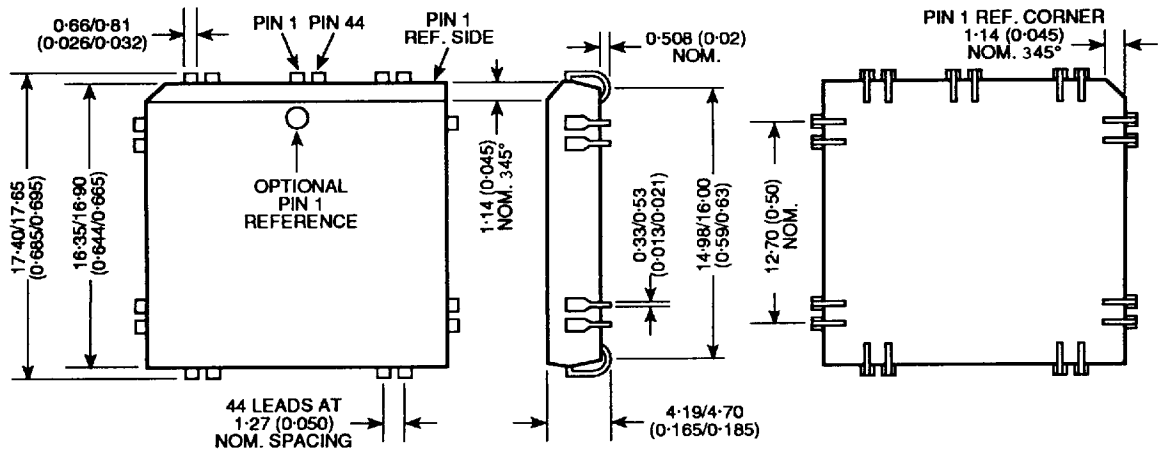
Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



28-LEAD PLASTIC DIL – DP28

PACKAGE DETAILS (Cont.)

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

44-LEAD QUAD PLASTIC J-LEAD – HP44

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