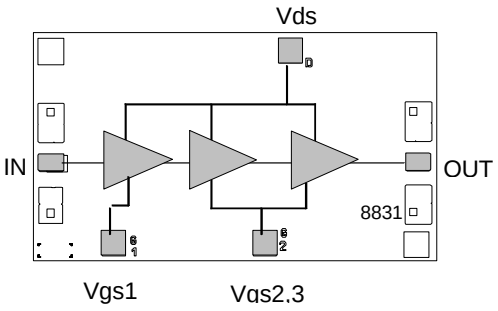
# 18-32GHz Low Noise Amplifier

## GaAs Monolithic Microwave IC

## Description

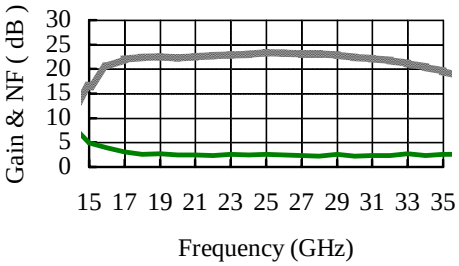
The CHA2092 is a high gain broadband three-stage monolithic low noise amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC ground. This helps simplify the assembly process. Self biasing technique is implemented on chip to ease the circuit biasing.

The circuit is manufactured with a P-HEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.




## Main Features

- Broadband performances : 18-32GHz
- 2.5dB Noise Figure
- 10dBm output power ( -1dB gain comp. )
- 22dB ±1.0dB gain
- Low DC power consumption, 60mA @ 3.5V
- Chip size : 1.67 X 0.97 X 0.10 mm




## Main Characteristics

Tamb. = 25°C

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Fop | Operating frequency range | 18 | | 32 | GHz |
| G | Small signal gain | 17 | 22 | | dB |
| NF | Noise figure (20-32GHz) | | 2.5 | 3.5 | dB |
| P1dB | Output power at 1dB gain compression | 8 | 10 | | dBm |
| Id | Bias current | | 60 | 100 | mA |

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !



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## Electrical Characteristics

Tamb = +25°C, Vds = 3.5V; Ids=60mA

| Symbol | Parameter | Min | Typ | Max | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Fop | Operating frequency range (1) | 20 | | 28 | 18 | | 32 | GHz |
| G | Small signal gain (1) | 18 | 22 | | 17 | 22 | | dB |
| ΔG | Small signal gain flatness (1) | | ±1.5 | | | ±2.5 | | dB |
| ΔGsb | Gain flatness over 40MHz | | | 0.5 | | | 0.5 | dBpp |
| Is | Reverse isolation (1) | 25 | 30 | | 25 | 30 | | dB |
| P1dB | Output power at 1dB gain compression (3) | 8 | 10 | | 8 | 10 | | dBm |
| VSWRin | Input VSWR (1) | | 2.5:1 | 3.0:1 | | 2.5:1 | 3.5:1 | |
| VSWRout | Output VSWR (1) | | 2.5:1 | 3.0:1 | | 2.5:1 | 3.5:1 | |
| NF | Noise figure (2) 18-20GHz<br>20-28GHz<br>28-32GHz | | 2.5 | 3.5 | | 2.5<br>2.5<br>2.5 | 4<br>3.5<br>3.5 | dB |
| Vd | DC Voltage Vd<br>Vgs1,Vgs2&3 | | 3.5<br>-0.5 | 4.5 | | 3.5<br>-0.5 | 4.5 | V<br>V |
| Id | Bias current (2) | | 60 | 100 | | 60 | 100 | mA |

(1)These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.
(2) 60 mA is the typical bias current used for on wafer measurements, with Vgs1 and Vgs2&3 connected together. For optimum noise figure, the bias current could be reduced down to 50 mA, adjusting the Vgs1 voltage.
(3) Ids=90mA

## Absolute Maximum Ratings

Tamb. = 25°C (1)

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| Vd | Drain bias voltage | 5.0 | V |
| Id | Drain bias current | 120 | mA |
| Vg | Gate bias voltage | -2.0 to +0.4 | V |
| Pin | Maximum peak input power overdrive (2) | +15 | dBm |
| Ta | Operating temperature range | -40 to +85 | °C |
| Tstg | Storage temperature range | -55 to +155 | °C |

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.



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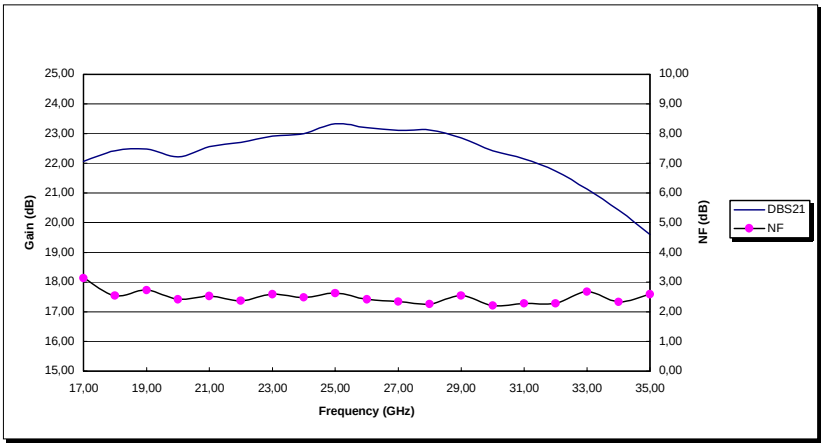
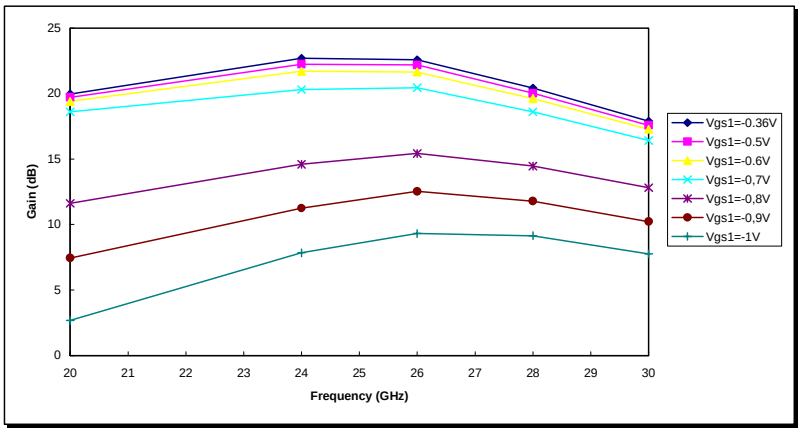
## Typical Results

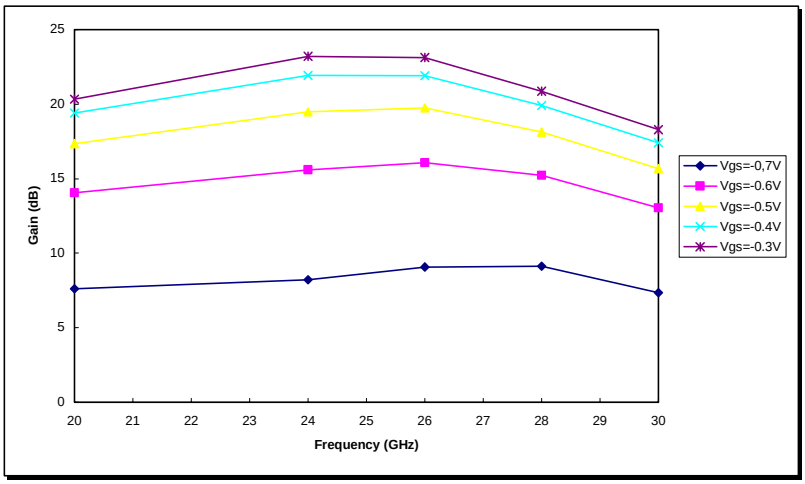
Tamb=25°C




Gain and NF vs Frequency (Vdd=3.5V; Ids=60mA)




Gain vs Frequency and Vgs1 (Vdd=3.5V; Vgs23=-0.3V)



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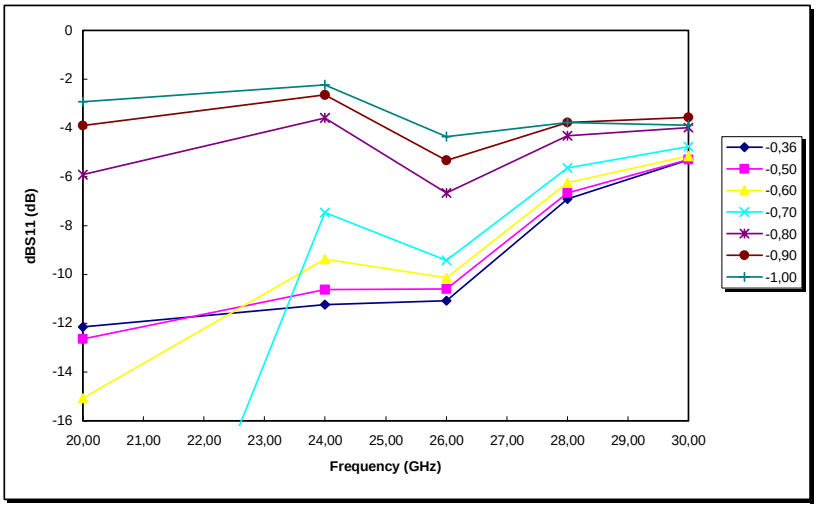
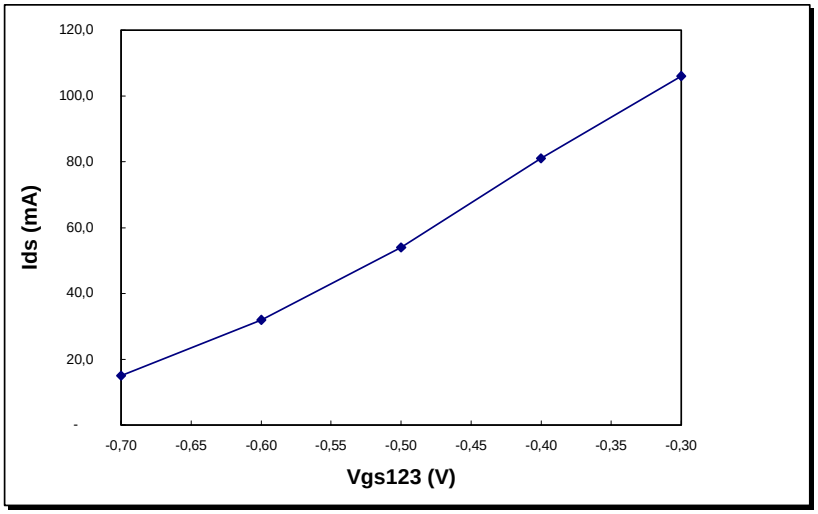
Gain vs Frequency and Vgs123 (Vdd=3.5V)




dBS11 vs Frequency and Vgs1 (Vdd=3.5V; Vgs23=-0.3V)




Ids vs Vgs123 (Vdd=3.5V)



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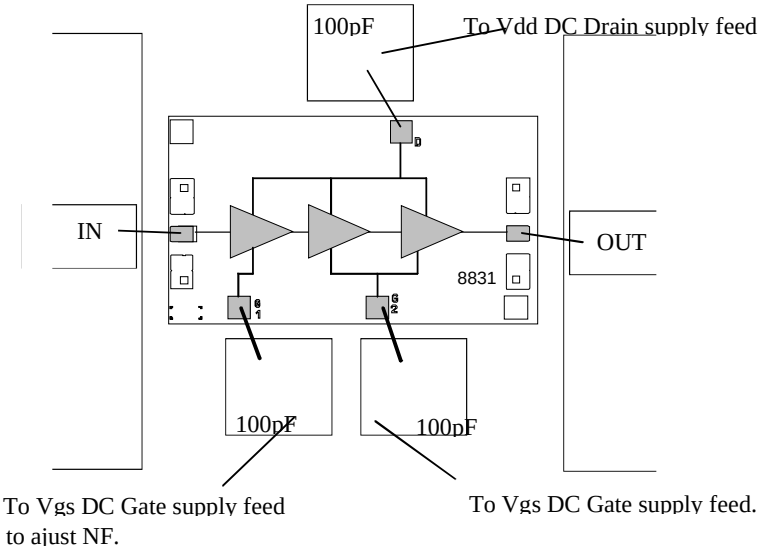
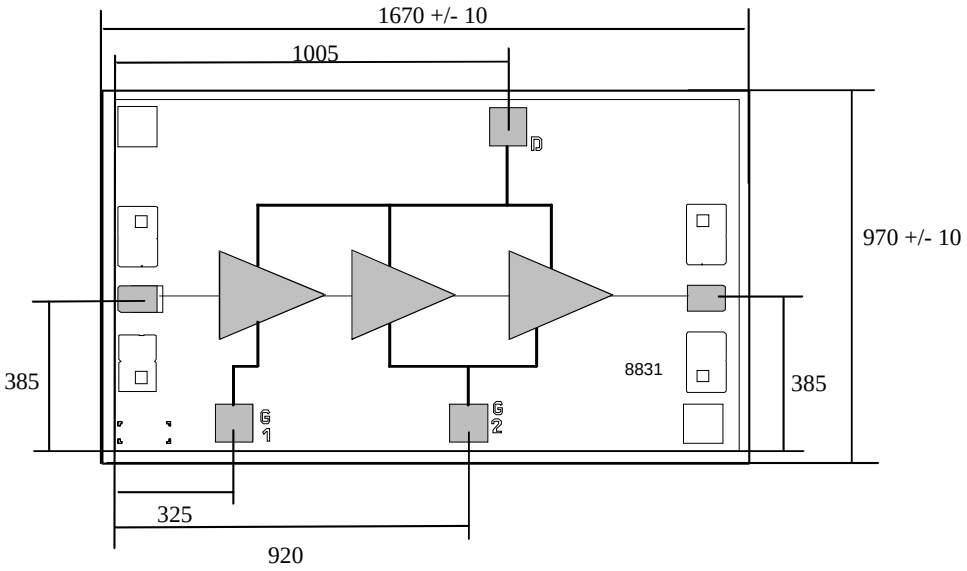
## Chip Assembly and Mechanical Data




Note : Supply feed should be capacitively bypassed.




**Bonding pad positions.**

( Chip thickness : 100µm. All dimensions are in micrometers )



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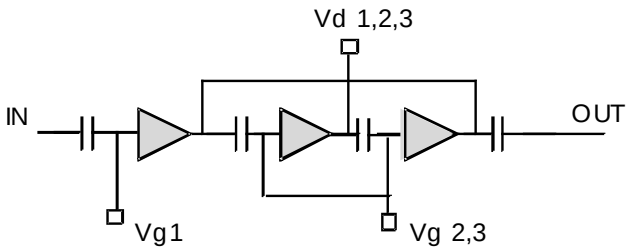
## Typical Bias Tuning

The circuit schematic is given below :




The three drain biases are connected altogether on chip. For typical operation, all the gate biases are connected together at the same power supply, tuned to drive a small signal operating current of 60 mA. A separate access to the gate voltages of the first stage ( Vg1 ) and the second and third stages ( Vgs2,3 ) is provided for the fine tuning of the amplifier regarding the application.

## Ordering Information

Chip form : CHA2092b99F/00





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