Dual 4MHz, 3A Synchronous Step-Down DC/DC Converter

FEATURES

- **High Efficiency: Up to 94%**
- **Dual Outputs with 2 × 3A Output Current Capability**
- **Low Output Ripple Burst Mode® Operation: I_Q = 130µA**
- **2.25V to 5.5V Input Voltage Range**
- **±1% Output Voltage Accuracy**
- **Output Voltages Down to 0.6V**
- Programmable Slew Rate at Switch Pins
- Low Dropout Operation: 100% Duty Cycle
- Shutdown Current ≤1µA
- Adjustable Switching Frequency Up to 4MHz
- Internal or External Compensation
- Selectable Pulse-Skipping/Forced Continuous/ Burst Mode Operation with Adjustable Burst Clamp
- Optional Active Voltage Positioning (AVP) with Internal Compensation
- Selectable 0°/90°/180° Phase Shift Between Channels
- Fixed Internal and Programmable External Soft-Start
- Accurate Start-Up Tracking Capability
- DDR Memory Mode I_{OUT} = ±1.5A
- Available in 4mm × 4mm QFN-24 and TSSOP-24 Packages

APPLICATIONS

- Point-of-Load Supplies
- Distributed Power Supplies
- Portable Computer Systems
- DDR Memory Termination
- Handheld Devices

DESCRIPTION

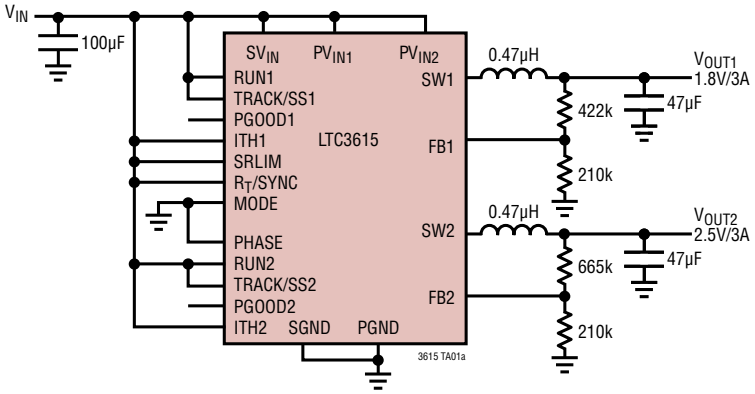
The LTC®3615 is a dual 3A synchronous step-down regulator using a current mode, constant-frequency architecture. The DC supply current is only 130µA (Burst Mode operation at no-load) while maintaining the output voltages, dropping to zero current in shutdown. The 2.25V to 5.5V input supply range makes the LTC3615 ideally suited for single Li-Ion applications. 100% duty cycle capability provides low dropout operation, which extends operating time in battery-operated systems.

The operating frequency is externally programmable up to 4MHz, allowing the use of small surface mount inductors. 0°, 90°, or 180° of phase shift between the two channels can be selected to minimize input current ripple and output voltage ripple in a single 6A output configuration. Programmable slew rate limiting reduces EMI, and external synchronization can be applied up to 4MHz.

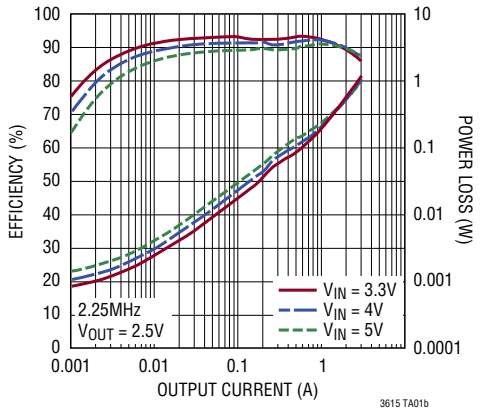
The internal synchronous switches increase efficiency and eliminate the need for external catch diodes, saving external components and board space.

The LTC3615 is offered in leadless 24-pin 4mm × 4mm QFN and thermally enhanced 24-pin TSSOP packages.

TYPICAL APPLICATION



Efficiency and Power Loss vs Load Current

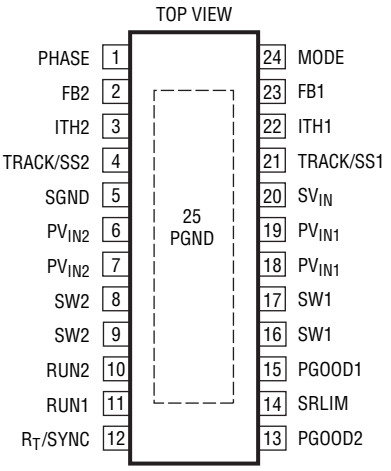


ABSOLUTE MAXIMUM RATINGS (Note 1)

PV_{IN1}, PV_{IN2} Voltages.....–0.3V to SV_{IN} + 0.3V
SV_{IN} Voltage.....–0.3V to 6V
SW1 Voltage .....–0.3V to (PV_{IN1} + 0.3V)
SW2 Voltage .....–0.3V to (PV_{IN2} + 0.3V)
PGOOD1, PGOOD2 Voltages .....–0.3V to 6V
All Other Pins.....–0.3V to (SV_{IN} + 0.3V)

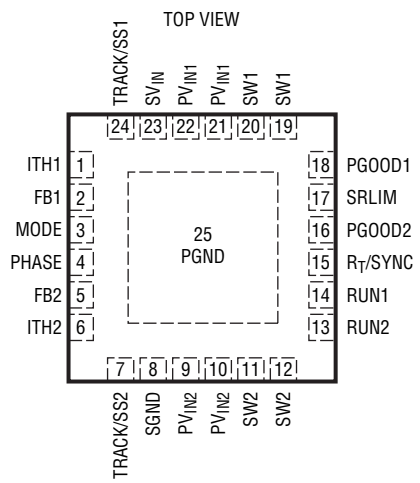
Operating Junction Temperature
Range (Note 2).....–40°C to 125°C
Storage Temperature.....–65°C to 150°C
Lead Soldering Temperature (TSSOP) .....300°C
Reflow Peak Body Temperature (QFN) .....260°C

PIN CONFIGURATION



FE PACKAGE
24-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 33°C/W
EXPOSED PAD (PIN 25) IS PGND, MUST BE SOLDERED TO PCB



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 25) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3615EFE#PBF	LTC3615EFE#TRPBF	LTC3615FE	24-Lead Plastic TSSOP	–40°C to 125°C
LTC3615IFE#PBF	LTC3615IFE#TRPBF	LTC3615FE	24-Lead Plastic TSSOP	–40°C to 125°C
LTC3615EUF#PBF	LTC3615EUF#TRPBF	3615	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3615IUF#PBF	LTC3615IUF#TRPBF	3615	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), SV_{IN} = PV_{INx} = 3.3V, R_T = 178k, R_{SRLIM} = 40.2k, unless otherwise specified (Notes 1, 2, 11).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range		●	2.25		5.5	V
V_{UVLO}	Undervoltage Lockout Threshold	SV_{IN} Ramping Down	●	1.7			V
		SV_{IN} Ramping Up				2.25	V
V_{FB}	Feedback Voltage Internal Reference	(Note 3) V_{TRACK} = SV_{IN}, V_{SRLIM} = 0V 0°C < T_J < 85°C –40°C < T_J < 125°C	 ●	 0.592 0.590	 0.6	 0.608 0.610	 V V
	Feedback Voltage External Reference (Note 7)	(Note 3) V_{TRACK} = 0.3V, V_{SRLIM} = SV_{IN}		0.289	0.3	0.311	V
		(Note 3) V_{TRACK} = 0.5V, V_{SRLIM} = SV_{IN}		0.489	0.5	0.511	V
I_{FB}	Feedback Input Current	V_{FBx} = 0.6V	●		0	±30	nA
$\Delta V_{LINEREG}$	Line Regulation	SV_{IN} = PV_{INx} = 2.25V to 5.5V (Note 4)	●			0.2	%/V
$\Delta V_{LOADREG}$	Load Regulation	V_{ITHx} from 0.5V to 0.9V (Note 4) V_{ITHx} = SV_{IN}, V_{FBx} = 0.6V (Note 5)				0.2 2	% %
I_S	Active Mode	V_{FB1} = 0.5V, V_{MODE} = SV_{IN}, V_{RUN2} = 0V (Note 6)			1100		µA
		V_{FBx} = 0.5V, V_{MODE} = SV_{IN}, V_{RUNx} = SV_{IN} (Note 6)			1900		µA
	Sleep Mode	V_{FB1} = 0.7V, V_{RUN1} = SV_{IN}, V_{RUN2} = 0V, V_{MODE} = 0V, V_{ITH1} = SV_{IN} (Note 5)			95	130	µA
		V_{FBx} = 0.7V, V_{RUN1} = SV_{IN}, V_{RUN2} = 0V, V_{MODE} = 0V (Note 4)			145	220	µA
		V_{FBx} = 0.7V, V_{RUNx} = SV_{IN}, V_{MODE} =0V, V_{ITHx} = SV_{IN} (Note 5)			130	200	µA
		V_{FBx} = 0.7V, V_{RUNx} = SV_{IN}, V_{MODE} =0V, I_{TH} = (Note 4)			240	360	µA
	Shutdown	SV_{IN} = PV_{IN} = 5.5V, V_{RUNx} = 0V			0.1	1	µA
$R_{DS(ON)}$	Top Switch On-Resistance	PV_{INx} = 3.3V (Note 10)			75		mΩ
	Bottom Switch On-Resistance	PV_{INx} = 3.3V (Note 10)			55		mΩ
I_{LIM}	Top Switch Current Limit	Sourcing (Note 8), V_{FB} = 0.5V Duty Cycle <35% Duty Cycle = 100%		 4.5 3.6	 6	 7.5	 A A
	Bottom Switch Current Limit	Sinking (Note 8), V_{FB} = 0.7V, Forced Continuous Mode		–2.5	–3.5	–5	A
$I_{SW(LKG)}$	Switch Leakage Current	SV_{IN} = PV_{IN} = 5.5V, V_{RUNx} = 0V			0.01	1	µA
$g_{m(EA)}$	Error Amplifier Transconductance	–5µA < I_{TH} < 5µA			240		µmho
I_{EAO}	Error Amplifier Output Current	(Note 4)			±30		µA
$t_{SOFT-START}$	Internal Soft-Start Time	V_{FBx} from 0.06V to 0.54V, TRACK/SSx = SV_{IN}		0.65	1.1	1.7	ms
$R_{ON(TRACK/SS\_DIS)}$	TRACK/SS Pull-Down Resistance at Start-Up					200	Ω
t_{TRACK/SS_DIS}	Soft-Start Discharge Time at Start-Up			70			µs
f_{OSC}	Internal Oscillator Frequency	$R_{RT/SYNC}$ = 178k	●	1.85	2.25	2.65	MHz
		$V_{RT/SYNC}$ = SV_{IN}	●	1.8	2.25	2.7	MHz
f_{SYNC}	Synchronization Frequency	t_{LOW}, t_{HIGH} > 30ns		0.4		4	MHz
$V_{RT/SYNC}$	SYNC Level High			1.2			V
	SYNC Level Low					0.3	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), SV_{IN} = PV_{INx} = 3.3V, R_T = 178k, R_{SRLIM} = 40.2k, unless otherwise specified (Notes 1, 2, 11).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\varphi_{SW1-SW2}$	Output Phase Shift Between SW1 and SW2	V_{PHASE} < 0.15 • SV_{IN}			0		Deg
		0.35 • SV_{IN} < V_{PHASE} < 0.65 • SV_{IN}			90		Deg
		V_{PHASE} > 0.85 • SV_{IN}			180		Deg
V_{SRLIM}	Voltage at SRLIM to Enable DDR Mode	(Note 9)		SV_{IN} – 0.3			V
V_{MODE} (Note 9)	Internal Burst Mode Operation					0.3	V
	Pulse-Skipping Mode			SV_{IN} – 0.3			V
	Forced Continuous Mode			1.1		SV_{IN} • 0.58	V
	External Burst Mode Operation			0.5		0.85	V
PGOOD	Power Good Voltage Windows	TRACK/SSx = SV_{IN}, Entering Window V_{FBx} Ramping Up V_{FBx} Ramping Down		 –3.5 3.5	 –6 6		 % %
		TRACK/SSx = SV_{IN}, Leaving Window V_{FBx} Ramping Up V_{FBx} Ramping Down			 9 –9	 11 –11	 % %
t_{PGOOD}	Power Good Blanking Time	Entering/Leaving Window		70	105	140	µs
R_{PGOOD}	Power Good Pull-Down On-Resistance	I = 10mA		8	12	30	Ω
V_{RUN}	Enable Pin	Input High Input Low	● ●	1		 0.4	V V
		Pull-Down Resistance			4		MΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3615 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3615E is guaranteed to meet performance specifications over the 0°C to 85°C operating junction temperature range. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3615I is guaranteed to meet specifications over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedence.

Note 3: This parameter is tested in a feedback loop which servos $V_{FB1,2}$ to the midpoint for the error amplifier ($V_{ITH1,2}$ = 0.75V).

Note 4: External compensation on ITH pin.

Note 5: Tying the ITH pin to SV_{IN} enables internal compensation and AVP mode for the selected channel.

Note 6: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 7: See description of the TRACK/SS pin in the Pin Functions section.

Note 8: When sourcing current, the average output current is defined as flowing out of the SW pin. When sinking current, the average output current is defined as flowing into the SW pin. Sinking mode requires the use of forced continuous mode.

Note 9: See description of the MODE pin in the Pin Functions section.

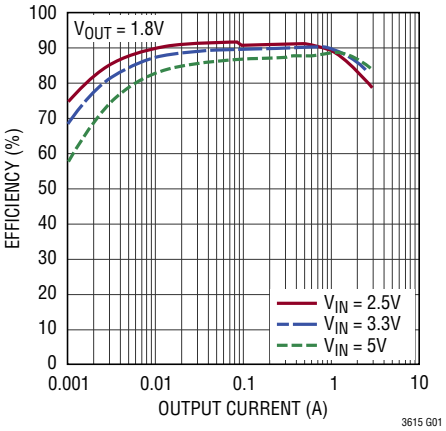
Note 10: Guaranteed by design and correlation to wafer level measurements for QFN packages.

Note 11: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability or permanently damage the device.

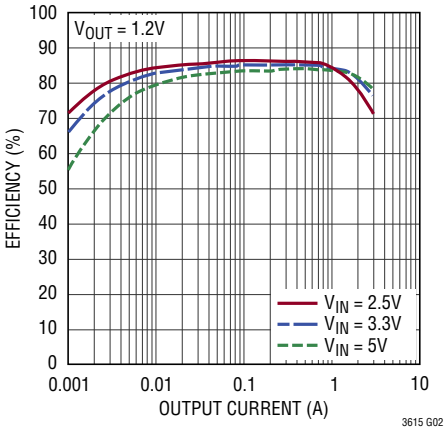
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, R_T/SYNC = SV_{IN}, unless otherwise noted.

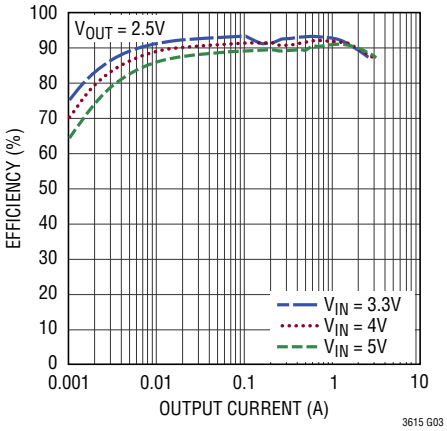
Efficiency vs Load Current (V_{MODE} = 0V)



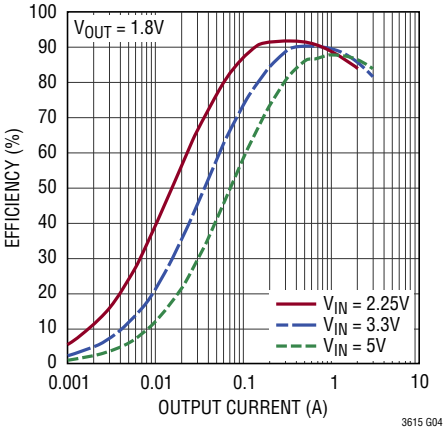
Efficiency vs Load Current (V_{MODE} = 0V)



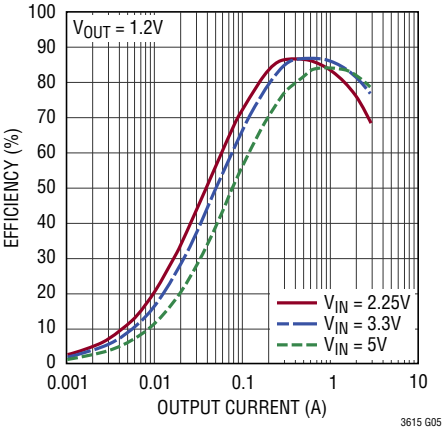
Efficiency vs Load Current (V_{MODE} = 0V)



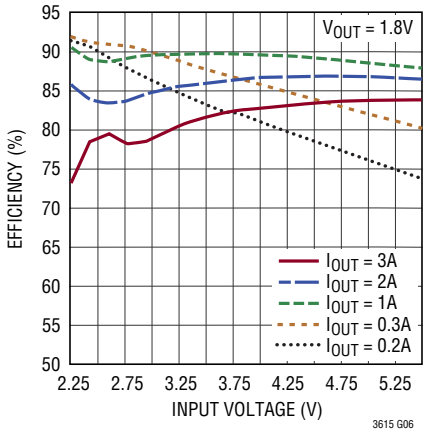
Efficiency vs Load Current (V_{MODE} = 0.55 • SV_{IN})



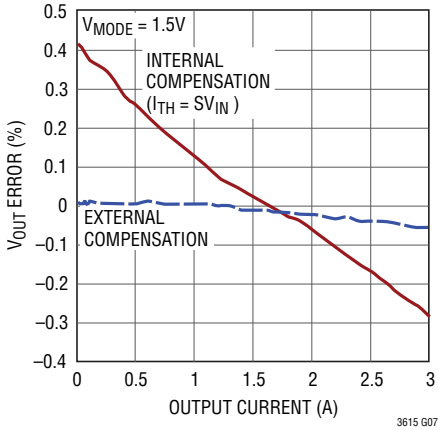
Efficiency vs Load Current (V_{MODE} = 0.55 • SV_{IN})



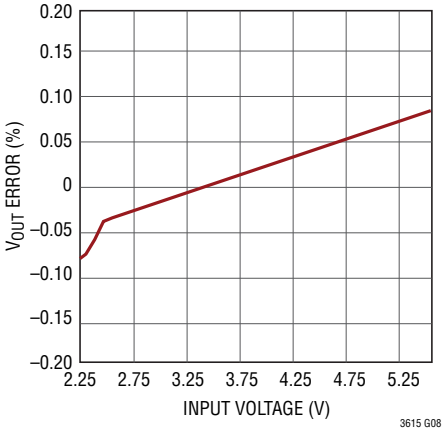
Efficiency vs Input Voltage (V_{MODE} = 0V)



Load Regulation

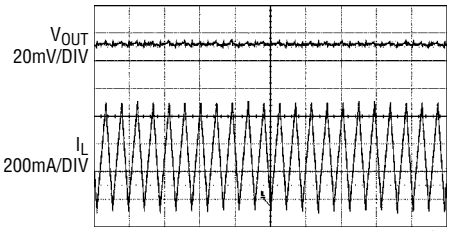


Line Regulation



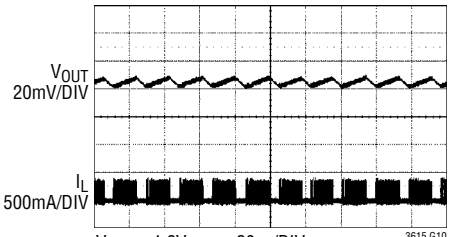
TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.3V, R_T/SYNC = SV_{IN}, unless otherwise noted.

Forced Continuous Mode Operation (FCM)



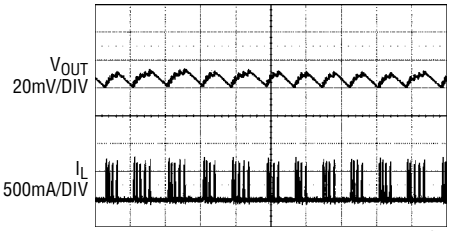
V_{OUT} = 1.8V 1µs/DIV
I_{OUT} = 100mA
V_{MODE} = 1.5V

Pulse-Skipping Mode Operation



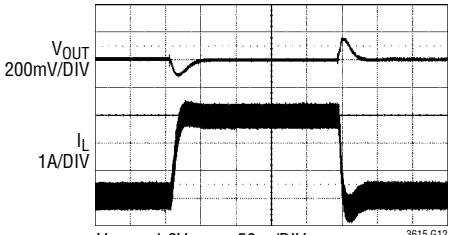
V_{OUT} = 1.8V 20µs/DIV
I_{OUT} = 75mA
V_{MODE} = 3.3V

Burst Mode Operation



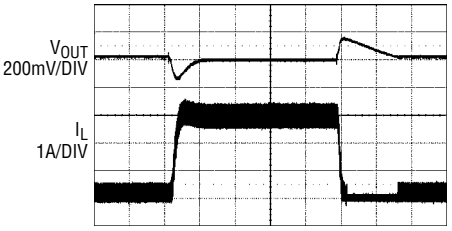
V_{OUT} = 1.8V 20µs/DIV
I_{OUT} = 75mA
V_{MODE} = 0V

Load Step Transient in FCM External Compensation



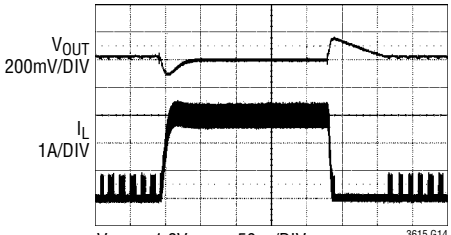
V_{OUT} = 1.8V 50µs/DIV
I_{LOAD} = 100mA TO 3A
V_{MODE} = 1.5V
COMPENSATION FIGURE 1

Load Step Transient in Pulse-Skipping Mode



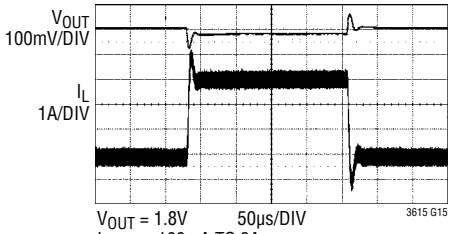
V_{OUT} = 1.8V 50µs/DIV
I_{LOAD} = 100mA TO 3A
V_{MODE} = 3.3V
COMPENSATION FIGURE 1

Load Step Transient in Burst Mode Operation



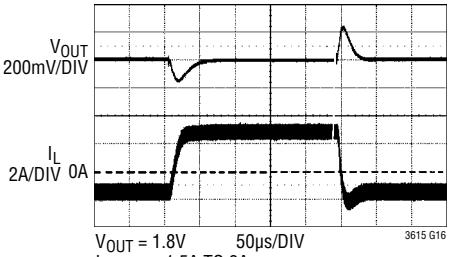
V_{OUT} = 1.8V 50µs/DIV
I_{LOAD} = 100mA TO 3A
V_{MODE} = 0V
COMPENSATION FIGURE 1

Load Step Transient in FCM with AVP Mode



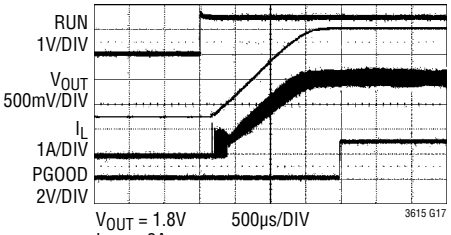
V_{OUT} = 1.8V 50µs/DIV
I_{LOAD} = 100mA TO 3A
V_{MODE} = 1.5V
V_{ITH} = 3.3V
OUTPUT CAPACITOR VALUE FIGURE 1

Load Step Transient in Forced Continuous Mode Sourcing and Sinking Current



V_{OUT} = 1.8V 50µs/DIV
I_{LOAD} = –1.5A TO 3A
V_{MODE} = 1.5V
COMPENSATION FIGURE 1

Internal Start-Up in Forced Continuous Mode

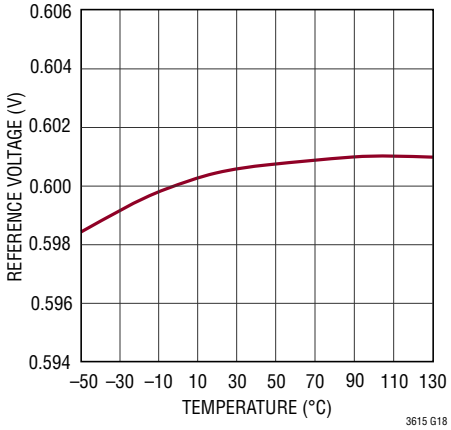


V_{OUT} = 1.8V 500µs/DIV
I_{OUT} = 3A
V_{MODE} = 1.5V

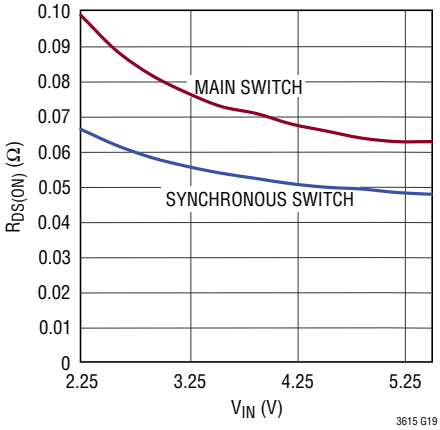
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, R_T/SYNC = SV_{IN}, unless otherwise noted.

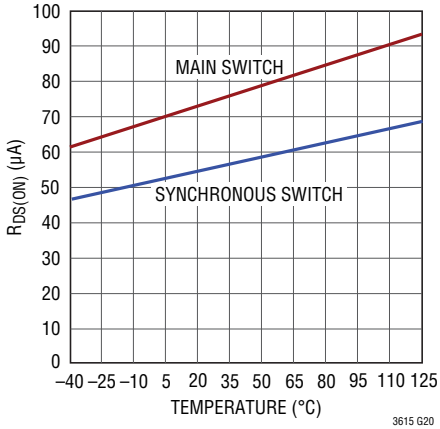
Reference Voltage vs Temperature



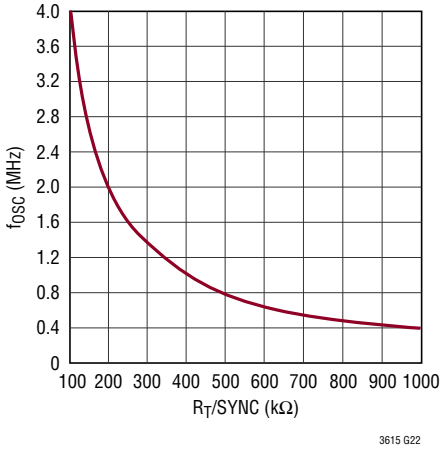
Switch On-Resistance vs Input Voltage



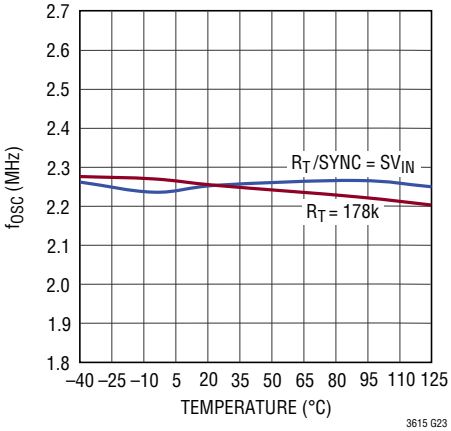
Switch On-Resistance vs Temperature



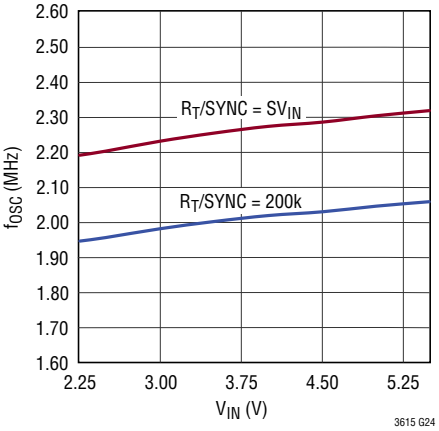
Frequency vs R_T/SYNC



Frequency vs Temperature

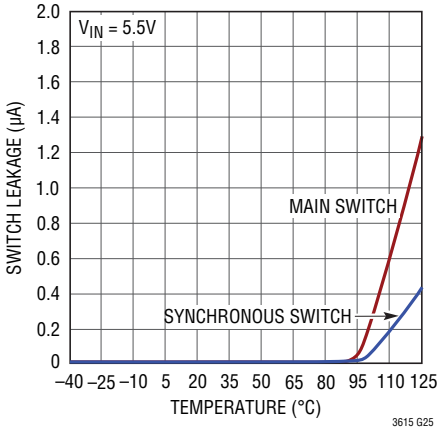


Frequency vs Input Voltage

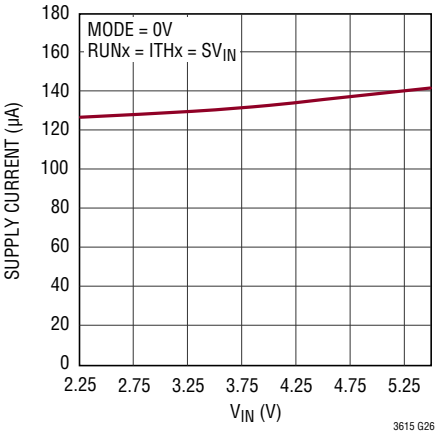


TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.3V, R_T/SYNC = SV_{IN}, unless otherwise noted.

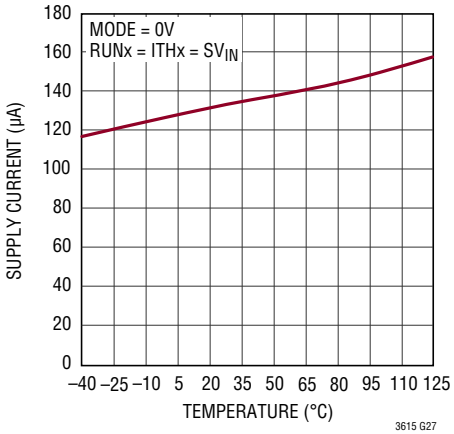
Switch Leakage vs Temperature



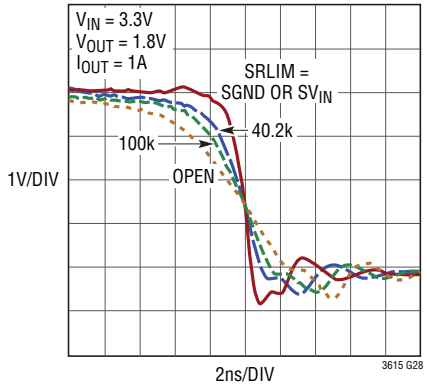
No Load Supply Current vs Input Voltage



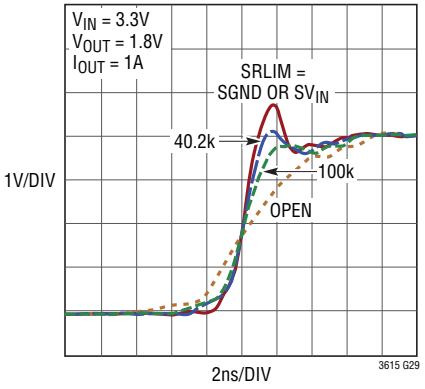
No Load Supply Current vs Temperature



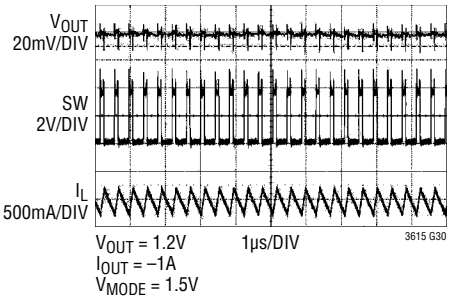
Slew Rate of Falling Edge at SW1/2 vs SRLIM Resistor



Slew Rate of Rising Edge at SW1/2 vs SRLIM Resistor

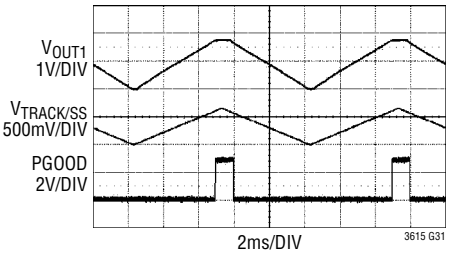


Sinking Current



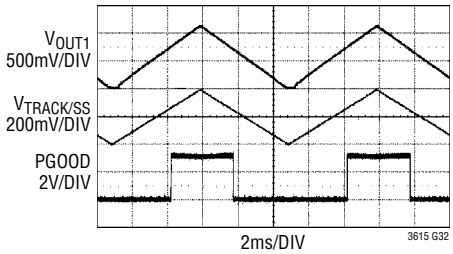
V_{OUT} = 1.2V
I_{OUT} = –1A
V_{MODE} = 1.5V

Tracking Up/Down in Forced Continuous Mode, SRLIM Pin Tied to 0V



V_{OUT} = 0V TO 1.8V
I_{OUT} = 3A
$V_{TRACK/SS}$ = 0V TO 0.7V
V_{MODE} = 1.5V
V_{SRLIM} = 0V

Tracking Up/Down in Forced Continuous Mode, SRLIM Pin Tied to SV_{IN}



V_{OUT} = 0V TO 1.2V
I_{OUT} = 3A
$V_{TRACK/SS}$ = 0V TO 0.4V
V_{MODE} = 1.5V
V_{SRLIM} = 3.3V

PIN FUNCTIONS (FE/UF)

PHASE (Pin 1/Pin 4): Phase Shift Selection. If pin is tied to SGND, the phase between SW1 and SW2 will be 0°. Tying PHASE to SV_{IN} will select 180° of phase shift. With the PHASE pin tied to half of the SV_{IN} voltage, 90° of phase shift will be selected.

V_{FB2} (Pin 2/Pin 5): Voltage Feedback Input Pin for Channel 2. See V_{FB1}.

ITH2 (Pin 3/Pin 6): Error Amplifier Compensation of Channel 2. See ITH1.

TRACK/SS2 (Pin 4 /Pin 7): Internal, External Soft-Start, External Reference Input for Channel 2. See TRACK/SS1.

SGND (Pin 5/Pin 8): Signal Ground. All small-signal and compensation components should connect to this ground pin which, in turn, should be connected to PGND at one point.

PV_{IN2} (Pins 6, 7/Pins 9, 10) Channel 2 Power Supply Input. See PV_{IN1}.

SW2 (Pins 8, 9/Pins 11, 12): Channel 2 Switching Node. See SW1.

RUN2 (Pin 10/Pin 13): Enable Pin for Channel 2. See RUN1.

RUN1 (Pin 11/Pin 14): Enable Pin for Channel 1. Forcing RUN1 above the input threshold enables the output SW1 of channel 1. Forcing both RUNx pins to ground shuts down the LTC3615. In shutdown, all functions are disabled and the LTC3615 draws <1µA of supply current.

R_T/SYNC (Pin 12/Pin 15): Oscillator Frequency. This pin provides three modes of setting the switching frequency.

1. Connecting a resistor from R_T/SYNC to ground will set the switching frequency based on the resistor value.
2. Driving R_T/SYNC with an external clock signal will synchronize the switcher to the applied frequency. The slope compensation is automatically adapted to the external clock frequency.
3. Tying this pin to SV_{IN} enables the internal 2.25MHz oscillator frequency.

PGOOD2 (Pin 13/Pin 16): Power Good Output for Channel 2. See PGOOD1.

SRLIM (Pin 14 /Pin 17): Slew Rate Limit. Slew rate on the switch pins is programmed with the SRLIM pin:

1. Tying this pin to SGND selects maximum slew rate.
2. Minimum slew rate is selected when the pin is open.
3. Connecting a resistor from SRLIM to SGND allows the slew rate to be continuously adjusted.
4. If SRLIM is tied to SV_{IN} the slew rate is set to maximum and DDR mode is enabled (see the Applications Information section).

PGOOD1 (Pin 15/Pin 18): Power Good Output Pin for Channel 1. The open-drain output will be pulled down to ground when the FB1 voltage of the channel is not within the power good voltage window. The PGOOD1 will also be pulled down if the channel is not enabled with the RUN1 pin or an undervoltage at SV_{IN} is detected. In DDR mode (SRLIM = SV_{IN}), the power good window moves in relation to the actual TRACK/SS pin voltage.

SW1 (Pins 17, 16/Pins 19, 20): Channel 1 Switching Node. Connection to the external inductor. This pin connects to the drains of the internal synchronous power MOSFET switches.

PV_{IN1} (Pins 18, 19/Pins 21, 22): Channel 1 Power Supply Inputs. These pins connect to the source of the internal power P-channel MOSFET of channel 1. P_{VIN1} and P_{VIN2} are independent of each other. They may connect to equal or lower supplies than S_{VIN}.

SV_{IN} (Pin 20/Pin 23) Signal Input Supply. This pin powers the internal control circuitry and is monitored by the undervoltage lockout comparator.

PIN FUNCTIONS (FE/UF)

TRACK/SS1 (Pin 21/Pin 24): Internal, External Soft-Start, External Reference Input for Channel 1. The type of start-up behavior for channel 1 is programmable with the TRACK/SS1 pin:

1. Internal soft-start with a fixed timing can be programmed by tying TRACK/SS1 to SV_{IN}.
2. External soft-start can be programmed with the timing set by a capacitor to ground and a resistor to SV_{IN}.
3. Tracking the start-up behavior of another supply is programmable (see the Applications Information section).
4. The pin can be used as external reference input.

ITH1 (Pin 22/Pin 1): Error Amplifier Compensation. Connection for external compensation from ITH to SGND. The current comparator's threshold increases with this control voltage. Tying this pin to SV_{IN} enables AVP mode with internal compensation.

V_{FB1} (Pin 23/Pin 2): Voltage Feedback Input Pin for Channel 1. Receives the feedback voltage for channel 1 from the external resistive divider across the output.

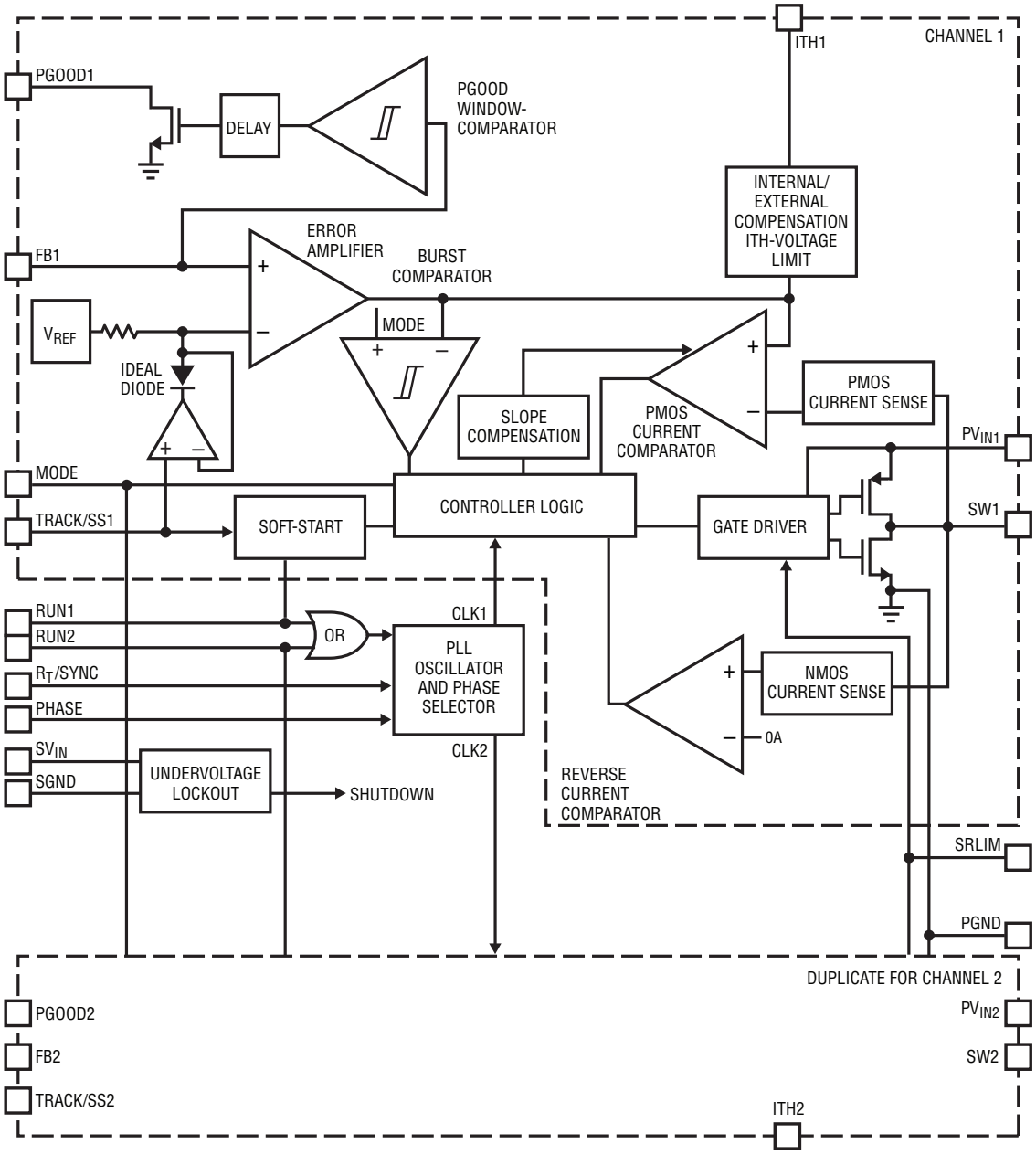
MODE (Pin 24/Pin 3): Mode Selection.

1. Tying the MODE pin to SV_{IN} or SGND enables pulse-skipping mode or Burst Mode operation (with an internal Burst Mode clamp), respectively.
2. If this pin is held at slightly higher than half of SV_{IN}, forced continuous mode will be selected.
3. Connecting this pin to an external voltage will select Burst Mode operation with the burst clamp set to the pin voltage.

PGND (Exposed Pad Pin 25/ Exposed Pad Pin 25): Power Ground. The exposed pad connects to the sources of the power N-channel MOSFETs. The PGND pin is common for both channels. The exposed pad must be soldered to the PCB.

For electrical connection and rated thermal performance, refer to the Operation and Applications Information sections for more information.

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3615 is a dual monolithic step-down DC/DC converter featuring current-mode, constant-frequency operation. Both channels are identical and share common clock and reference circuits to improve channel-to-channel matching.

During normal operation, the internal top power switch (P-channel MOSFET) of each channel is turned on at the beginning of its clock cycle. Current in the inductor increases until the current comparator trips and turns off the top power MOSFET. The peak inductor current at which the current comparator shuts off is controlled by the voltage on the ITH pin. The error amplifier adjusts the voltage on the ITH pin by comparing the feedback signals derived from an external resistor divider on the V_{FBx} pin with an internal 0.6V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier raises the ITH voltage until the average inductor current matches the new load current. Typical voltage range for the ITH pin is from 0.45V to 1.05V with 0.45V corresponding to zero current.

When the top power MOSFET shuts off, the synchronous power switch (N-channel MOSFET) turns on until either the current limit is reached or the next clock cycle begins. The bottom current limit is typically set at –4A for forced continuous mode and 0A for Burst Mode operation and pulse-skipping mode.

The operating frequency defaults to 2.25MHz when R_T/SYNC is connected to SV_{IN}, or can be set by an external resistor connected between the R_T/SYNC pin and ground, or by a clock signal applied to the R_T/SYNC pin. The switching frequency can be set from 400kHz to 4MHz (see the Applications Information section).

Overvoltage and undervoltage comparators pull the PGOOD output low if the output voltage varies more than ±7.5% from the set point.

MODE SELECTION

The MODE pin is used to select one of four different operating modes for both channels together (see Figures 1 and 3):

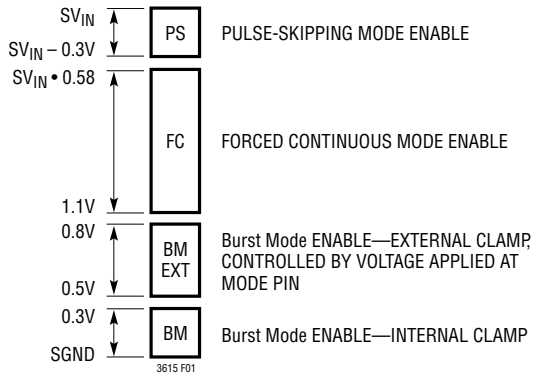


Figure 1. Mode Selection Voltage

Burst Mode Operation—Internal Clamp

Connecting the MODE pin to the SGND pin enables Burst Mode operation with its peak current set internally. In Burst Mode operation the internal power MOSFETs operate intermittently at light loads. This increases efficiency by minimizing switching losses. During the intervals when the MOSFETs are not switching, the LTC3615 enters a sleep state where many of the internal circuits are disabled to save power. During Burst Mode operation, the ITH voltage is monitored by the burst comparator to determine when the sleep state is entered or exited again. When the average inductor current is greater than the load current, the voltage on the ITH pin drops. As the ITH voltage falls below the internal threshold, the LTC3615 enters the sleep state. In the sleep state, the power MOSFETs are held off and the load current is solely supplied by the output capacitor. When the output voltage drops, the top power MOSFET is switched back on and the internal circuits are reenabled. This process repeats at a rate that is dependent on the load current.

OPERATION

Burst Mode Operation—External Clamp

Connecting the MODE pin to a voltage in the range of 0.5V to 0.8V enables Burst Mode operation with external clamp. During this mode of operation, the minimum voltage on the ITH pin is externally set by the voltage on the MODE pin. It is recommended to use Burst Mode operation with the internal clamp for ambient temperatures above 85°C.

Pulse-Skipping Mode Operation

Pulse-skipping mode is similar to Burst Mode operation, but the LTC3615 does not disable power to the internal circuitry during sleep mode. This improves output voltage ripple but uses more quiescent current compromising light load efficiency.

Connecting the MODE pin to SV_{IN} enables pulse-skipping mode. As the load current decreases, the peak inductor current will be determined by the voltage on the ITH pin until the ITH voltage drops below 450mV, corresponding to 0A. At this point switching cycles will be skipped to keep the output voltage in regulation.

Forced Continuous Mode Operation

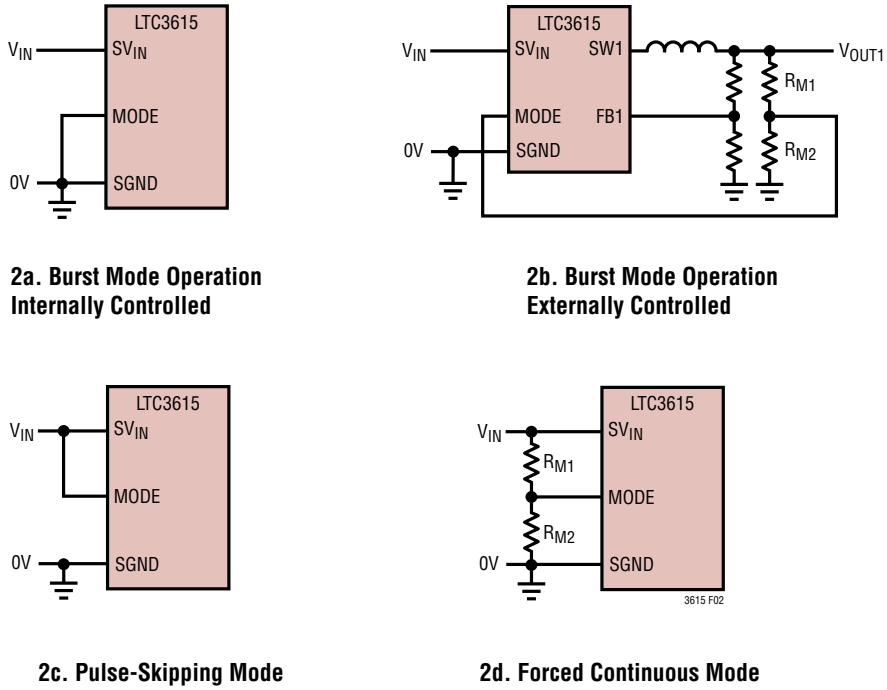
In forced continuous mode the inductor current is constantly cycled which creates a minimum output voltage ripple at all output current levels.

Connecting the MODE pin, to a voltage in the range of 1.1V to SV_{IN} • 0.58 will select the forced continuous mode operation.

The forced continuous mode must be used if the output is required to sink current.

Dropout Operation

As the input supply voltage approaches the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle, eventually reaching 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-channel MOSFET and the inductor.



2a. Burst Mode Operation Internally Controlled

2b. Burst Mode Operation Externally Controlled

2c. Pulse-Skipping Mode

2d. Forced Continuous Mode

Figure 2. Modes of Operation

OPERATION

Low Supply Operation

The LTC3615 is designed to operate down to an input supply voltage of 2.25V. An important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-channel and N-channel power switches increases by 50% compared to 5V. The user should calculate the power dissipation when the LTC3615 is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in current mode constant-frequency architectures by preventing subharmonic oscillations at duty cycles greater than 50%. The LTC3615 implements slope compensation by adding a compensation ramp to the inductor current signal.

Short-Circuit Protection

The peak inductor current at which the current comparator shuts off the top power switch is controlled by the voltage on the ITH pin.

If the output current increases, the error amplifier raises the ITH pin voltage until the average inductor current matches the new load current. In normal operation, the LTC3615 clamps the maximum ITH pin voltage at approximately 1.05V which corresponds to about 5A peak inductor current.

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. The LTC3615 uses two techniques to prevent current runaway from occurring:

1. If the output voltage drops below 50% of its nominal value, the clamp voltage at pin ITH is lowered, causing the maximum peak inductor current to lower gradually with the output voltage. When the output voltage reaches 0V, the clamp voltage at the ITH pin drops to 40% of the clamp voltage during normal operation. The short-circuit peak inductor current is determined by the minimum on-time of the LTC3615, the input voltage and the inductor value. This foldback behavior helps in limiting the peak inductor current when the output is shorted to ground. It is disabled during internal or external soft-start and tracking up/down operation (see the Applications Information section).
2. If the inductor current of the bottom MOSFET increases beyond 6A typical, the top power MOSFET will be held off and switching cycles will be skipped until the inductor current reduces.

APPLICATIONS INFORMATION

Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values.

Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency of the LTC3615 is determined by an external resistor that is connected between pin R_T/SYNC and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_T = \frac{4 \bullet 10^{11} \Omega Hz}{f_{OSC}}$$

Although frequencies as high as 4MHz are possible, the minimum on-time of the LTC3615 imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 60ns, therefore, the minimum duty cycle is equal to 60ns • 100% • f_{OSC}(Hz)

Tying the R_T/SYNC pin to SV_{IN} sets the default internal operating frequency to 2.25MHz ±20%.

Frequency Synchronization

The LTC3615's internal oscillator can be synchronized to an external frequency by applying a square wave clock signal to the R_T/SYNC pin. During synchronization, the top MOSFET turn-on of channel 1 is locked to the rising edge of the external frequency source. The synchronization frequency range is 400kHz to 4MHz. The internal slope compensation is automatically adapted to the external clock frequency.

In the signal path from the R_T/SYNC clock input to the SW output, the LTC3615 is processing the external clock frequency through an internal PLL.

After detecting an external clock on the first rising edge of R_T/SYNC the PLL starts up with the internal default of 2.25MHz. The internal PLL then requires a certain number

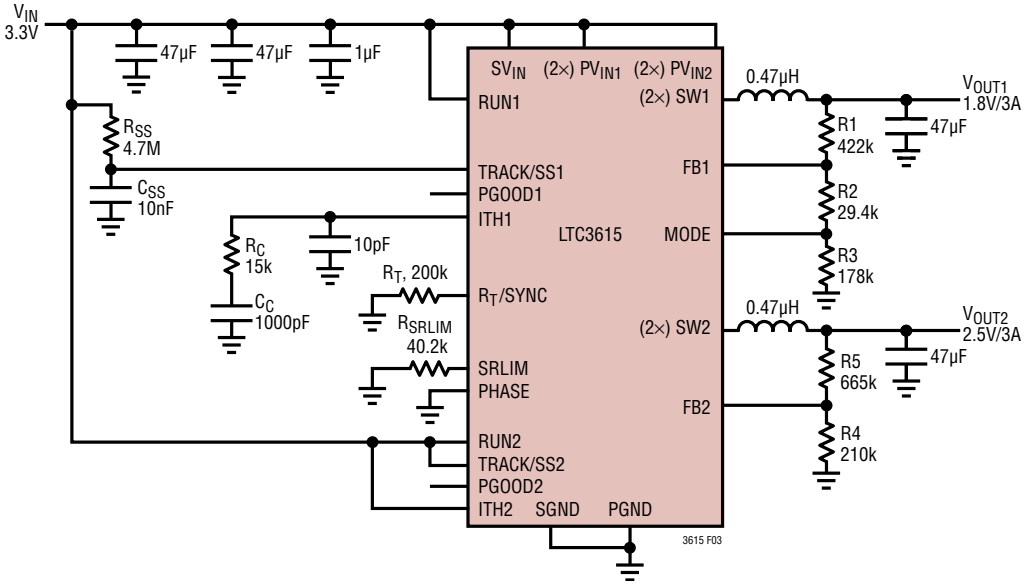


Figure 3. Soft-Start and Compensation for Channel 1 Externally Programmed, Soft-Start and Compensation for Channel 2 Internally Programmed

APPLICATIONS INFORMATION

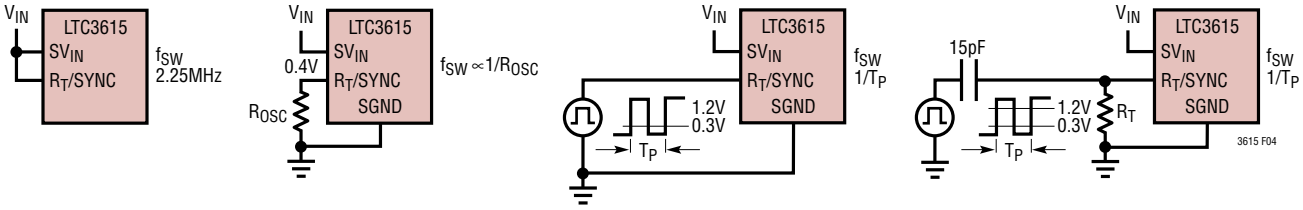


Figure 4. Setting the Switching Frequency

of periods to settle until the frequency at SW matches the frequency and phase of R_T/SYNC.

When the external clock signal is removed, the LTC3615 needs approximately 5µs to detect the absence of the external clock. During this time, the PLL will continue to provide clock cycles before it is switched back to the default frequency or selected frequency (set via the external R_T resistor).

A safe way of driving the R_T/SYNC input is with an AC coupling to the clock generator via a 15pF capacitor. The AC coupling avoids complications if the external clock generator cannot provide a continuous clock signal at the time of start-up, operation and shut down of the LTC3615.

In general, any abrupt clock frequency change of the regulator will have an effect on the SW pin timing and may cause equally sudden output voltage changes. This must be taken into account in particular if the external clock frequency is significantly different from the internal default of 2.25MHz.

Phase Selection

Channel 2 will operate in-phase, 180° out-of-phase (anti-phase) or shifted by 90° from channel 1 depending on the state of the PHASE pin—low, midrail and high, respectively. Antiphase generally reduces input voltage and current ripple. Crosstalk between switch nodes SW1, SW2 and components or sensitive lines connected to FBx, ITHx, R_T/SYNC or SRLIM can cause unstable switching waveforms and unexpectedly large input and output voltage ripple.

The situation improves if rising and falling edges of the switch nodes are timed carefully not to coincide. Depending on the duty cycle of the two channels, choose the phase difference between the channels to keep edges as far away from each other as possible.

For a duty cycle of less than 40% for one channel and more than 60% for the other channel, choose a phase shift of 0 or 180° (PHASE = SGND or SV_{IN}). If both channels have a duty cycle of around 50%, select a phase difference of 90° (PHASE = one-half SV_{IN}).

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{SW} \bullet L}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Having a lower ripple current reduces the core losses in the inductor, the ESR losses in the output capacitors and the output voltage ripple. A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.3(I_{OUT(MAX)})$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f_{SW} \bullet \Delta I_{L(MAX)}}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor value will also have an effect on Burst Mode operation. The transition to low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this to occur at lower DC load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

APPLICATIONS INFORMATION

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for fixed inductor value, but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire, and therefore, copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow a ferrite core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. Table 1 shows some typical surface mount inductors that work well in LTC3615 applications.

Input Capacitor C_{IN} Selection

In continuous mode, the source current of the top P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used for C_{IN}.

The maximum RMS capacitor current is given by:

$$I_{RMS} = I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\left(\frac{V_{IN}}{V_{OUT}} - 1\right)}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

Table 1. Representative Surface Mount Inductors

INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)
Vishay IHLP-2020BZ-01				
0.33	7.6	25	5.18 × 5.49	2
0.47	8.9	21	5.18 × 5.49	2
0.68	11.2	15	5.18 × 5.49	2
1	18.9	16	5.18 × 5.49	2
Toko DE3518C Series				
0.22	8	24	4.3 × 4.7	2
Sumida CDMC6D28 Series				
0.3	3.2	15.4	6.7 × 7.25	3
0.47	4.2	13.6	6.7 × 7.25	3
0.68	5.4	11.3	6.7 × 7.25	3
1	8.8	8.8	6.7 × 7.25	3
NEC/Tokin MPLC0730L Series				
0.47	4.5	16.6	6.9 × 7.7	3.0
0.75	7.5	12.2	6.9 × 7.7	3.0
1.0	9.0	10.6	6.9 × 7.7	3.0
Coilcraft DO1813H Series				
0.33	4	10	8.9 × 6.1	5
0.56	10	7.7	8.9 × 6.1	5
Coilcraft SLC7530 Series				
0.27	0.1	14	7.5 × 6.7	3
0.35	0.1	11	7.5 × 6.7	3
0.4	0.1	8	7.5 × 6.7	3

APPLICATIONS INFORMATION

Output Capacitor C_{OUT} Selection

The selection of C_{OUT} is typically driven by the required ESR to minimize voltage ripple and load step transients (low-ESR ceramic capacitors are discussed in the next section). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \bullet \left(ESR + \frac{1}{8 \bullet f_{SW} \bullet C_{OUT}} \right)$$

where f_{SW} = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolytic, special polymer, ceramic and dry tantalum capacitors are all available in surface mount packages.

Tantalum capacitors have the highest capacitance density, but can have higher ESR and must be surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can often be used in extremely cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability.

Ceramic Input and Output Capacitors

Ceramic capacitors have the lowest ESR and can be cost effective, but also have the lowest capacitance density, high voltage and temperature coefficients, and exhibit audible piezoelectric effects. In addition, the high-Q of ceramic capacitors along with trace inductance can lead to significant ringing.

Capacitors are tempting for switching regulator use because of their very low ESR. Great care must be taken when using only ceramic input and output capacitors.

Ceramic caps are prone to temperature effects which require the designer to check loop stability over the operating temperature range. To minimize their large temperature and voltage coefficients, only X5R or X7R ceramic capacitors should be used.

When a ceramic capacitor is used at the input, and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to damage the part.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor size. Typically, three to four cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about two to three times the linear drop of the first cycle. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx \frac{2.5 \bullet \Delta I_{OUT}}{f_{SW} \bullet V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements. In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low.

APPLICATIONS INFORMATION

Output Voltage Programming

The output voltages are set by external resistive dividers. For example, V_{OUT2} can be set according to the following equation:

$$V_{OUT2} = 0.6V \bullet \left(1 + \frac{R5}{R4}\right)$$

The resistive divider allows pin V_{FB} to sense a fraction of the output voltage as shown in Figure 3.

Burst Clamp Programming

If the voltage on the MODE pin is less than 0.8V, Burst Mode operation is enabled. If the voltage on the MODE pin is less than 0.3V, the internal default burst clamp level is selected. The minimum voltage on the ITH pin is typically 525mV (internal clamp).

If the voltage is between 0.45V and 0.8V, the voltage on the MODE pin (V_{BURST}) is equal to the minimum voltage on the ITH pin (external clamp) and determines the burst clamp level I_{BURST} (typically from 1A to 3.5A).

When the ITH voltage falls below the internal (or external) clamp voltage, the sleep state is entered. As the output load current drops, the peak inductor current decreases to keep the output voltage in regulation. When the output load current demands a peak inductor current that is less than I_{BURST}, the burst clamp will force the peak inductor current to remain equal to I_{BURST} regardless of further reductions in the load current.

Since the average inductor current is greater than the output load current, the voltage on the ITH pin will decrease. When the ITH voltage drops, sleep mode is enabled in which both power switches are shut off along with most of the circuitry to minimize power consumption. All circuitry is turned back on and the power switches resume operation when the output voltage drops out of regulation. The value for I_{BURST} is determined by the desired amount of output voltage ripple. As the value of I_{BURST} increases, the sleep period between pulses and the output voltage ripple increase. It is recommend to use Burst Mode operation with internal clamp for temperatures above 85°C ambient.

Pulse-Skipping Mode

Pulse-skipping mode, which is a compromise between low output voltage ripple and efficiency, can be implemented by connecting the MODE pin to SV_{IN}. This sets I_{BURST} to 0A. In this condition, the peak inductor current is limited by the minimum on-time of the current comparator. The lowest output voltage ripple is achieved while still operating discontinuously. During very light output loads, pulse-skipping allows only a few switching cycles to skip while maintaining the output voltage in regulation.

Internal and External Compensation

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC load current. When a load step occurs, like the one shown in Figure 5, V_{OUT} shifts by an amount equal to ΔI_{LOAD} • ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the ITH pin allows the transient response to be optimized over a wide range of output capacitance.

The ITH1 external components (15k and 100pF) shown in Figure 3 will provide an adequate compensation as well as a starting point for most applications. The values can be modified slightly to optimize transient response once the final PCB layout is complete and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system. The external compensation, forced continuous operation circuit in the Typical

APPLICATIONS INFORMATION

Applications section uses faster compensation to improve load step response.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. More output capacitance may be required depending on the duty cycle and load step requirements.

If the ITH pin is tied to SV_{IN}, the active voltage positioning (AVP) mode and the internal compensation is selected.

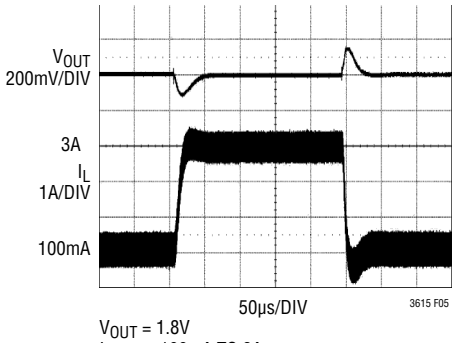
In AVP mode, the load regulation performance is intentionally reduced, setting the output voltage at a point that is dependent on the load current. When the load current suddenly increases, the output voltage starts from a level slightly higher than nominal so the output voltage can droop more and stay within the specified voltage range.

When the load current suddenly decreases, the output voltage starts at a level lower than nominal so the output voltage can have more overshoot and stay within the specified voltage range. This behavior is demonstrated in Figure 6.

The benefit is a lower peak-to-peak output voltage deviation for a given load step without having to increase the output filter capacitance. Alternatively, the output voltage filter capacitance can be reduced while maintaining the same peak-to-peak transient response. For this operation mode, the loop gain is reduced and no external compensation is required.

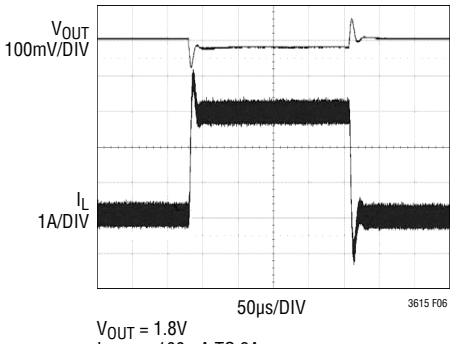
Programmable Switch Pin Slew Rate

As switching frequencies rise, it is desirable to minimize the transition time required when switching to minimize power losses and blanking time for the switch to settle. However, fast slewing of the switch node results in relatively high external radiated EMI and high on-chip supply transients, which can cause problems for some applications.



V_{OUT} = 1.8V
I_{LOAD} = 100mA TO 3A
V_{MODE} = 1.5V
COMPENSATION AND OUTPUT CAPACITOR VALUES OF FIGURE 3

Figure 5. Load Step Transient in FCM with External Compensation



V_{OUT} = 1.8V
I_{LOAD} = 100mA TO 3A
V_{MODE} = 1.5V
V_{IN} = V_{ITH} = 3.3V
OUTPUT CAPACITOR VALUE FIGURE 3

Figure 6. Load Step Transient in FCM in AVP Mode

APPLICATIONS INFORMATION

The LTC3615 allows the user to control the slew rate of the switching node SW by using the SRLIM pin. Tying this pin to ground selects the fastest slew rate. The slowest slew rate is selected when the pin is open. Connecting a resistor (between 10k to 100k) from SRLIM pin to ground adjusts the slew rate between the maximum and minimum values. The reduced dV/dt of the switch node results in a significant reduction of the supply and ground ringing, as well as lower radiated EMI. See Figure 7a and the Typical Performance Characteristics section for examples.

Reducing the slew rate causes a trade-off between efficiency and low EMI (see Figure 7b).

Particular attention should be used with very high switching frequencies. Using the slowest slew rate (SRLIM open) can reduce the minimum duty cycle capability.

Soft-Start

The RUNx pins provide a means to shut down each channel of the LTC3615. Pulling both pins below 0.3V places the LTC3615 in a low quiescent current shutdown state (I_Q < 1µA).

After enabling the LTC3615 by bringing either one or both RUNx pins above the threshold, the enabled channels enter a soft-start-up state. The type of soft-start behavior is set by the TRACK/SSx pins. The soft-start cycle begins with an initial discharge pulse pulling down the TRACK/SSx pin to SGND and discharging the external capacitor C_{SS} (see Figure 3).

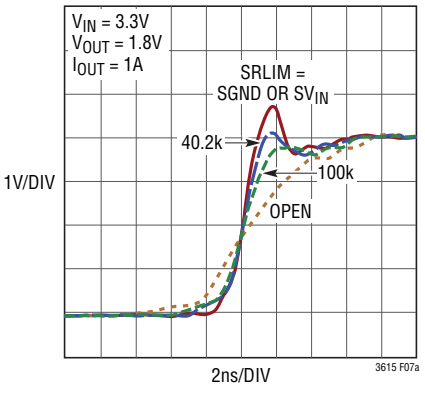
The initial discharge is adequate to discharge capacitors up to 33nF. If a larger capacitor is required, connect the external soft-start resistor R_{SS} to the RUN pin to fully discharge the capacitor.

1. Tying this pin to SV_{IN} selects the internal soft-start circuit. This circuit ramps the output voltage to the final value within 1ms.
2. If a longer soft-start period is desired, it can be set externally with a resistor and capacitor on the TRACK/SSx pins as shown in Figure 3. The voltage applied at the TRACK/SSx pins sets the value of the internal reference at V_{FB} until TRACK/SSx is pulled above 0.6V. The external soft-start duration can be calculated by using the following equation:

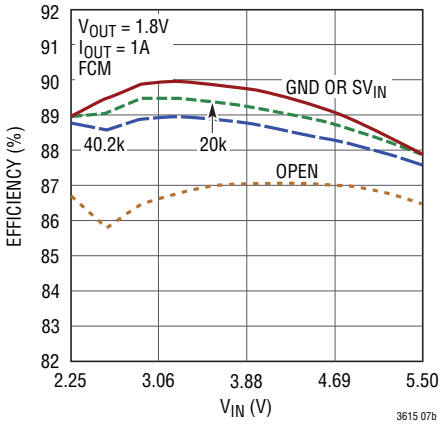
$$t_{SS} = R_{SS} \bullet C_{SS} \bullet \ln\left(\frac{SV_{IN}}{SV_{IN} - 0.6V}\right)$$

3. The TRACK/SSx pin can be used to track the output voltage of another supply.

   Regardless of either the internal or external soft-start state, the MODE pin is ignored during start-up and the regulator defaults to pulse-skipping mode. In addition, the PGOODx pin is kept low, and the frequency foldback function is disabled.



(7a) Slew Rate of Rising Edge at SW1/2 vs SRLIM Resistor



(7b) Efficiency vs SRLIM Resistor Programming

Figure 7. Slew Rate and the SRLIM Resistor

APPLICATIONS INFORMATION

Output Voltage Tracking Input

If SRLIM is low, once $V_{TRACK/SS}$ reaches or exceeds 0.6V the run state is entered, and the MODE selection, power good and current foldback circuits are enabled.

In the run state, the TRACK/SS pin can be used to track down/up the output voltage of another supply. If the $V_{TRACK/SS}$ again drops below 0.6V, the LTC3615 enters the down-tracking state and the V_{OUT} is referenced to the TRACK/SS voltage. If $V_{TRACK/SS}$ reaches 0.1V value the switching frequency is reduced by 4x to ensure that the minimum duty cycle limit does not prevent the output from following the TRACK/SS pin. The run state will resume if the $V_{TRACK/SS}$ again exceeds 0.6V and the V_{OUT} is referenced to the internal reference.

Through the TRACK/SS pin, the output voltage can be set up to either coincidental or ratiometric tracking, as shown in Figures 8 and 9.

To implement the coincidental tracking waveform in Figure 8, connect an extra resistive divider to the output of the master channel and connect its midpoint to the TRACK/SS pin for the slave channel. The ratio of this divider should be selected the same as that of the slave channel's feedback divider (Figure 10).

In this tracking mode, the master channel's output must be set higher than slave channel's output. To implement the ratiometric start-up in Figure 9, no extra divider is needed; simply connect the TRACK/SS pin to the other channel's V_{FB} pin (Figure 12).

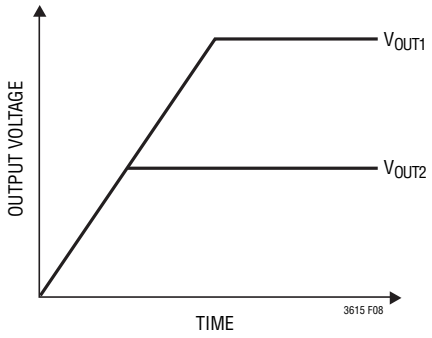


Figure 8. Coincident Start-Up Tracking

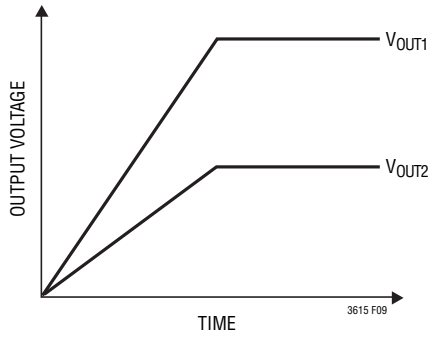


Figure 9. Ratiometric Start-Up Tracking

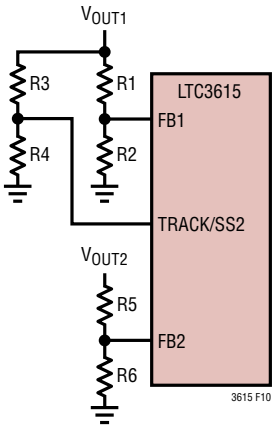


Figure 10. Set for Coincidentally Tracking (R3 = R5, R4 = R6)

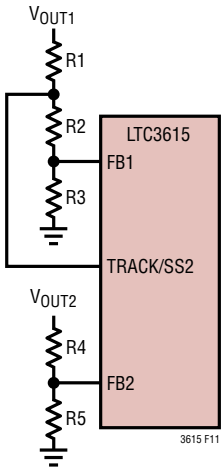


Figure 11. Alternative Set-Up for Coincident Start-Up Tracking (R1 = R3, R2 = R3 = R5)

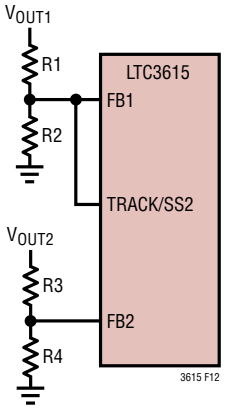


Figure 12. Set-Up for Ratiometric Tracking

APPLICATIONS INFORMATION

External Reference Input (DDR Mode)

If SRLIM is tied to SV_{IN}, the TRACK/SS pin can be used as an external reference input between 0.3V and 0.5V, if desired (see Figure 13).

In DDR mode, the maximum slew rate is selected. If $V_{TRACK/SS}$ is within 0.3V and 0.5V, the PGOOD function is enabled. If $V_{TRACK/SS}$ is less than 0.3V, the output current foldback is disabled and the PGOOD pin is always pulled down.

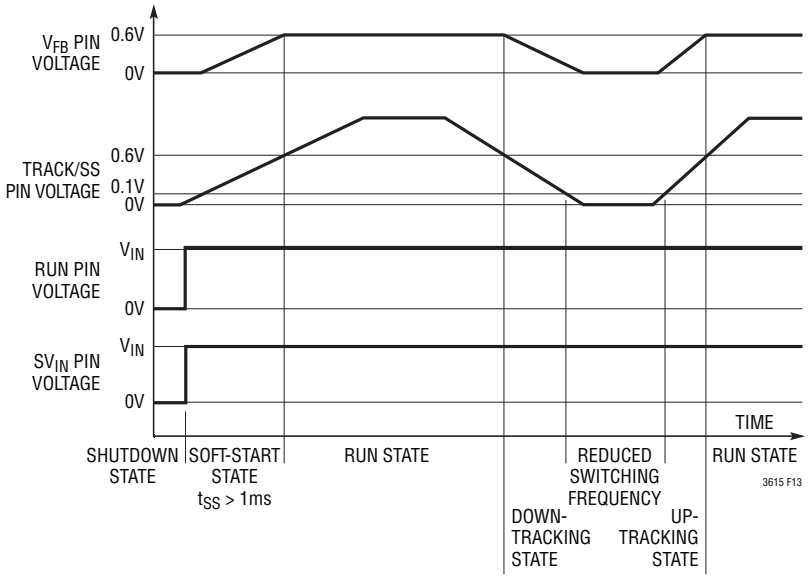


Figure 13. Tracking if V_{SRLIM} Is Low

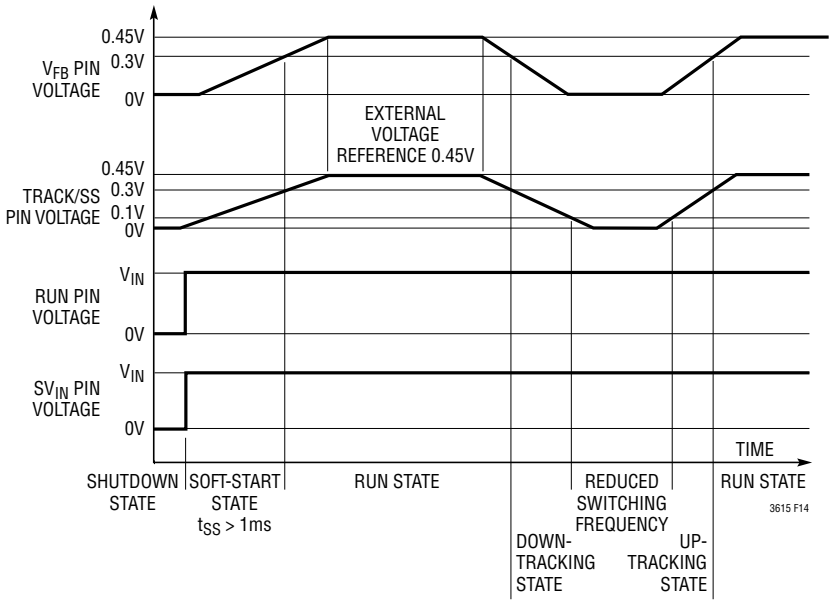


Figure 14. Tracking if V_{SRLIM} Is Tied to SV_{IN}

APPLICATIONS INFORMATION

DDR Application

The LTC3615 can be used in DDR memory power supply applications by tying the SRLIM pin to SV_{IN}. In DDR mode, the maximum slew rate is selected. The output can both source and sink current. Current sinking is typically limited to 1.5A, for 1MHz frequency and 1µH inductance, but can be lower at higher frequencies and low output voltages. If higher ripple current can be tolerated, smaller inductor values can increase the sink current limit. See the Typical Performance Characteristics curves for more information. In addition, in DDR mode, lower external reference voltages and tracking output voltages between channels are possible. See the Output Voltage Tracking Input section.

Single, Low Ripple 6A Output Application

The LT3615 can generate a single, low ripple 6A output if the outputs of the two switching regulators are tied together and share a single output capacitor (see Figure 15 on back of data sheet). In order to evenly share the current between the two regulators, it is needed to connect pins FB1 to FB2, ITH1 to ITH2 and to select forced continuous mode at the MODE pin. To achieve lowest ripple, 90°, or better, 180°, antiphase is selected by connecting the PHASE pin to midrail or SV_{IN}. There are several advantages to this 2-phase buck regulator. Ripple currents at the input and output are reduced, reducing voltage ripple and allowing the use of smaller, less expensive capacitors. Although two inductors are required, each will be smaller than the inductor required for a single-phase regulator. This may be important when there are tight height restrictions on the circuit.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: Efficiency = 100% – (L1 + L2 + L3 + ...) where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of little consequence.

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the Electrical Characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} due to gate charge, and it is typically larger than the DC bias current. Both the DC bias and gate charge losses are proportional to V_{IN}, thus, their effects will be more pronounced at higher supply voltages.
2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC), as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 – DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. To obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% of the total loss.

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Thermal Considerations

In most applications, the LTC3615 does not dissipate much heat due to its high efficiency. However, in applications where the LTC3615 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, all four power switches will be turned off and the SW node will become high impedance.

To prevent the LTC3615 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. To determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated by the regulator, and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by:

$$T_J = T_A + T_{RISE}$$

where T_A is the ambient temperature.

As an example, consider this case: the LTC3615 is in dropout at an input voltage of 3.3V with a load current for each channel of 2A at an ambient temperature of 70°C. Assuming a 20°C rise in junction temperature, to 90°C, results in an $R_{DS(ON)}$ of 0.086mΩ (see the graph in the Typical Performance Characteristics section). Therefore, the power dissipated by the part is:

$$P_D = (I_1^2 + I_2^2) \bullet R_{DS(ON)} = 0.69W$$

For the QFN package, the θ_{JA} is 37°C/W.

Therefore, the junction temperature of the regulator operating at 70°C ambient temperature is approximately:

$$T_J = 0.69W \bullet 37°C/W + 70°C = 95°C$$

Note that for very low input voltage, the junction temperature will be higher due to increased switch resistance $R_{DS(ON)}$. It is not recommended to use full load current at high ambient temperature and low input voltage.

To maximize the thermal performance of the LTC3615, the Exposed Pad should be soldered to a ground plane. See the PC Board Layout Checklist.

Design Example

As a design example, consider using the LTC3615 in an application with the following specifications:

V_{IN} = 3.3V to 5.5V
V_{OUT1} = 2.5V
V_{OUT2} = 1.2V
$I_{OUT1(MAX)}$ = 1A
$I_{OUT2(MAX)}$ = 3A
$I_{OUT(MIN)}$ = 100mA
f = 2.25MHz

Because efficiency is important at both high and low load current, Burst Mode operation will be selected by connecting the MODE pin to SGND.

First, calculate the timing resistor:

$$R_{RT/SYNC} = \frac{4E11\,\Omega \bullet Hz}{2.25MHz} = 178k$$

Next, calculate the inductor values for about 1A ripple current at maximum V_{IN}:

$$L1 = \left(\frac{2.5V}{2.25MHz \bullet 1A}\right) \bullet \left(1 - \frac{2.5V}{5.5V}\right) = 0.6\mu H$$

$$L2 = \left(\frac{1.2V}{2.25MHz \bullet 1A}\right) \bullet \left(1 - \frac{1.2V}{5.5V}\right) = 0.42\mu H$$

Using a standard value of 0.56µH and 0.47µH inductors results in maximum ripple currents of:

$$\Delta I_{L1} = \left(\frac{2.5V}{2.25MHz \bullet 0.56\mu H}\right) \bullet \left(1 - \frac{2.5V}{5.5V}\right) = 1.08A$$

$$\Delta I_{L2} = \left(\frac{1.2V}{2.25MHz \bullet 0.47\mu H}\right) \bullet \left(1 - \frac{1.2V}{5.5V}\right) = 0.89A$$

APPLICATIONS INFORMATION

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, 47µF ceramic capacitors will be used with X5R or X7R dielectric.

C_{IN} should be sized for a maximum current rating of:

$$I_{RMS(MAX)} = \frac{I_{OUT1}}{2} + \frac{I_{OUT2}}{2} = 2A_{RMS}$$

Decoupling the PV_{IN} with two 47µF capacitors is adequate for most applications.

Finally, it is possible to define the soft-start up time choosing the proper value for the capacitor and the resistor connected to TRACK/SS pin. If one sets minimum T_{SS} = 5ms and a resistor of 4.7M, the following equation can be solved with the maximum SV_{IN} = 5.5V:

$$C_{SS} = \frac{5ms}{4.7M \bullet \ln\left(\frac{5.5V}{5.5V - 0.6V}\right)} = 9.2nF$$

The standard value of 10nF and 4.7M guarantees the minimum soft-start time of 5ms. In Figure 3, channel 1 shows the schematic for this design example.

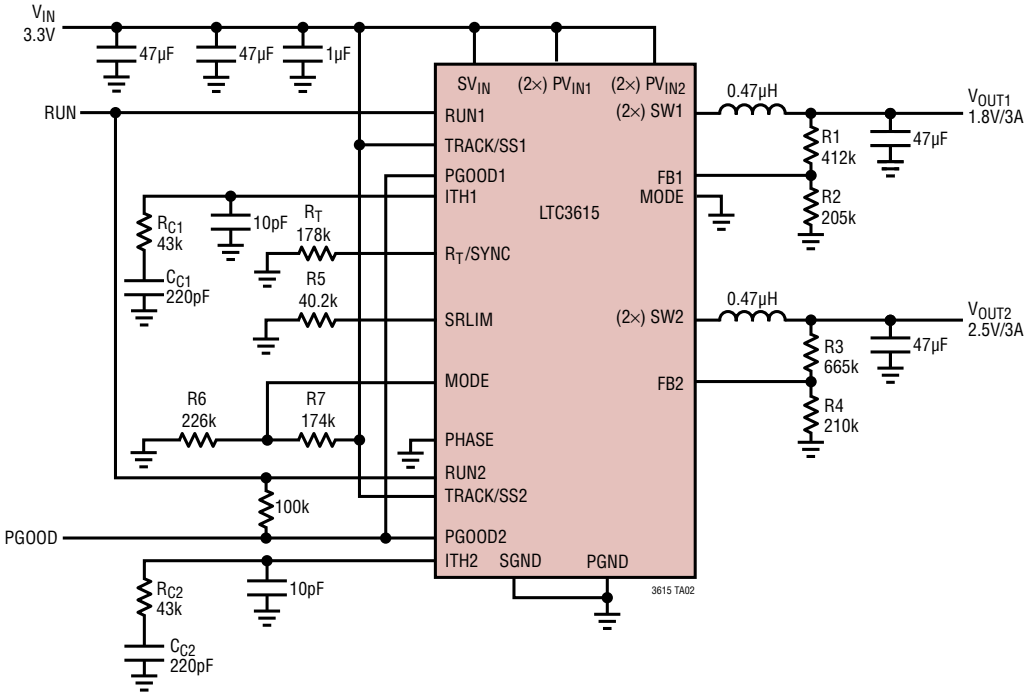
PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3615:

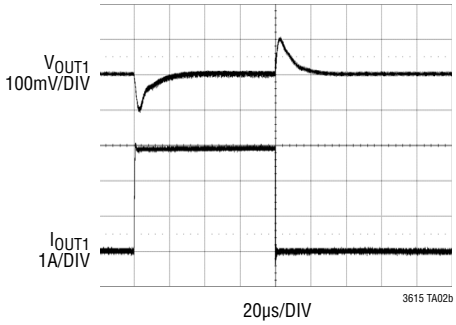
1. A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small signal components returning to the SGND pin at one point which is then connected to the PGND node at the exposed pad close to the LTC3615
2. Connect the (+) terminal of the input capacitors, C_{IN}, as close as possible to the PV_{INx} pins, and the (–) terminal as close as possible to the exposed pad PGND. This capacitor provides the AC current into the internal power MOSFETs.
3. Keep the switching nodes, SWx, away from all sensitive small signal nodes FBx, ITHx, RTSYNC, SRLIM.
4. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to PGND (exposed pad) for best performance.
5. Connect the V_{FBx} pins directly to the feedback resistors. The resistor divider must be connected between V_{OUTx} and SGND.

TYPICAL APPLICATIONS

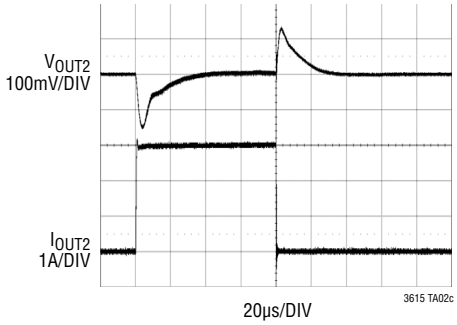
External Compensation, Forced Continuous Operation, In-Phase Switching, Slew Rate Limit, Common PGOOD Output



V_{OUT1} Waveform

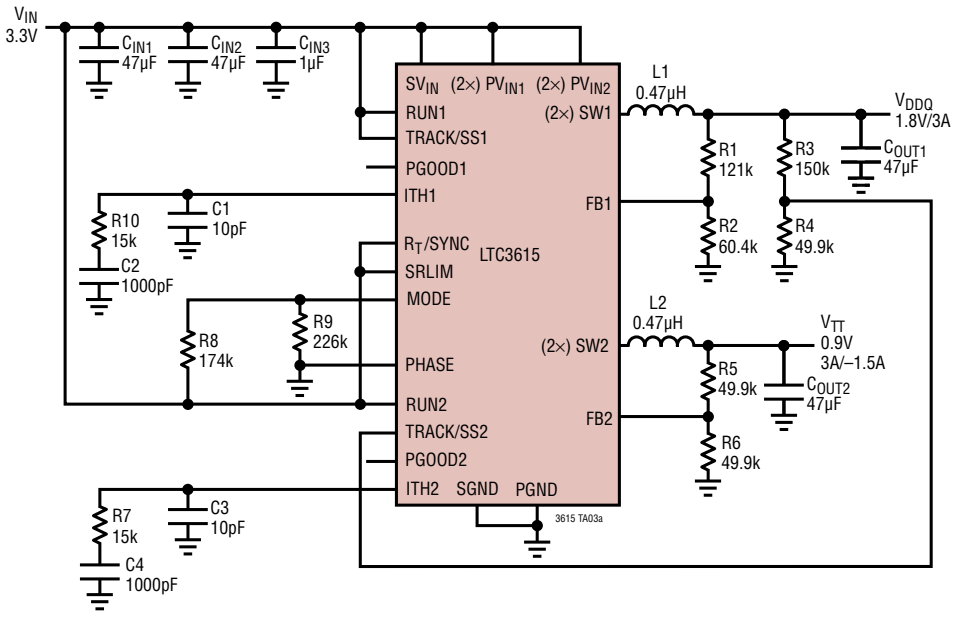


V_{OUT2} Waveform

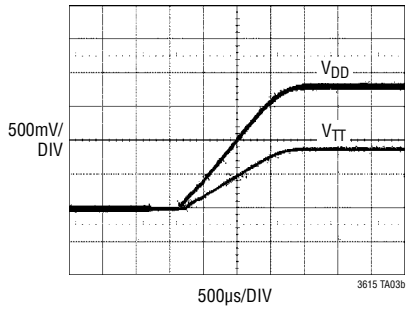


TYPICAL APPLICATIONS

DDR Memory Termination

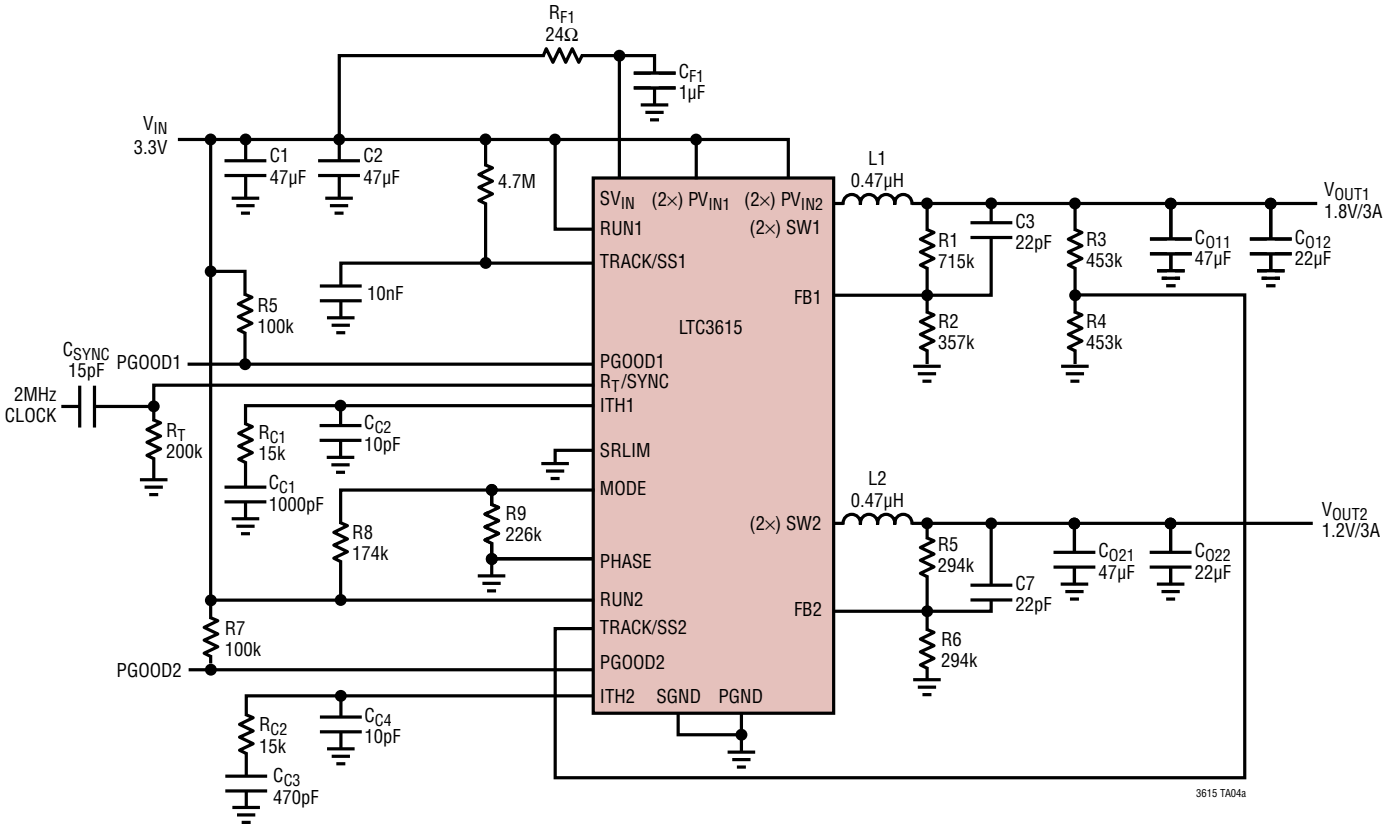


Ratiometric Start-Up

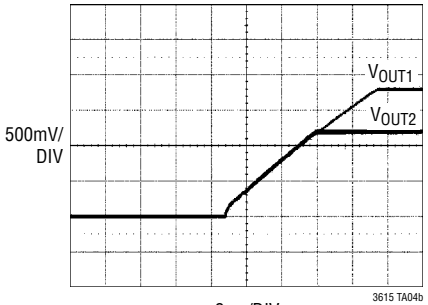


TYPICAL APPLICATIONS

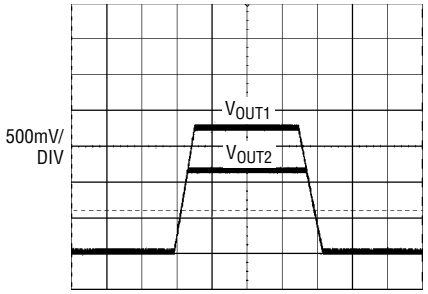
Master and Slave for Coincident Tracking Outputs Using a 2MHz External Clock



Coincident Start-Up

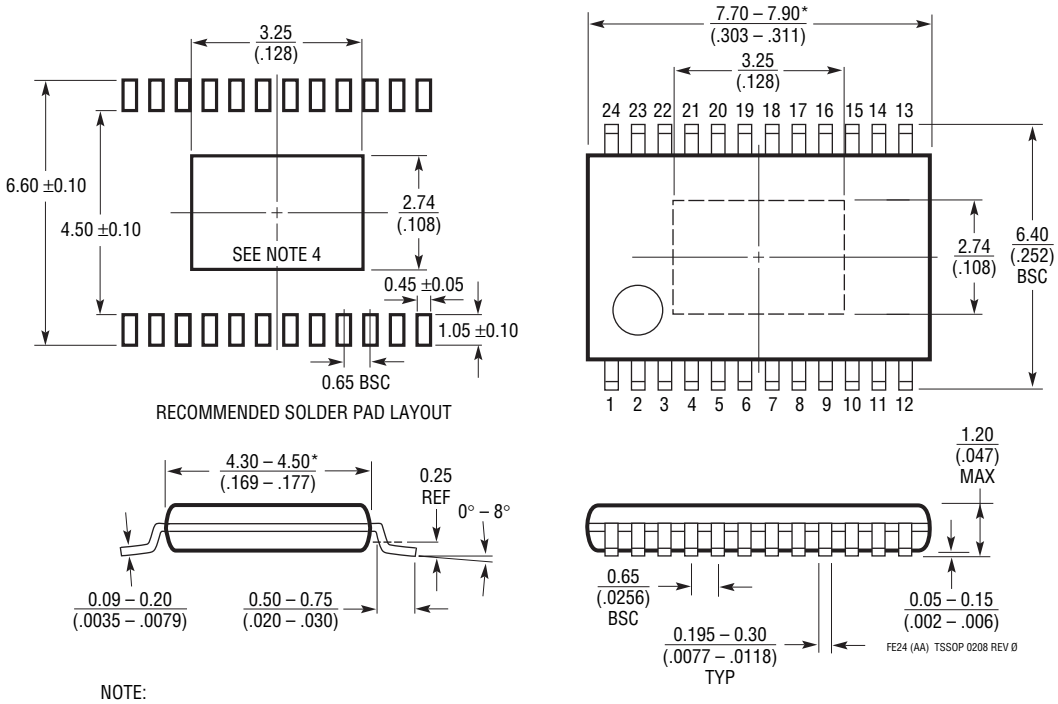


Coincident Tracking Up/Down



PACKAGE DESCRIPTION

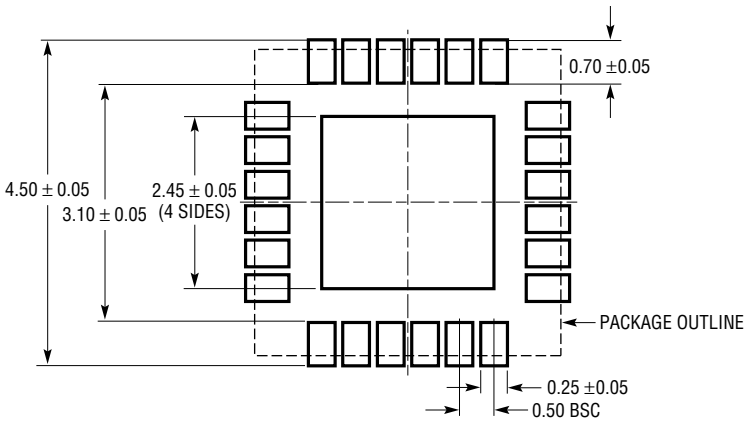
FE Package
24-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation AA



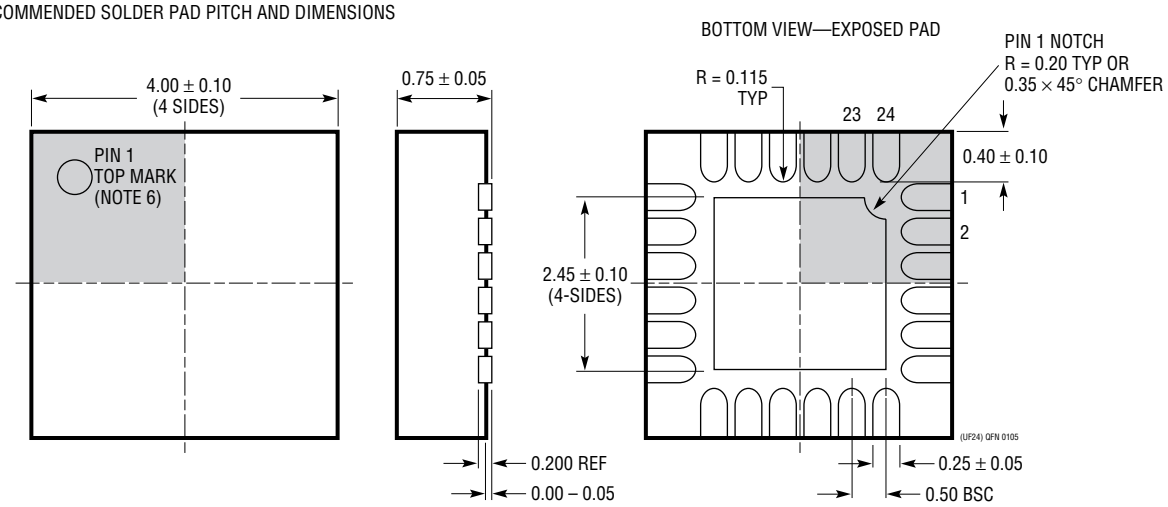
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

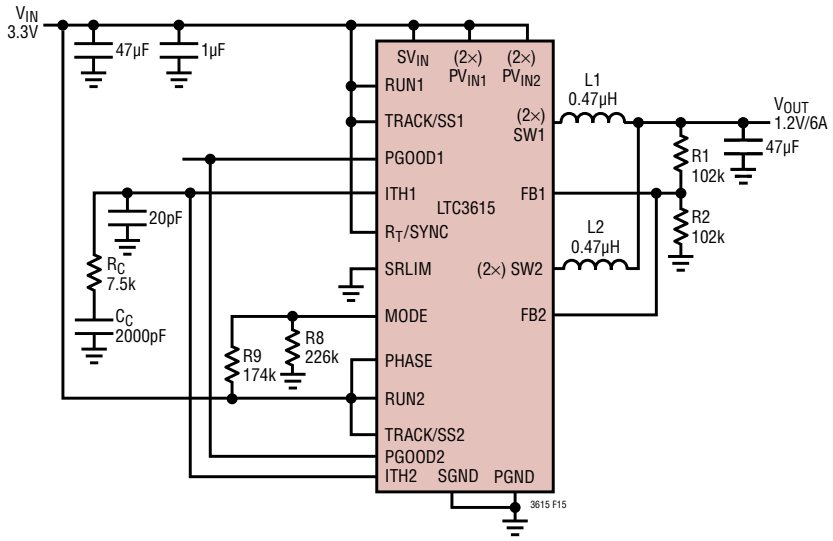


Figure 15. Single, Low Ripple 6A Output

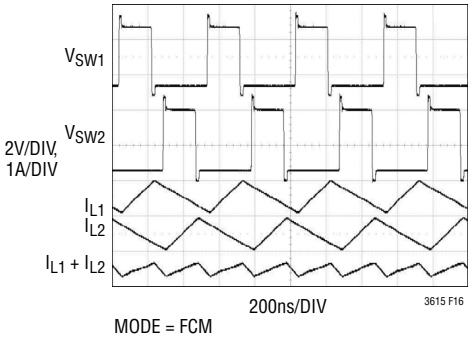


Figure 16. Reduced Ripple Current (Waveform $I_{L1} + I_{L2}$) and Ripple Voltage (Not Shown) Through 180° Phase Shift Between SW1 and SW2

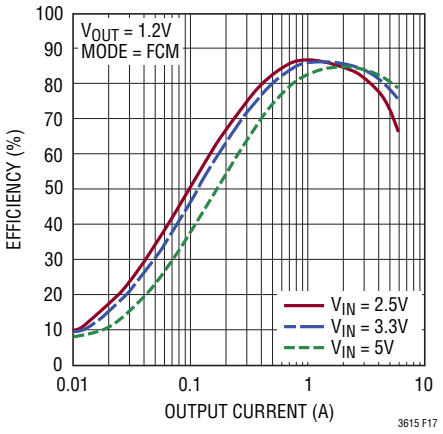


Figure 17. Efficiency vs Load Current for V_{OUT} = 1.2V and I_{OUT} Up to 6A

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3633	15V, Dual 3A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.60V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 500µA, I_{SD} < 13µA, 4mm × 5mm QFN-28 and TSSOP-28E Packages
LTC3546	5.5V, Dual 3A/1A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 160µA, I_{SD} < 1µA, 4mm × 5mm QFN-28 Package
LTC3417A-2	5.5V, Dual 1.5A/1A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 125µA, I_{SD} < 1µA, TSSOP-16E and 3mm × 5mm DFN-16 Packages
LTC3612	5.5V, 3A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 4mm QFN-20 and TSSOP-20E Packages
LTC3614	5.5V, 4A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 4mm QFN-20 and TSSOP-20E Packages
LTC3616	5.5V, 6A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 5mm QFN-24 Package

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