LTC3544

Quad Synchronous Step-Down Regulator: 2.25MHz, 300mA, 200mA, 200mA, 100mA

FEATURES

- **High Efficiency: Up to 95%**
- **Four Independent Regulators Provide Up to 300mA, 200mA, 200mA and 100mA Output Current**
- **2.25V to 5.5V Input Voltage Range**
- **2.25MHz Constant-Frequency Operation**
- **No Schottky Diodes Required**
- **Extremely Low Channel-to-Channel Transient Crosstalk**
- **Low Ripple (20mV$_{P-P}$) Burst Mode Operation: I_Q = 70µA (All Channels On)**
- Low Output Voltages
- Shutdown Mode Draws <1µA Supply Current
- Current Mode Operation for Excellent Line and Load Transient Response
- Overtemperature Protected
- Low Profile (3mm × 3mm) 16-Lead QFN Package

APPLICATIONS

- Cellular Telephones
- Personal Information Appliances
- Wireless and DSL Modems
- Digital Still Cameras
- Media Players
- Portable Instruments

DESCRIPTION

The LTC®3544 is a quad, high efficiency, monolithic synchronous buck regulator using a constant-frequency, current mode architecture. The four regulators operate independently with separate run pins. The 2.25V to 5.5V input voltage range makes the LTC3544 well suited for single Li-Ion/polymer battery-powered applications. 100% duty cycle provides low dropout operation, extending battery runtime in portable systems. Low ripple Burst Mode® operation increases efficiency at light loads, further extending battery runtime with typically only 20mV of ripple.

Switching frequency is internally set to 2.25MHz, allowing the use of small surface mount inductors and capacitors. The internal synchronous switches increase efficiency and eliminate the need for external Schottky diodes. Low output voltages are easily supported with the 0.8V feedback reference voltage.

The LTC3544 is available in a low profile (0.75mm) (3mm × 3mm) QFN package.

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TYPICAL APPLICATION

High Efficiency Quad Step-Down Converter
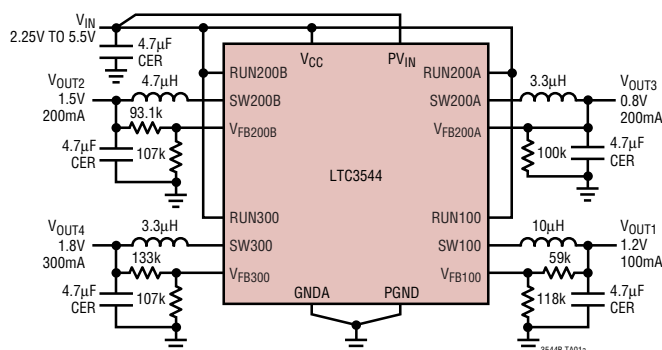
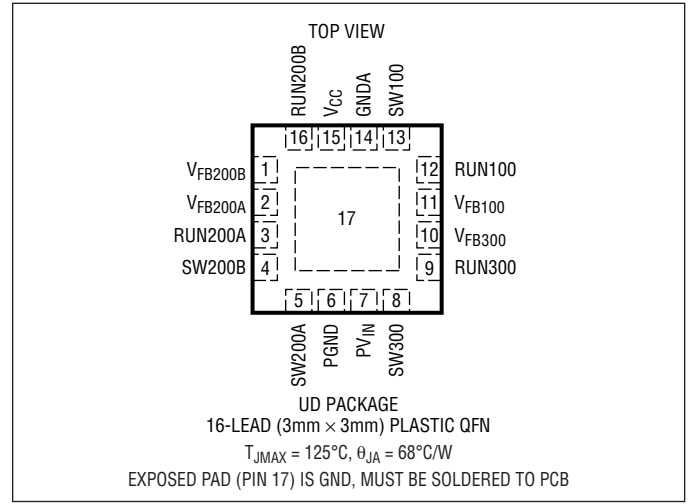**Efficiency vs Load Current, 300mA Channel, All Other Channels Off**

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1
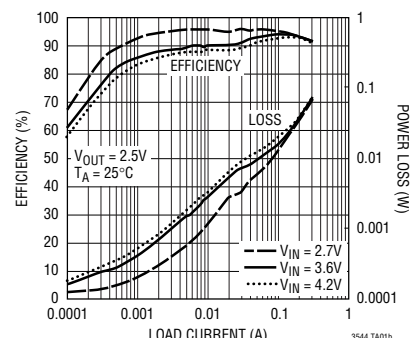
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage ....–0.3V to 6V
RUNx .... –0.3V to (V$_{IN}$ + 0.3V)
V$_{FBx}$.. –0.3V to (V$_{IN}$ + 0.3V)
SWx .... –0.3V to (V$_{IN}$ + 0.3V)
300mA P-Channel Source Current (DC) (Note 8) ..450mA
300mA N-Channel Sink Current (DC) (Note 8) 450mA
200mA P-Channel Source Current (DC) (Note 8) ..300mA
200mA N-Channel Sink Current (DC) (Note 8) 300mA
100mA P-Channel Source Current (DC) (Note 8) ..200mA
100mA N-Channel Sink Current (DC) (Note 8) 200mA
Peak 300mA SW Sink and Source Current
(Note 8)..600mA
Peak 200mA SW Sink and Source Current
(Note 8)..400mA
Peak 100mA SW Sink and Source Current
(Note 8)..200mA
Operating Temperature Range ....–40°C to 85°C
Junction Temperature (Notes 3, 4) .... 125°C
Storage Temperature Range ....–65°C to 125°C

PIN CONFIGURATION

TOP VIEW

RUN200B V$_{CC}$ GNDA SW100

16 | 15 | 14 | 13

V$_{FB200B}$ 1 — 12 RUN100
V$_{FB200A}$ 2 — 11 V$_{FB100}$
RUN200A 3 — 17 — 10 V$_{FB300}$
SW200B 4 — 9 RUN300

5 | 6 | 7 | 8

SW200A PGND PV$_{IN}$ SW300

UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
T$_{JMAX}$ = 125°C, θ$_{JA}$ = 68°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3544EUD#PBF	LTC3544EUD#TRPBF	LCXM	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3544EUD	LTC3544EUD#TR	LCXM	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T$_A$ = 25°C. V$_{IN}$ = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
General Characteristics							
V$_{IN}$	Input Voltage Range		●	2.25		5.5	V
V$_{FBREGx}$	Regulated Feedback Voltage (Note 5)		●	0.792 0.784	0.8 0.8	0.808 0.816	V V
ΔV$_{FBREGx}$	Reference Voltage Line Regulation (Note 5)	V$_{IN}$ = 2.25V to 5.5V			0.05	0.25	%/V
V$_{LOADREG}$	Output Voltage Load Regulation (Note 6)				0.5		%

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	Input DC Bias Current Active Mode (Four Regulators Enabled)	V_{FB} = 0.7V, I_{LOAD} = 0A, 2.25MHz			825	1100	µA
	Sleep Mode (Four Regulators Enabled)	V_{FB} = 0.9V, I_{LOAD} = 0A, 2.25MHz			70	80	µA
	Shutdown				0.1	2	µA
f_{OSC}	Oscillator Frequency	V_{IN} = 3V V_{IN} = 2.5V to 5.5V	●	1.8	2.25	2.7	MHz MHz
$V_{RUN(HIGH)}$	RUNx Input High Voltage		●	1.0			V
$V_{RUN(LOW)}$	RUNx Input Low Voltage		●			0.3	V
I_{SWx}	SWx Leakage	V_{RUN} = 0V, V_{SW} = 0V or 5.5V, V_{IN} = 5.5V			±0.1	±1	µA
I_{RUNx}	RUN Leakage Current	V_{IN} = 5.5V	●		±0.1	±1	µA
I_{VFBx}	V_{FBx} Leakage Current					80	nA
t_{SS}	Soft-Start Period	V_{FB} = 7.5% to 92.5% Full Scale		650	875	1200	µs
V_{UVLO}	Undervoltage Lockout		●		1.9	2.25	V

Individual Regulator Characteristics

Regulator SW300 – 300mA

I_{PK}	Peak Switch Current Limit	V_{FB} < V_{FBREG}, Duty Cycle < 35%		400	600	800	mA
I_{S300}	Input DC Bias Current–Reg SW300 Only Burst Mode Operation (Sleep)	V_{FB} = 0.9V, I_{LOAD} = 0A, 2.25MHz			32		µA
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET (Note 7)	I_{SW} = 100mA			0.55		Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET (Note 7)	I_{SW} = −100mA			0.50		Ω

Regulator SW200A – 200mA

I_{PK}	Peak Switch Current Limit	V_{FB} < V_{FBREG}, Duty Cycle < 35%		300	400	500	mA
I_{S200}	Input DC Bias Current–Reg SW200A Only Burst Mode Operation (Sleep)	V_{FB} = 0.9V, I_{LOAD} = 0A, 2.25MHz			32		µA
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET (Note 7)	I_{SW} = 100mA			0.65		Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET (Note 7)	I_{SW} = −100mA			0.60		Ω

Regulator SW200B – 200mA

I_{PK}	Peak Switch Current Limit	V_{FB} < V_{FBREG}, Duty Cycle < 35%		300	400	500	mA
I_{S200}	Input DC Bias Current–Reg SW200B Only Burst Mode Operation (Sleep)	V_{FB} = 0.9V, I_{LOAD} = 0A, 2.25MHz			32		µA
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET (Note 7)	I_{SW} = 100mA			0.65		Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET (Note 7)	I_{SW} = −100mA			0.60		Ω

Regulator SW100 – 100mA

I_{PK}	Peak Switch Current Limit	V_{FB} < V_{FBREG}, Duty Cycle < 35%		200	300	400	mA
I_{S100}	Input DC Bias Current–Reg SW100B Only Burst Mode Operation (Sleep)	V_{FB} = 0.9V, I_{LOAD} = 0A, 2.25MHz			32		µA
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET (Note 7)	I_{SW} = 100mA			0.80		Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET (Note 7)	I_{SW} = −100mA			0.75		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3544E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

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ELECTRICAL CHARACTERISTICS

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D)(68°C/W)$.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: The LTC3544 is tested in a proprietary test mode that connects V_{FB} to the output of the error amplifier.

Note 6: Load regulation is inferred by measuring the regulation loop gain.

Note 7: The QFN switch on-resistance is guaranteed by correlation to wafer level measurements.

Note 8: Guaranteed by long-term current density limitations.

TYPICAL PERFORMANCE CHARACTERISTICS

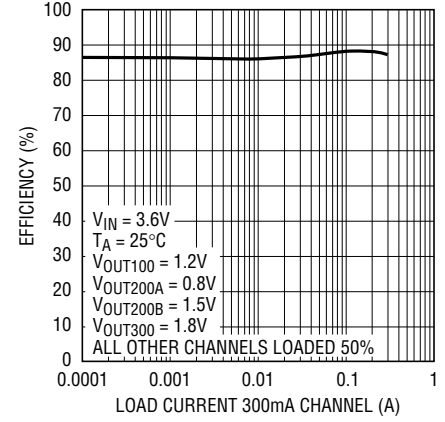**V_{REF} vs Temperature at 2.25V, 3.6V, 5.5V**
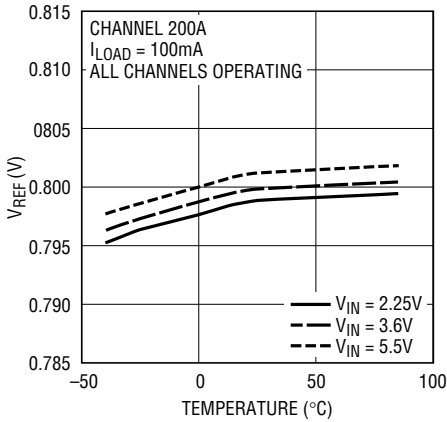
3544 G01

Switching Frequency vs Supply Voltage and Temperature
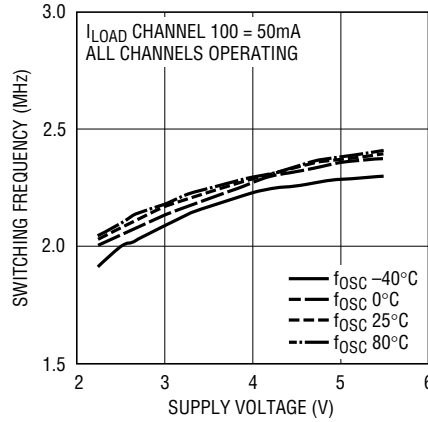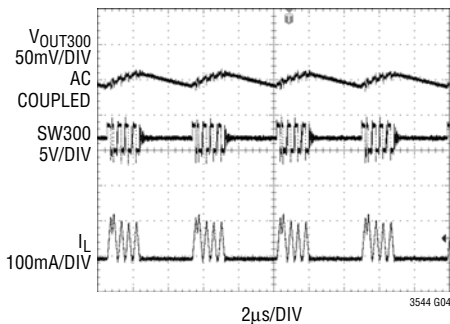

3544 G02

Efficiency vs Load Current 300mA Channel. All Other Channels at 50% Peak Current
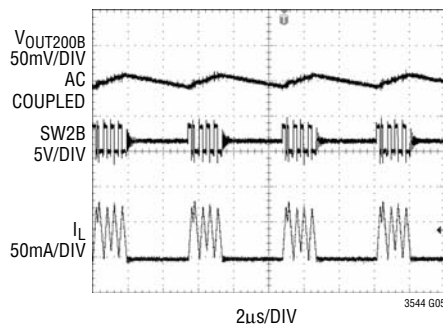

3544B G03

Burst Mode Operation 300mA Channel
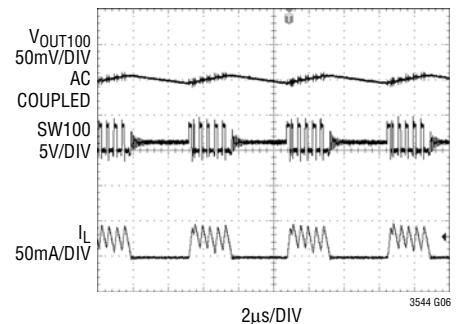

3544 G04

$V_{IN} = 3.6V$ $T_A = 25°C$
$V_{OUT} = 1.8V$ $I_{LOAD} = 20mA$

Burst Mode Operation 200mA, A-B Channels

3544 G05

$V_{IN} = 3.6V$ $T_A = 25°C$
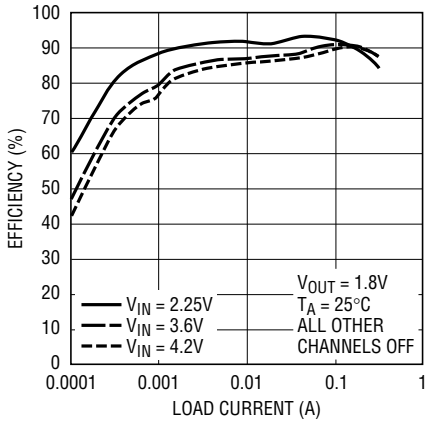$V_{OUT} = 1.5V$ $I_{LOAD} = 15mA$

Burst Mode Operation 100mA Channel

3544 G06

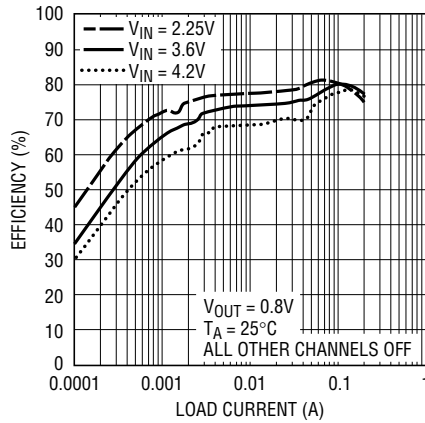$V_{IN} = 3.6V$ $T_A = 25°C$
$V_{OUT} = 1.2V$ $I_{LOAD} = 12mA$

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TYPICAL PERFORMANCE CHARACTERISTICS

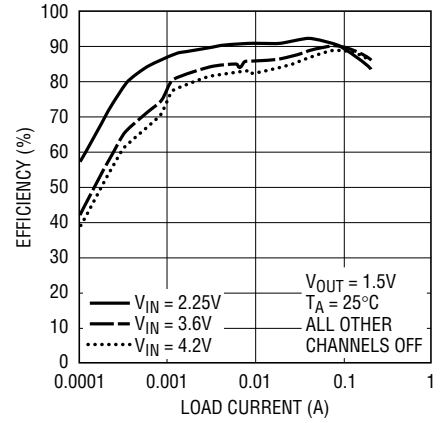**Efficiency vs Load Current 300mA Channel. All Other Channels Off**

V_IN = 2.25V
V_IN = 3.6V
V_IN = 4.2V

V_OUT = 1.8V
T_A = 25°C
ALL OTHER CHANNELS OFF

3544 G07

Efficiency vs Load Current 200mA Channel A. All Other Channels Off

V_IN = 2.25V
V_IN = 3.6V
V_IN = 4.2V

V_OUT = 0.8V
T_A = 25°C
ALL OTHER CHANNELS OFF

3544 G08

Efficiency vs Load Current 200mA Channel B. All Other Channels Off

V_IN = 2.25V
V_IN = 3.6V
V_IN = 4.2V

V_OUT = 1.5V
T_A = 25°C
ALL OTHER CHANNELS OFF

3544 G09

Efficiency vs Load Current 100mA Channel. All Other Channels Off

V_IN = 2.25V
V_IN = 3.6V
V_IN = 4.2V

V_OUT = 1.2V
T_A = 25°C
ALL OTHER CHANNELS OFF
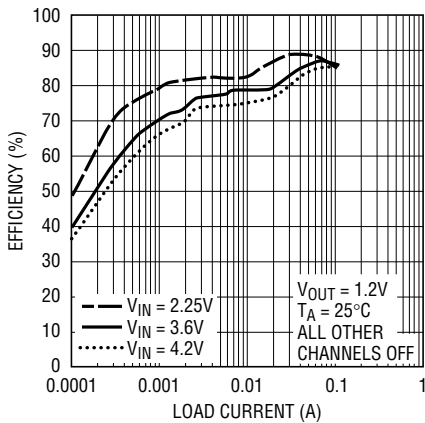
3544 G10

Load Regulation All Channels

100mA = 1.2V
200mA (A) = 0.8V
200mA (B) = 1.5V
300mA = 1.8V

V_IN = 3.6V
T_A = 25°C

Burst Mode OPERATION RIPPLE
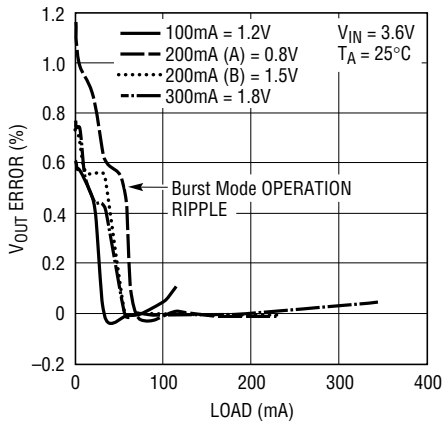
3544 G11

Start-Up Curves All Channels

V_OUT100
V_OUT200A
V_OUT200B
V_OUT300
RUNx

V_IN = 3.6V   200μs/DIV
T_A = 25°C
ALL CHANNELS UNLOADED
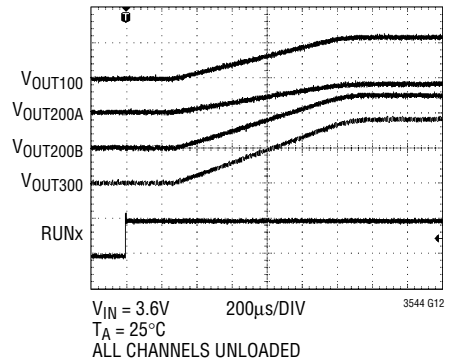
3544 G12

Load Step Response 300mA Channel

V_OUT300
100mV/DIV
AC
COUPLED

I_L
250mA/DIV

I_LOAD
250mA/DIV

V_IN = 3.6V   20μs/DIV
V_OUT = 1.8V
T_A = 25°C
I_LOAD = 600μA TO 300mA
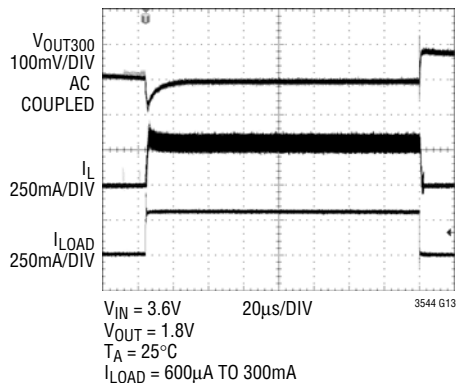
3544 G13

Load Step Response 200mA Channel A

V_OUT200A
50mV/DIV
AC
COUPLED

I_L
250mA/DIV

I_LOAD
250mA/DIV

V_IN = 3.6V   20μs/DIV
V_OUT = 0.8V
T_A = 25°C
I_LOAD = 600μA TO 200mA
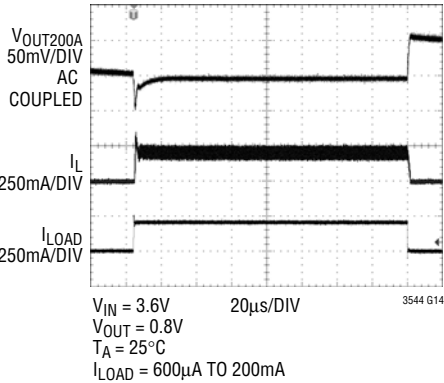
3544 G14

Load Step Response 200mA Channel B

V_OUT200B
50mV/DIV
AC COUPLED

I_L
250mA/DIV

I_LOAD
250mA/DIV

V_IN = 3.6V   20μs/DIV
V_OUT = 1.5V
T_A = 25°C
I_LOAD = 600μA TO 200mA

3544 G15

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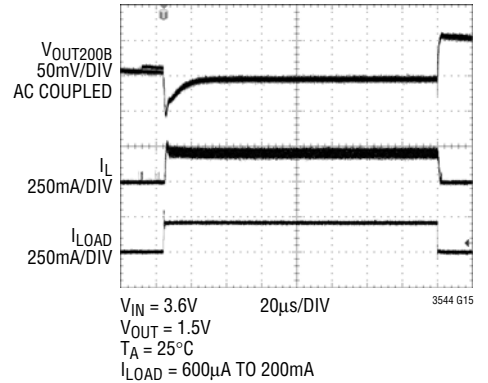
TYPICAL PERFORMANCE CHARACTERISTICS

Load Step Response 100mA Channel

V_{OUT100}
50mV/DIV
AC COUPLED

I_L
100mA/DIV

I_{LOAD}
100mA/DIV

$V_{IN} = 3.6V$ 20μs/DIV   3544 G16
$V_{OUT} = 1.2V$
$T_A = 25°C$
$I_{LOAD} = 400μA$ TO 100mA

Load Step Crosstalk

V_{OUT100}
1mV/DIV

$V_{OUT200A}$
1mV/DIV

$V_{OUT200B}$
1mV/DIV

V_{OUT300}
50mV/DIV

$V_{IN} = 3.6V$ 40μs/DIV   3544 G17
$T_A = 25°C$
300mA LOAD STEP ON V_{OUT300}
OTHER CHANNELS LOADED 50% OF MAXIMUM

PFET $R_{DS(ON)}$ vs Supply Voltage

$T_A = 25°C$

y-axis: $R_{DS(ON)}$ (Ω), 0 to 1.2
x-axis: V_{IN} (V), 2 to 6

300
200B
200A
100
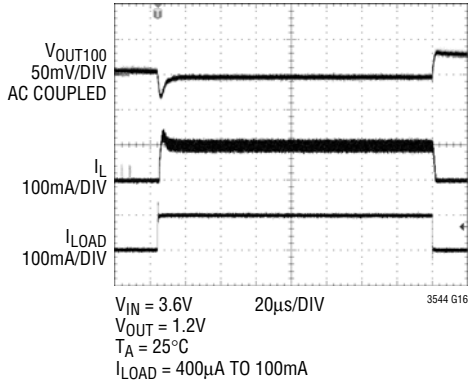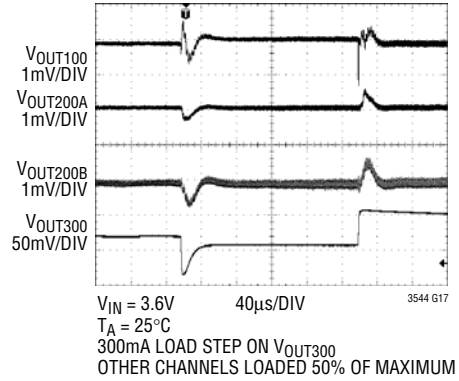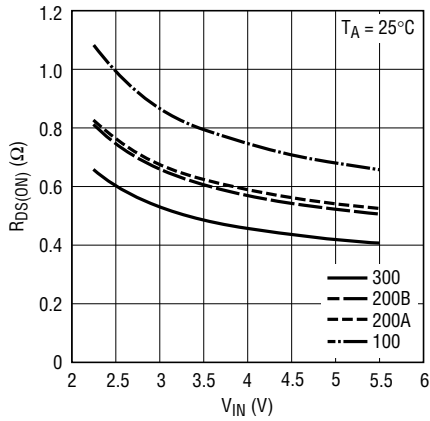
3544 G16

NFET $R_{DS(ON)}$ vs Supply Voltage

$T_A = 25°C$

y-axis: $R_{DS(ON)}$ (Ω), 0 to 1.0
x-axis: V_{IN} (V), 2 to 6

300
200B
200A
100
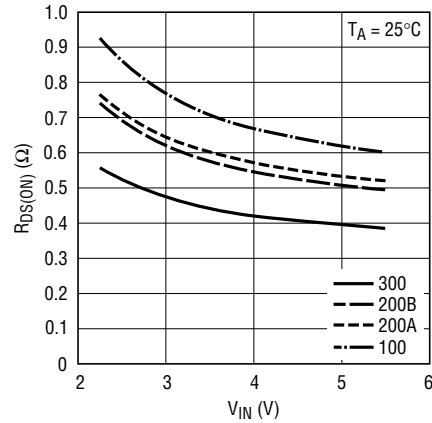
3544 G17

PFET $R_{DS(ON)}$ vs Temperature

$V_{IN} = 3.6V$

y-axis: $R_{DS(ON)}$ (Ω), 0 to 1.0
x-axis: TEMPERATURE (°C), −50 to 90

300
200B
200A
100
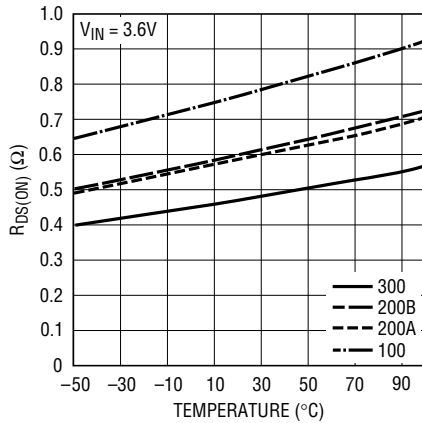
3544 G18

NFET $R_{DS(ON)}$ vs Temperature

$V_{IN} = 3.6V$

y-axis: $R_{DS(ON)}$ (Ω), 0 to 1.0
x-axis: TEMPERATURE (°C), −50 to 100

300
200B
200A
100

3544 G19

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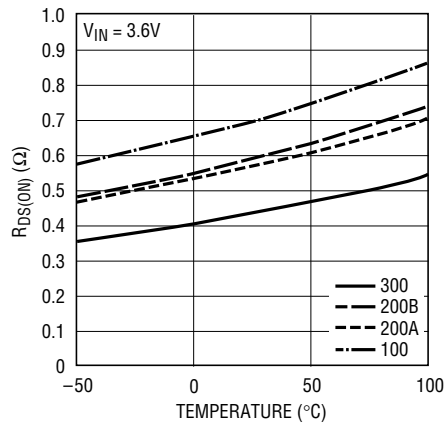
PIN FUNCTIONS

V_{FB200B} **(Pin 1):** 200mA Regulator B Feedback Pin. This pin receives the feedback voltage from an external resistive divider across the output.

V_{FB200A} **(Pin 2):** 200mA Regulator A Feedback Pin. This pin receives the feedback voltage from an external resistive divider across the output.

RUN200A (Pin 3): 200mA Regulator A Enable Pin. Forcing this pin to V_{IN} enables the 200mA regulator (channel A), while forcing it to GND causes the regulator to shut off.

SW200B (Pin 4): Switch Node Connection to Inductor for 200mA Regulator B. This pin connects to the drains of the internal power MOSFET switches.

SW200A (Pin 5): Switch Node Connection to Inductor for 200mA Regulator A. This pin connects to the drains of the internal power MOSFET switches.

PGND (Pin 6): Power Path Return Pin for Both 200mA Regulators and the 300mA Regulator.

PV$_{IN}$ (Pin 7): Power Path Supply Pin for Both 200mA Regulators and the 300mA Regulator. This pin must be closely decoupled to PGND, with a 4.7µF or greater ceramic capacitor.

SW300 (Pin 8): Switch Node Connection to Inductor for 300mA Regulator. This pin connects to the drains of the internal power MOSFET switches.

RUN300 (Pin 9): 300mA Regulator Enable Pin. Forcing this pin to V_{IN} enables the 300mA regulator, while forcing it to GND causes the regulator to shut off.

V_{FB300} **(Pin 10):** 300mA Regulator Feedback Pin. This pin receives the feedback voltage from an external resistive divider across the output.

V_{FB100} **(Pin 11):** 100mA Regulator Feedback Pin. This pin receives the feedback voltage from an external resistive divider across the output.

RUN100 (Pin 12): 100mA Regulator Enable Pin. Forcing this pin to V_{IN} enables the 100mA regulator, while forcing it to GND causes the 100mA regulator to shut off.

SW100 (Pin 13): Switch Node Connection to Inductor for 100mA Regulator. This pin connects to the drains of the internal power MOSFET switches.

GNDA (Pin 14): Ground Pin for Internal Reference and Control Circuitry. Power path return for the 100mA regulator.

V$_{CC}$ (Pin 15): Supply Pin for Internal Reference and Control Circuitry. Power path supply pin for the 100mA regulator.

RUN200B (Pin 16): 200mA Regulator B Enable Pin. Forcing this pin to V_{IN} enables the 200mA regulator (channel B), while forcing it to GND causes the regulator to shut off.

Exposed Pad (Pin 17): Ground. Must be soldered to PCB.

LTC3544

FUNCTIONAL DIAGRAMS
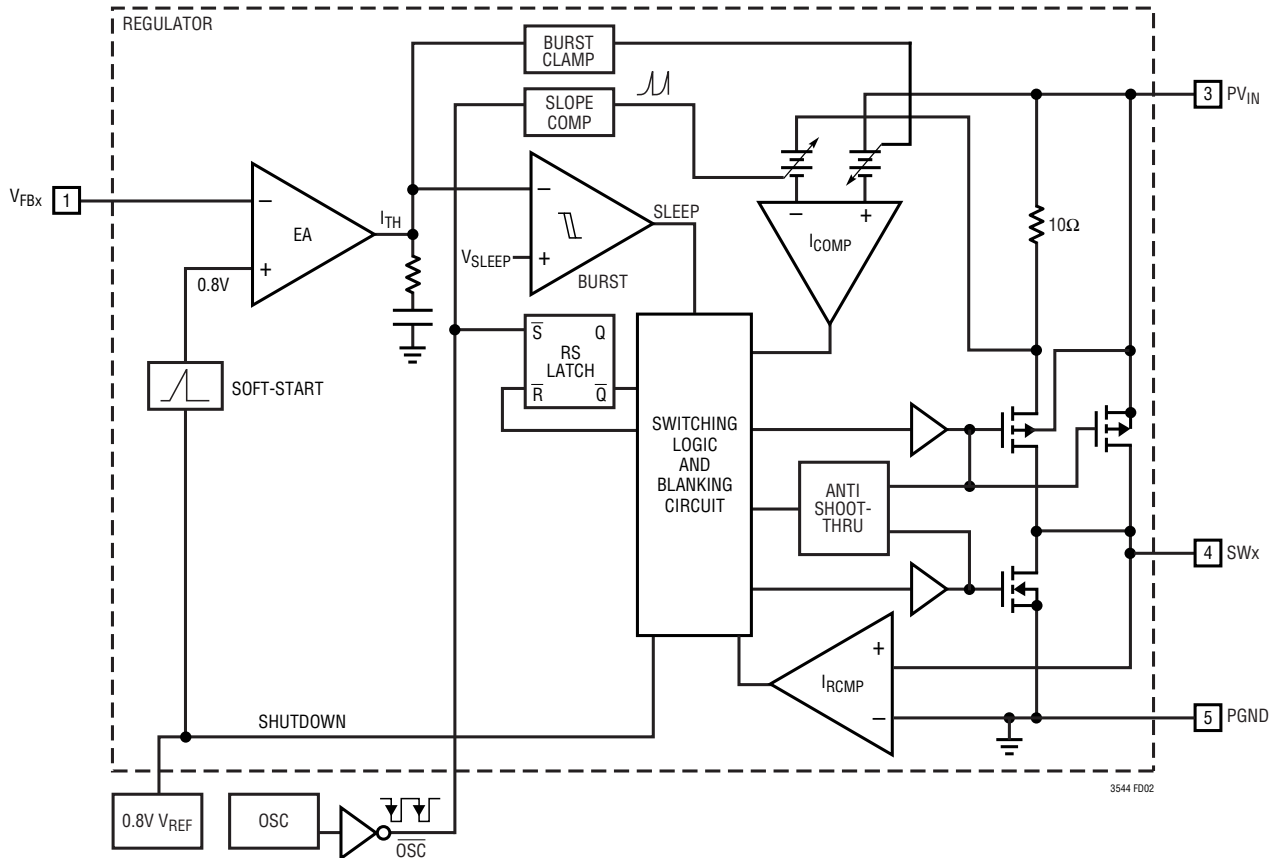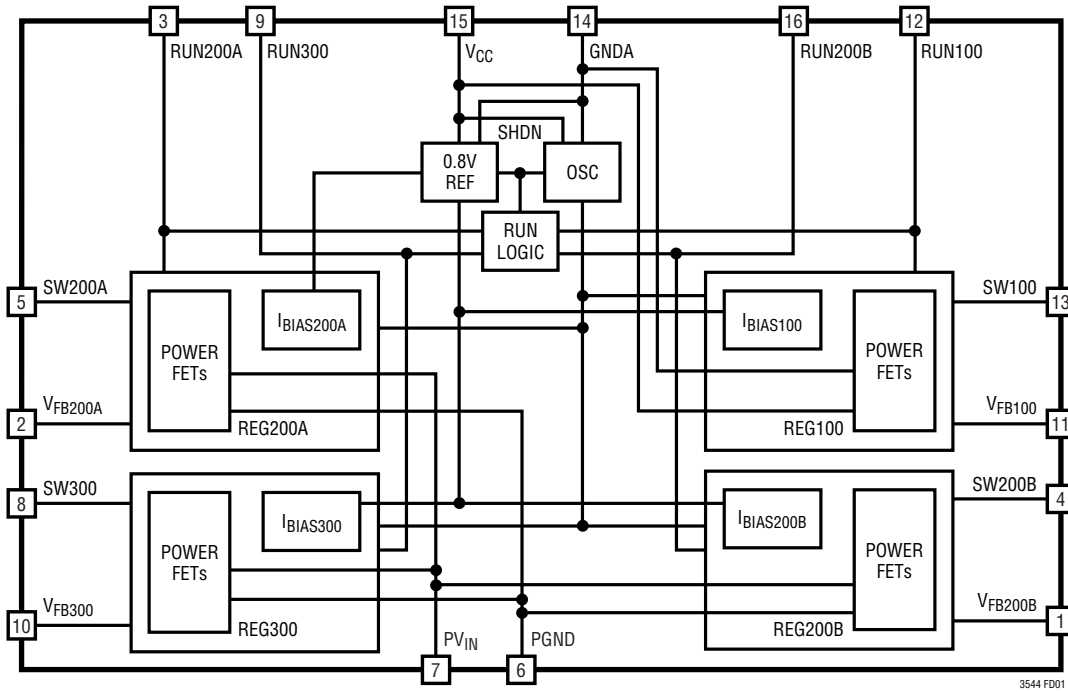
3544 FD01

3544 FD02

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OPERATION (Refer to Functional Diagrams)

The LTC3544 uses a constant-frequency current mode architecture. The operating frequency is set at 2.25MHz. All channels share the same clock and run in-phase.

The output voltage for each regulator is set by an external resistor divider returned to the V_{FB} pin. An error amplifier compares the divided output voltage with a reference voltage of 0.8V and regulates the peak inductor current accordingly.

Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle when the V_{FB} voltage is below the reference voltage. The current into the inductor and the load increases until the peak inductor current (controlled by I_{TH}) is reached. The RS latch turns off the top switch, turns on the bottom switch, and energy stored in the inductor is discharged through the bottom switch (N-channel MOSFET) into the load until the next clock cycle begins, or until the inductor current begins to reverse (sensed by the I_{RCMP} comparator).

The peak inductor current is controlled by the internally compensated I_{TH} voltage, which is the output of the error amplifier. This amplifier regulates the V_{FB} pin to the internal 0.8V reference by adjusting the peak inductor current accordingly.

Burst Mode Operation

To optimize efficiency, the LTC3544 automatically switches from continuous operation to Burst Mode operation when the load current is relatively light. During Burst Mode operation, the peak inductor current (as set by I_{TH}) remains fixed at a low level and the PMOS switch operates intermittently based on load demand. By running cycles periodically, the switching losses are minimized.

The duration of each burst event can range from a few cycles at light load to almost continuous cycling with short sleep intervals at moderate loads. During the sleep intervals, the load current is being supplied solely from the output capacitor. As the output voltage droops, the error amplifier output rises above the sleep threshold, signaling the burst comparator to trip and turn the top MOSFET on. This cycle repeats at a rate that is dependent on load demand.
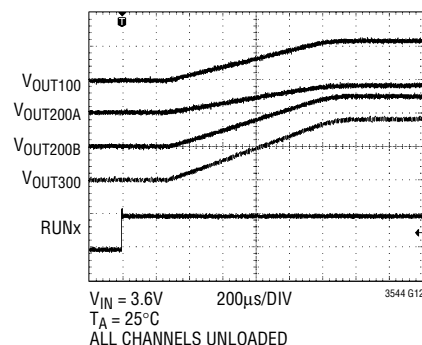

V_{IN} = 3.6V   200μs/DIV   3544 G12
T_A = 25°C
ALL CHANNELS UNLOADED

Figure 1. Regulator Soft-Start

Soft-Start

Soft-start reduces surge currents on V_{IN} and output overshoot during start-up. Soft-start on the LTC3544 is implemented by internally ramping the reference signal fed to the error amplifier over approximately a 1ms period. Figure 1 shows the behavior of the four regulator channels during soft-start.

Short-Circuit Protection

Short-circuit protection is achieved by monitoring the inductor current. When the current exceeds a predetermined level, the main switch is turned off, and the synchronous switch is turned on long enough to allow the current in the inductor to decay below the fault threshold. This prevents a catastrophic inductor current, run-away condition, but will still provide current to the output. Output voltage regulation in this condition is not achieved.

DROPOUT OPERATION

As the input supply voltage decreases to a value approaching the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor. An important detail to remember is that at low input supply voltages, the $R_{DS(ON)}$ of the P-channel switch increases (see Typical Performance Characteristics). Therefore, the user should calculate the power dissipation when the LTC3544 is used at 100% duty cycle with low input voltage (see Thermal Considerations in the Applications Information section).

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The basic LTC3544 application circuit is shown on the first page of this data sheet. External component selection is driven by the load requirement and begins with the selection of L followed by C_{IN} and C_{OUT}.

Inductor Selection

For most applications, the value of the inductor will fall in the range of 1µH to 10µH. Its value is chosen based on the desired ripple current. Large inductor values lower ripple current and small inductor values result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in Equation 1. A reasonable starting point for setting ripple current for the 300mA regulator is ΔI_L = 120mA (40% of 300mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \qquad (1)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 360mA rated inductor should be enough for most applications (300mA + 60mA). For better efficiency, choose a low DCR inductor.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the LTC3544 requires to operate. Table 1 shows typical surface mount inductors that work well in LTC3544 applications.

Table 1. Representative Surface Mount Inductors

Part Number	Value (µH)	DCR (Ω MAX)	MAX DC CURRENT (A)	W × L × H (mm³)
Sumida CDH2D09B	10	0.47	0.48	3.0 × 2.8 × 1.0
	6.4	0.32	0.6	
	4.7	0.218	0.7	
	3.3	0.15	0.85	
Wurth TPC744029	10	0.50	0.50	2.8 × 2.8 × 1.35
	6.8	0.38	0.65	
	4.7	0.210	0.80	
	3.3	0.155	0.95	
TDK VLF3010AT	10	0.67	0.49	2.8 × 2.6 × 1.0
	6.8	0.39	0.61	
	4.7	0.28	0.70	
	3.3	0.17	0.87	

C_{IN} and C_{OUT} Selection

In continuous mode, a worst-case estimate for the input current ripple can be determined by assuming that the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}, and amplitude $I_{OUT(MAX)}$. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life (non-ceramic capacitors). This makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output

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voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Using Ceramic Input and Output Capacitors

Higher value, lower cost, ceramic capacitors are now widely available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3544's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

However, care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN}, large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage charac-teristics of all the ceramics for a given value and size.

Output Voltage Programming

The output voltage is set by tying V_{FB} to a resistive divider according to the following formula:

$$V_{OUT} = 0.8V\left(1 + \frac{R2}{R1}\right)$$

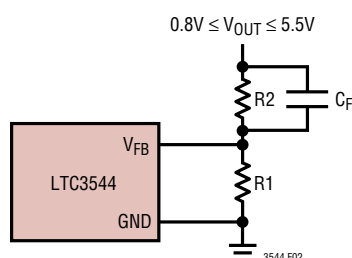The external resistive divider is connected to the output allowing remote voltage sensing as shown in Figure 2.

Figure 2. Setting the LTC3544 Output Voltage

Keeping the current in the resistors small maximizes the efficiency, but making them too small may allow stray capacitance to cause noise problems or reduce the phase margin of the control loop. It is recommended that the total feedback resistor string be kept to under 100k.

To improve the frequency response of the control loop, a feed forward capacitor, C_F, may be used. Great care should be taken to route the feedback line away from noise sources such as the inductor of the SW line.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: Efficiency = 100% – (L1 + L2 + L3 + ...) where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses in LTC3544 circuits: V_{IN} quiescent current and I^2R losses. V_{IN} quiescent current loss dominates the efficiency loss at low load currents, whereas the I^2R loss dominates the efficiency loss at medium to high load currents.

1. The quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, dQ, moves from PV_{IN} to ground. The resulting dQ/dt is the current out of PV_{IN} that is typically larger than the DC bias current and proportional to frequency. Both the DC bias and gate charge losses are proportional to PV_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both

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top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses when in switching operation, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% total additional loss.

Thermal Considerations

The LTC3544 requires the package backplane metal to be well soldered to the PC board. This gives the QFN package exceptional thermal properties, making it difficult in normal operation to exceed the maximum junction temperature of the part. In most applications the LTC3544 does not dissipate much heat due to its high efficiency. In applications where the LTC3544 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part if it is not well thermally grounded. If the junction temperature reaches approximately 150°C, the power switches will be turned off and the SW nodes will become high impedance.

To avoid the LTC3544 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = P_D \cdot \theta_{JA}$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

As an example, consider the LTC3544 in dropout at an input voltage of 2.5V, a total load current (all four regulators) of 800mA and an ambient temperature of 85°C. From the Typical Performance graphs of switch resistance, the $R_{DS(ON)}$ of the 300mA P-channel switch at 85°C can be estimated as 0.67Ω. Therefore, power dissipated by the 300mA channel is:

$$P_D = I_{LOAD}^2 \cdot R_{DS(ON)} = 60mW$$

Similar analysis on the other channels gives a total power dissipation of 138mW. For the 3mm × 3mm QFN package, the θ_{JA} is 68°C/W. Thus, the junction temperature of the regulator is:

$$T_J = 85°C + (0.138)(68) = 94.4°C$$

which is well below the maximum junction temperature of 125°C.

Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance $R_{DS(ON)}$.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ($\Delta I_{LOAD} \cdot ESR$), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal. The regulator loop then acts to return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. For a detailed explanation of switching control loop theory, see Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25 • C_{LOAD}). Thus, a 10µF capacitor charging to 3.3V would require a 250µs rise time, limiting the charging current to about 130mA.

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PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3544. These items are also illustrated graphically in Figures 3 and 4. Check the following in your layout:

1. The power traces, consisting of the PGND trace, the GNDA trace, the SW traces, the PV_{IN} trace and the V_{CC} trace should be kept short, direct and wide.

2. Does each of the V_{FBx} pins connect directly to the respective feedback resistors? The resistive dividers must be connected between the (+) plate of the corresponding output filter capacitor (e.g., C13) and GNDA. If the circuit being powered is at such a distance from the part where voltage drops along circuit traces are large, consider a Kelvin connection from the powered circuit back to the resistive dividers.

3. Keep C8 and C9 as close to the part as possible.

4. Keep the switching nodes (SWx) away from the sensitive V_{FBx} nodes.

5. Keep the ground connected plates of the input and output capacitors as close as possible.

6. Care should be taken to provide enough space between unshielded inductors in order to minimize any transformer coupling.

Design Example

As a design example, consider using the LTC3544 as a portable application with a Li-Ion battery. The battery provides V_{IN} ranging from 2.8V to 4.2V. The demand at 2.5V is 250mA necessitating the use of the 300mA output for this requirement.
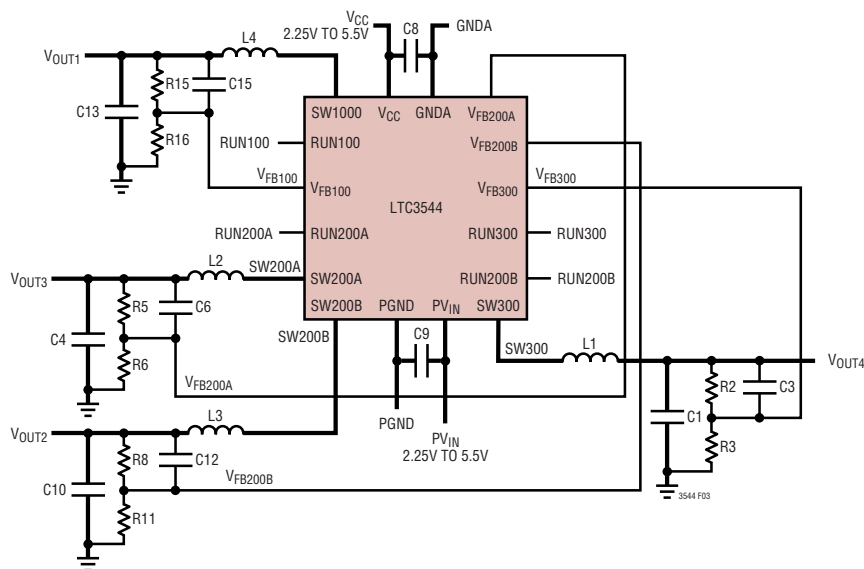

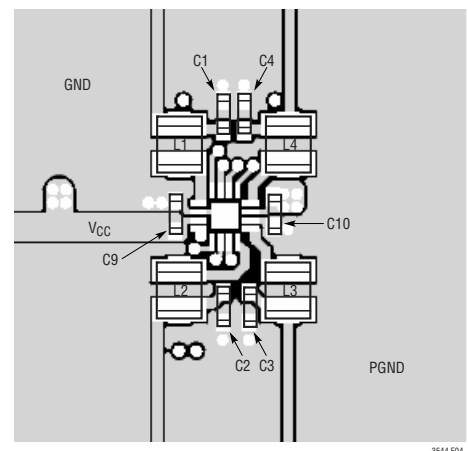**Figure 3. LTC3544 Layout Diagram**

Figure 4. LTC3544 Suggested Layout

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Beginning with this channel, first calculate the inductor value for about 35% ripple current (100mA in this example) at maximum V_{IN}. Using a form of Equation 1:

$$L4 = \frac{2.5V}{2.25MHz \cdot 100mA}\left(1 - \frac{2.5V}{4.2V}\right) = 4.5\mu H$$

For the inductor, use the closest standard value of 4.7µH. A 4.7µF capacitor should be sufficient for the output capacitor. A larger output capacitor will attenuate the load transient response, but increase the settling time. A value for C_{IN} = 4.7µF should suffice as the source impedance of a Li-Ion battery is very low.

The feedback resistors program the output voltage. Minimizing the current in these resistors will maximize efficiency at very light loads, but totals on the order of 200k are a good compromise between efficiency and immunity to any adverse effects of PCB parasitic capacitance on the feedback pins. Choosing 10µA with 0.8V feedback voltage makes R7 = 80k. A close standard 1% resistor is 76.8k. Using:

$$R8 = \left(\frac{V_{OUT}}{0.8} - 1\right) \cdot R7 = 163.2k$$

The closest standard 1% resistor is 162k. An optional 20pF feedback capacitor may be used to improve transient response. The component values for the other channels are chosen in a similar fashion.

Figure 5 shows the complete schematic for this example, along with the efficiency curve and transient response for the 300mA channel.
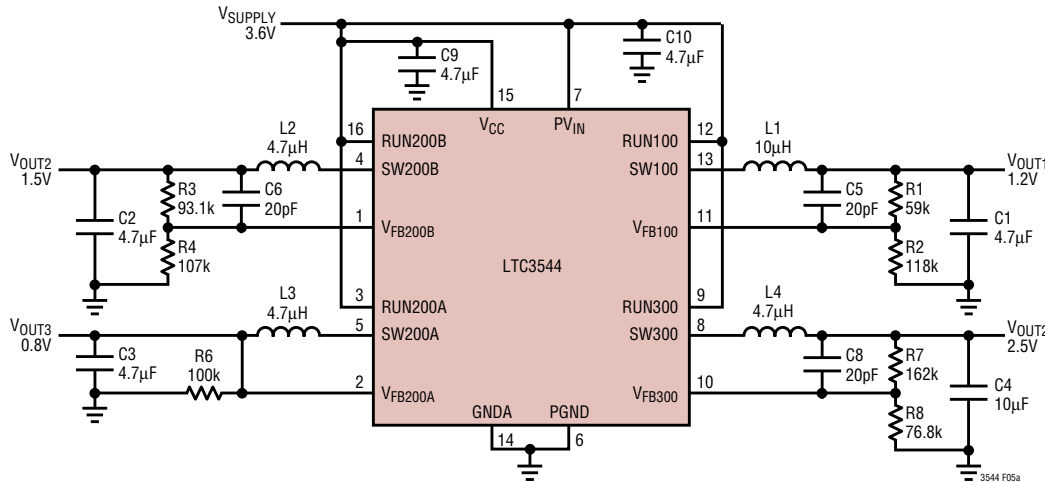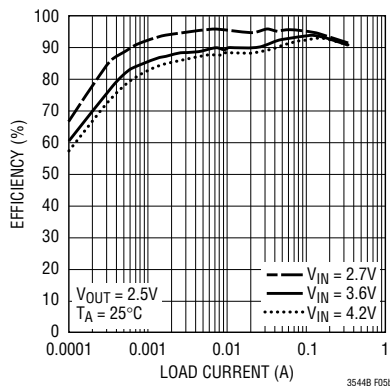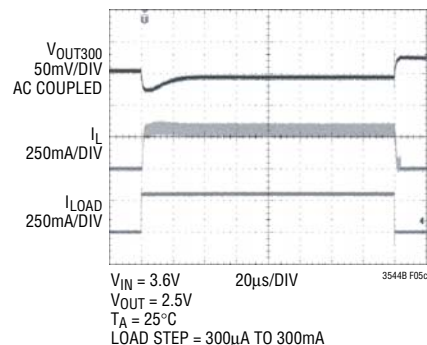
Figure 5. Design Example

Efficiency vs Output Current—300mA Channel, All Other Channels Off

Transient Response

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PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)

3.50 ± 0.05

2.10 ± 0.05

1.45 ± 0.05 (4 SIDES)

0.70 ±0.05

PACKAGE OUTLINE

0.25 ±0.05

0.50 BSC

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

3.00 ± 0.10 (4 SIDES)

0.75 ± 0.05

PIN 1 TOP MARK (NOTE 6)

1.45 ± 0.10 (4-SIDES)

0.200 REF

0.00 – 0.05

BOTTOM VIEW—EXPOSED PAD

R = 0.115 TYP

PIN 1 NOTCH R = 0.20 TYP OR 0.25 × 45° CHAMFER

15 16

0.40 ± 0.10

1

2

(UD16) QFN 0904

0.25 ± 0.05

0.50 BSC

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3405/LTC3405A	300mA I_{OUT}, 1.5MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT™ Package
LTC3406/LTC3406B	600mA I_{OUT}, 1.5MHz, Synchronous Step-Down DC/DC Converters	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3407/LTC3407-2	Dual 600mA/800mA I_{OUT}, 1.5MHz/2.25MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, 10-Lead MSE, DFN Packages
LTC3409	600mA I_{OUT}, 1.7MHz/2.6MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 1.6V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 65µA, I_{SD} < 1µA, DFN Package
LTC3410/LTC3410B	300mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 26µA, I_{SD} < 1µA, SC70 Package
LTC3411	1.25A I_{OUT}, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, 10-Lead MSE, DFN Packages
LTC3412	2.5A I_{OUT}, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, 16-Lead TSSOPE Package
LTC3441/LTC3442 LTC3443	1.2A I_{OUT}, 2MHz, Synchronous Buck-Boost DC/DC Converters	95% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MIN)}$: 2.4V to 5.25V, I_Q = 50µA, I_{SD} < 1µA, DFN Package
LTC3446	Monolithic Synchronous Buck Regulator with Dual VLDO™ Regulators	92% Efficiency, V_{IN}: 2.7V to 5.5V, $V_{OUT(MIN)}$ = 0.4V, I_Q = 140µA, I_{SD} < 1µA, 3mm × 4mm DFN Package
LTC3531/LTC3531-3 LTC3531-3.3	200mA I_{OUT}, 1.5MHz, Synchronous Buck-Boost DC/DC Converters	95% Efficiency, V_{IN}: 1.8V to 5.5V, $V_{OUT(MIN)}$: 2V to 5V, I_Q = 16µA, I_{SD} < 1µA, ThinSOT, DFN Packages
LTC3532	500mA I_{OUT}, 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MIN)}$: 2.4V to 5.25V, I_Q = 35µA, I_{SD} < 1µA, 10-Lead MSE, DFN Packages
LTC3544B	300mA, 2 × 200mA, 100mA Quad 2.25MHz Synchronous Buck DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 825µA, I_{SD} < 1mA, 3mm × 3mm QFN Package
LTC3547/LTC3547B	Dual 300mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, 8-Lead DFN Package
LTC3548/LTC3548-1 LTC3548-2	Dual 400mA/800mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, 10-Lead MSE, DFN Packages
LTC3561	1.25A I_{OUT}, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 240µA, I_{SD} < 1µA, DFN Package

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