2.7 V to 5.5 V, 250 µA, Rail-to-Rail Output 16-Bit *nano*DAC™ D/A in a SOT-23

Preliminary Technical Data

AD5662

FEATURES

Low power (250 µA @ 5 V) single 16-bit *nano*DAC™
True 12-bit accuracy guaranteed
Tiny 8-lead SOT-23/MSOP package
Power-down to 200 nA @ 5 V, 50 nA @ 3 V
Power-on-reset to zero/midscale
2.7 V to 5.5 V power supply
Guaranteed 16-bit monotonic by design
3 power-down functions
Serial interface with Schmitt-triggered inputs
Rail-to-rail operation
SYNC interrupt facility

APPLICATIONS

Process control
Data acquisition systems
Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators

FUNCTIONAL BLOCK DIAGRAM

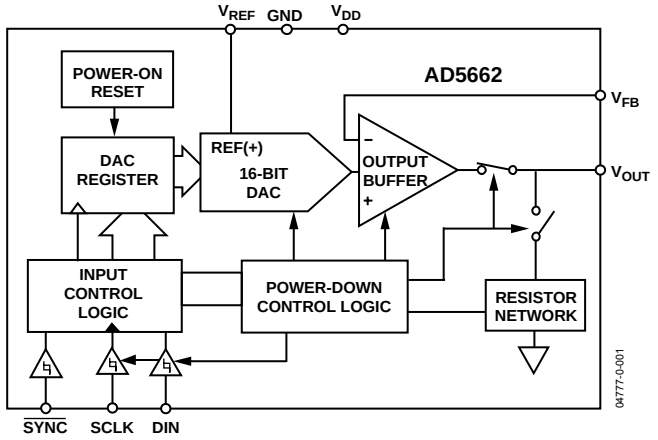

Figure 1.

GENERAL DESCRIPTION

The AD5662 parts are a member of the *nano*DAC™ family of devices. They are low power, single, 16-bit buffered voltage-out DACs. All devices operate from a single 2.7 V to 5.5 V, and are guaranteed monotonic by design.

The AD5662 requires an external reference voltage to set the output range of the DAC. The part incorporates a power-on-reset circuit that ensures the DAC output powers up to 0 V (AD5662x-1) or midscale (AD5662x-2), and remains there until a valid write takes place. The part contains a power-down feature that reduces the current consumption of the device to 200 nA at 5 V, and provides software selectable output loads while in power-down mode.

The low power consumption of this part in normal operation makes it ideally suited to portable battery-operated equipment. The power consumption is 0.7 mW at 5 V, reducing to 1 µW in power-down mode.

The AD5662's on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The AD5662 utilizes a versatile 3-wire serial interface that operates at clock rates up to 30 MHz, and is compatible with standard SPI™, QSPI™, MICROWIRE™, and DSP interface standards.

The AD5662 is designed with new technology, and is the next generation to the AD53xx family.

PRODUCT HIGHLIGHTS

1. 16-bit DAC; true 12-bit accuracy guaranteed.
2. Available in 8-lead SOT-23 and 8-lead MSOP package.
3. Power-on-reset to zero or midscale.
4. Low power. Operates with 2.7 V to 5.5 V supply. Typically consumes 0.35 mW at 3 V and 0.7 mW at 5 V, making it ideal for battery-powered applications.
5. Power-down capability. When powered down, the DAC typically consumes 50 nA at 3 V and 200 nA at 5 V.
6. 10 µs settling time.

RELATED DEVICES

Part No.	Description
AD5620/AD5640/AD5660	3 V/5 V 12-/14-/16-bit DAC with internal ref in Sot-23

Rev. PrA

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REVISION HISTORY

10/04—Revision PrA

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; V_{REF} = V_{DD}: all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	A Grade			B Grade				B Version[1]
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
STATIC PERFORMANCE[2]								
Resolution	16			16			Bits	
Relative Accuracy			±32			±16	LSB	See Figure 4.
Differential Nonlinearity			±1			±1	LSB	Guaranteed monotonic by design. See Figure 5.
Zero Code Error		1	5		1	5	mV	All 0s loaded to DAC register. See Figure 8.
Full-Scale Error		−0.15	−1.25		−0.15	−1.25	% FSR	All 1s loaded to DAC register. See Figure 8.
Offset Error			±10			±10	mV	
Gain Error			±1.25			±1.25	% FSR	
Zero Code Error Drift[3]		±2			±2		µV/°C	
Gain Temperature Coefficient[3]		±2.5			±2.5		ppm	Of FSR/°C
DC Power Supply Rejection Ratio		-100			-100		dB	DAC code = midscale; V_{DD} = 5V/3V ±10%
OUTPUT CHARACTERISTICS[3]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Output Voltage Settling Time		8	10		8	10	µs	¼ to ¾ scale; R_L = 2 kΩ; 0 pF < C_L < 200 pF. See Figure 18.
							µs	1 LSB Settling
Slew Rate		1.5			1.5		V/µs	¼ to ¾ scale
Capacitive Load Stability		2			2		nF	R_L = ∞
		10			10		nF	R_L = 2 kΩ
Output Noise Spectral Density		80			80		nV/√Hz	DAC code = midscale,10 kHz
Output Noise (0.1 Hz to 10 Hz)		10			10		µVp-p	DAC code = midscale
THD, Total Harmonic Distortion		-80			-80		dB	V_{REF} = 2 V ± 300 mV p-p, f = 5 kHz
Digital-to-Analog Glitch Impulse		5			5		nV-s	1 LSB change around major carry. See Figure 21.
Digital Feedthrough		0.1			0.1		nV-s	
DC Output Impedance		0.5			0.5		Ω	
Short-Circuit Current[4]		30			30		mA	V_{DD} = 5 V, 3 V
Power-Up Time		4			4		µs	Coming out of power-down mode. V_{DD} = 5 V
		10			10		µs	V_{DD} = 3 V
REFERENCE INPUTS								
Reference Current		35	45		35	45	µA	V_{REF} = V_{DD} = 5 V
		20	30		20	30	µA	V_{REF} = V_{DD} = 3.6 V
Reference Input Range	0		V_{DD}	0		V_{DD}	V	
Reference Input Impedance		150			150		kΩ	
LOGIC INPUTS[3]								
Input Current			±1			±1	µA	
V_{INL}, Input Low Voltage			0.8			0.8	V	V_{DD} = 5 V, 3 V
V_{INH}, Input High Voltage	2				2		V	V_{DD} = 5 V, 3 V
Pin Capacitance		3			3		pF	

Parameter	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit	B Version[1] Conditions/Comments
POWER REQUIREMENTS								
V_{DD}	2.7		5.5	2.7		5.5	V	All digital inputs at 0 V or V_{DD}
I_{DD} (Normal Mode)								DAC active and excluding load current
V_{DD}= 4.5 V to 5.5 V		250	400		250	400	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD}= 2.7 V to 3.6 V		240	390		240	390	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
I_{DD} (All Power-Down Modes)								
V_{DD} = 4.5 V to 5.5 V		0.2	1		0.2	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		0.05	1		0.05	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
POWER EFFICIENCY								
I_{OUT}/I_{DD}		89			89		%	I_{LOAD} = 2 mA. V_{DD} = 5 V

[1] Temperature ranges are as follows: B version: −40°C to +105°C, typical at +25°C.
[2] DC specifications tested with the outputs unloaded unless otherwise stated. Linearity calculated using a reduced code range of 512 to 65024.
[3] Guaranteed by design and characterization, not production tested.
[4] Output unloaded.

TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See Figure 2. V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	Limit at T_{MIN}, T_{MAX}			
Parameter	**V_{DD} = 2.7 V to 3.6 V**	**V_{DD} = 3.6 V to 5.5 V**	**Unit**	**Conditions/Comments**
t_1[1]	50	33	ns min	SCLK cycle time
t_2	13	13	ns min	SCLK high time
t_3	13	13	ns min	SCLK low time
t_4	0	0	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	5	5	ns min	Data setup time
t_6	4.5	4.5	ns min	Data hold time
t_7	0	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	50	33	ns min	Minimum $\overline{SYNC}$ high time
t_9	13	13	ns min	$\overline{SYNC}$ rising edge to sclk fall ignore
t_{10}	0	0	ns min	SCLK falling edge to $\overline{SYNC}$ fall ignore

[1] Maximum SCLK frequency is 30 MHz at V_{DD} = 3.6 V to 5.5 V, and 20 MHz at V_{DD} = 2.7 V to 3.6 V.

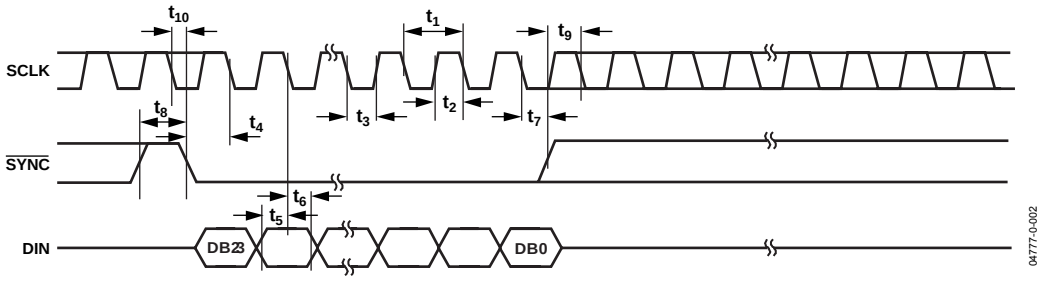

Figure 2. Serial Write Operation

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Max)	150°C
SOT-23 Package	
Power Dissipation	$(T_{J\,MAX} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	240°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

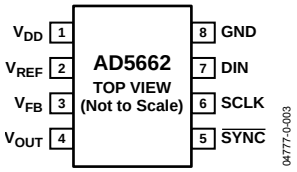

Figure 3. MSOP/SOT-23 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	V_{DD}	Power Supply Input. These parts can be operated from 2.5 V to 5.5 V. V_{DD} should be decoupled to GND.
2	V_{REF}	Reference Voltage Input.
3	V_{FB}	Feedback Connection for the Output Amplifier.
4	V_{OUT}	Analog Output Voltage from DAC. The output amplifier has rail-to-rail operation.
5	$\overline{SYNC}$	Level Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register, and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock cycle unless $\overline{SYNC}$ is taken high before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
6	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz.
7	DIN	Serial Data Input. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
8	GND	Ground Reference Point for All Circuitry on the Part.

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL versus code plot can be seen in Figure 4.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL versus code plot can be seen in Figure 5.

Zero-Code Error
Zero-code error is a measure of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5662 because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and the output amplifier. Zero-code error is expressed in mV. A plot of zero-code error versus temperature can be seen in Figure 8.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed in percent of full-scale range. A plot of full-scale error versus temperature can be seen in Figure 8.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale range.

Total Unadjusted Error
Total unadjusted error (TUE) is a measure of the output error, taking all the various errors into account. A typical TUE versus code plot can be seen in Figure 6.

Zero-Code Error Drift
This is a measure of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Error Drift
This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 21.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s, and measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

TYPICAL PERFORMANCE CHARACTERISTICS

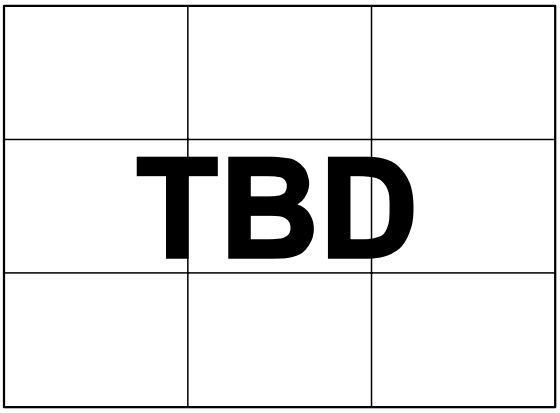

Figure 4. Typical INL Plot

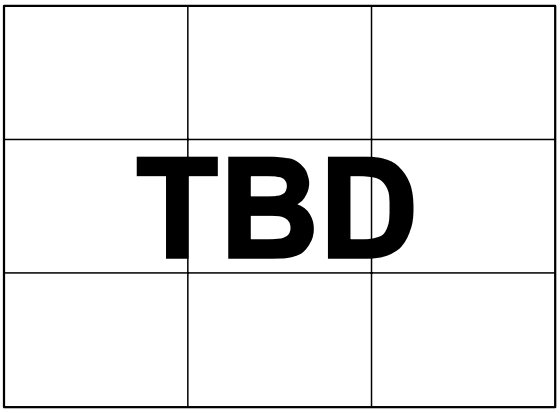

Figure 7. INL Error and DNL Error vs. Temperature

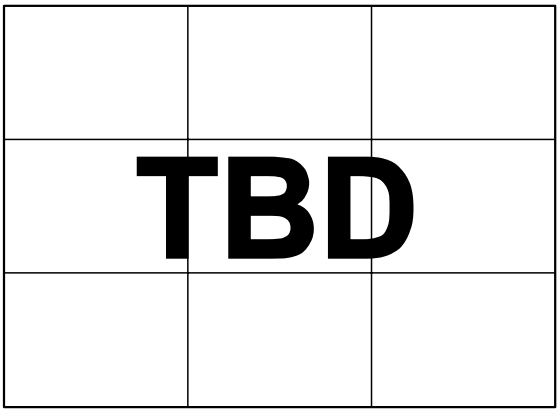

Figure 5. Typical DNL Plot

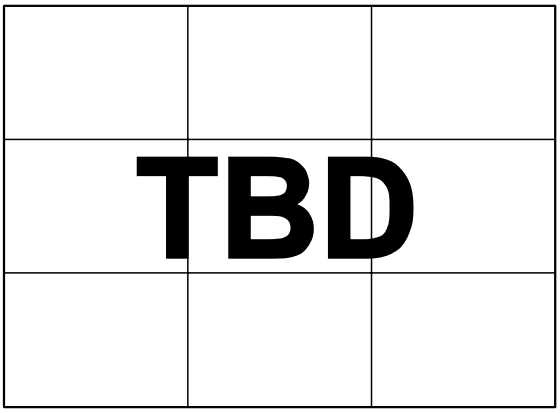

Figure 8. Zero-Scale Error and Full-Scale Error vs. Temperature

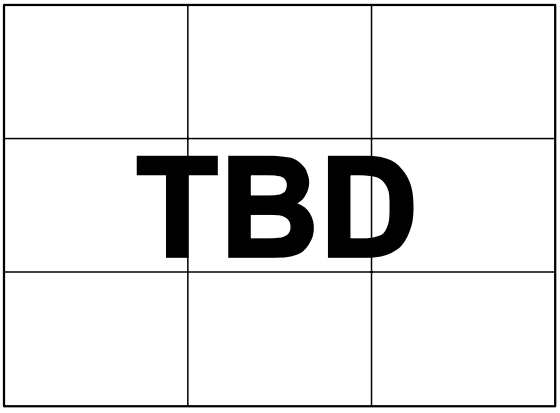

Figure 6. Typical Total Unadjusted Error Plot

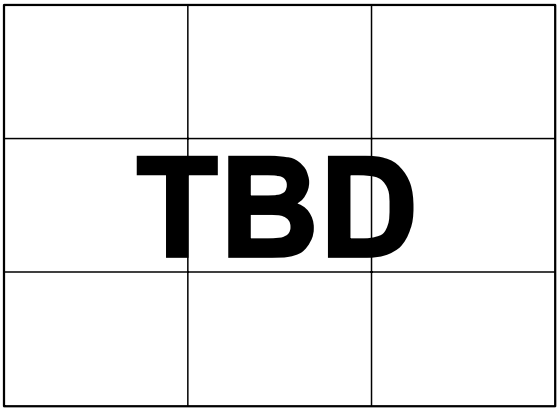

Figure 9. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V

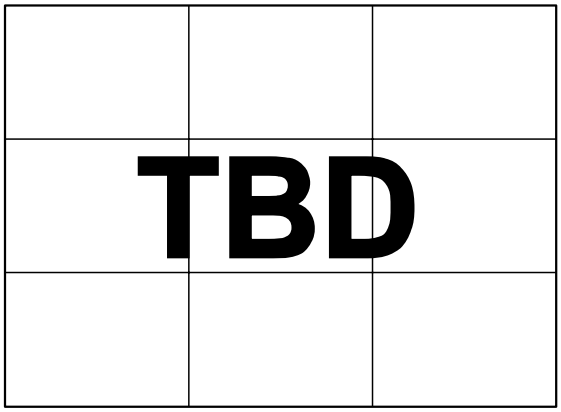

Figure 10. Source and Sink Current Capability with V_{DD} = 3 V

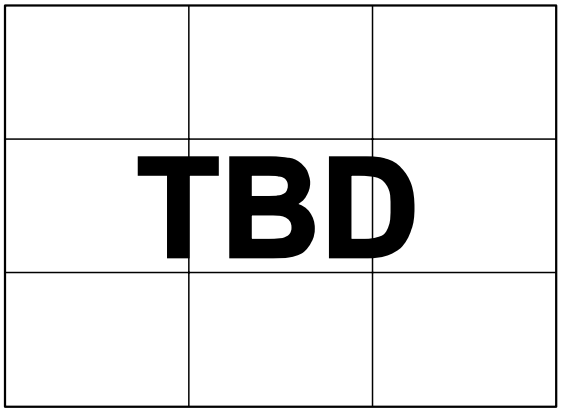

Figure 13. Supply Current vs. Temperature

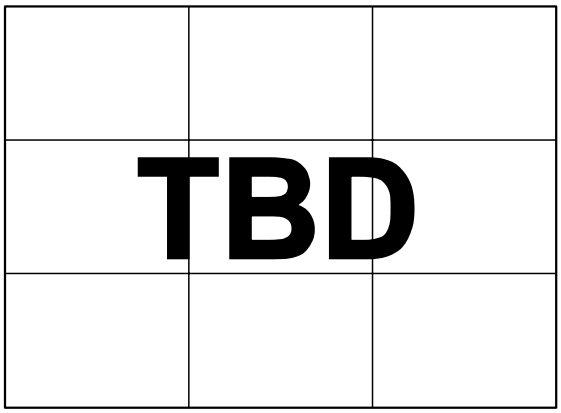

Figure 11. Source and Sink Current Capability with V_{DD} = 5 V

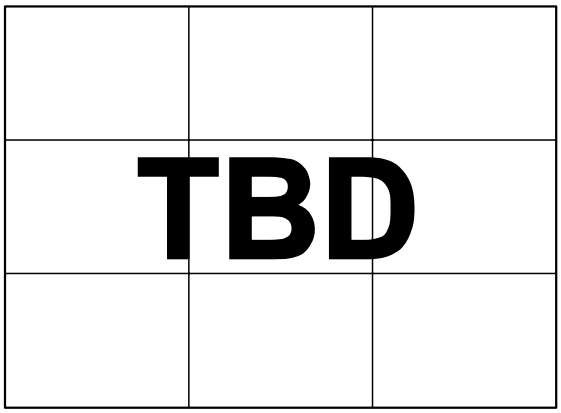

Figure 14. Supply Current vs. Supply Voltage

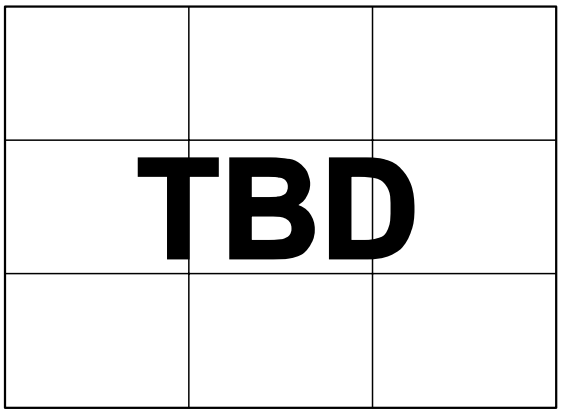

Figure 12. Supply Current vs. Code

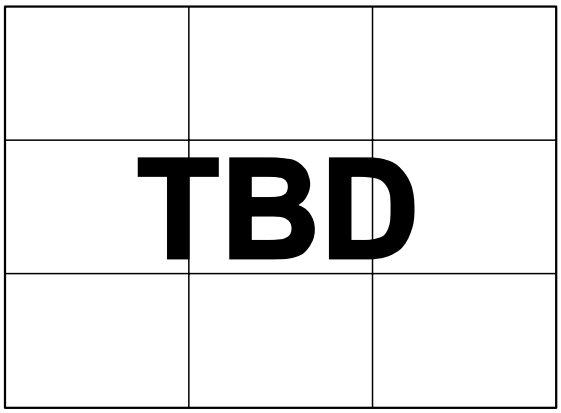

Figure 15. Power-Down Current vs. Supply Voltage

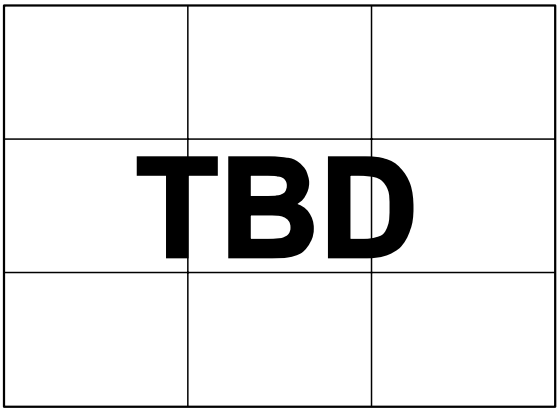

Figure 16. Supply Current vs. Logic Input Voltage

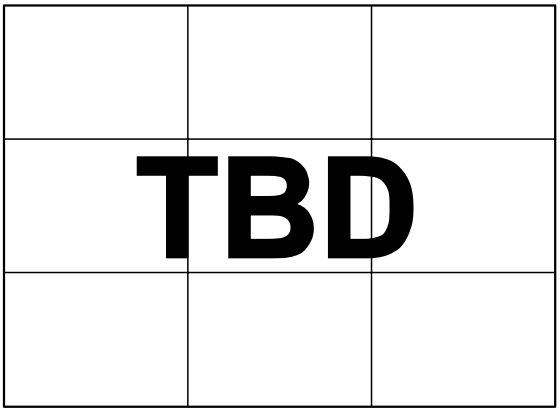

Figure 19. Power-On Reset to 0 V

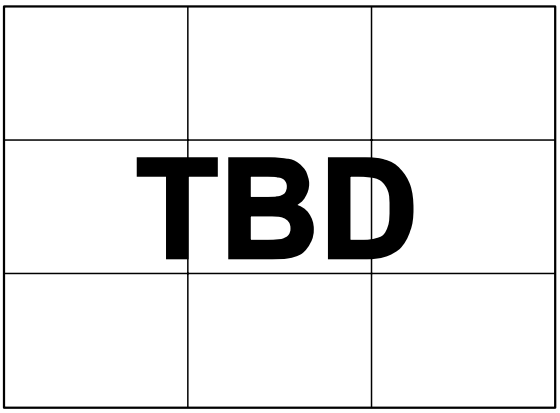

Figure 17. Full-Scale Settling Time

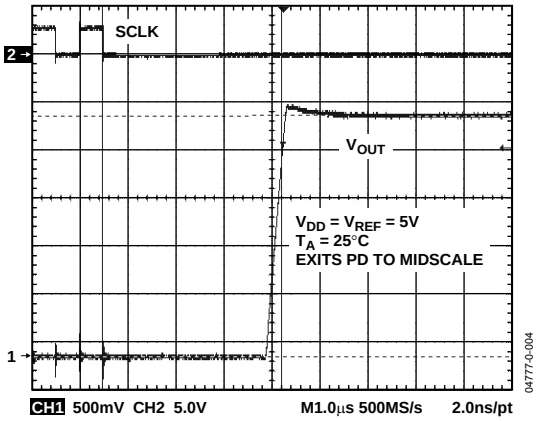

Figure 20. Exiting Power-Down to Midscale

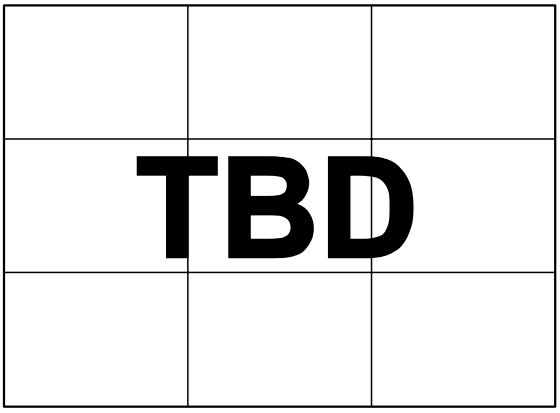

Figure 18. Half-Scale Settling Time

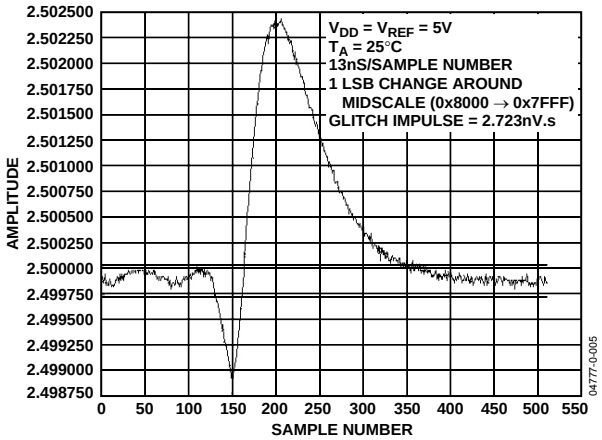

Figure 21. Digital-to-Analog Glitch Impulse (Negative)

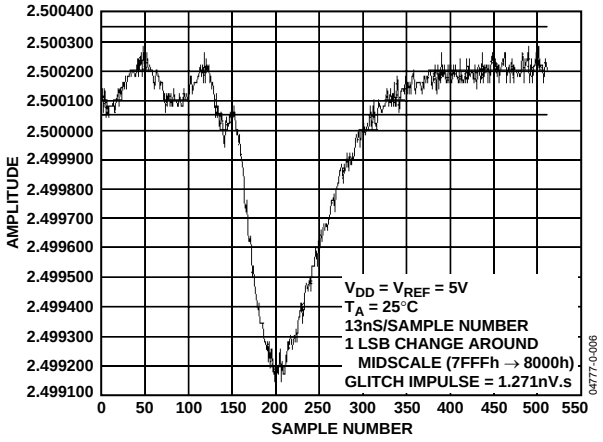

Figure 22. Digital-to-Analog Glitch Impulse (Positive)

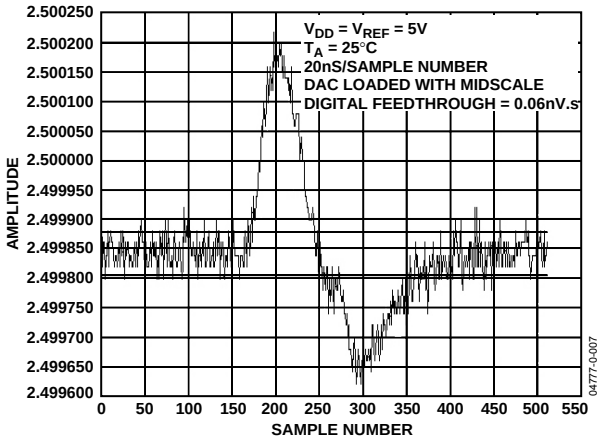

Figure 23. Digital Feedthrough

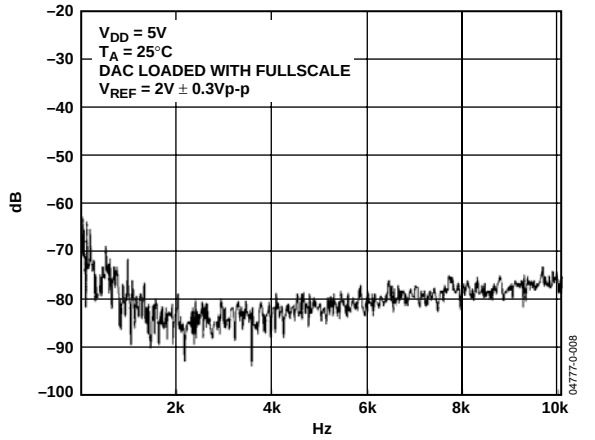

Figure 24. Total Harmonic Distortion

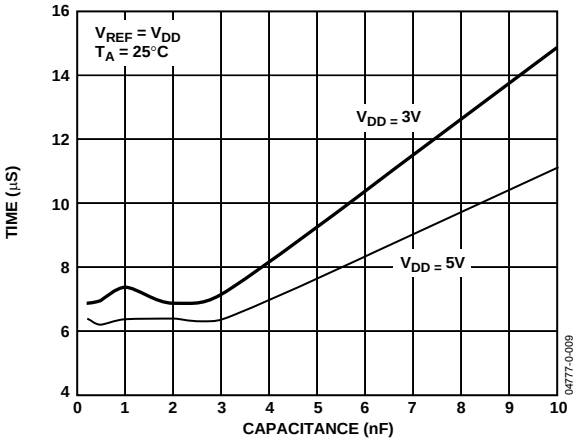

Figure 25. Settling Time vs. Capacitive Load

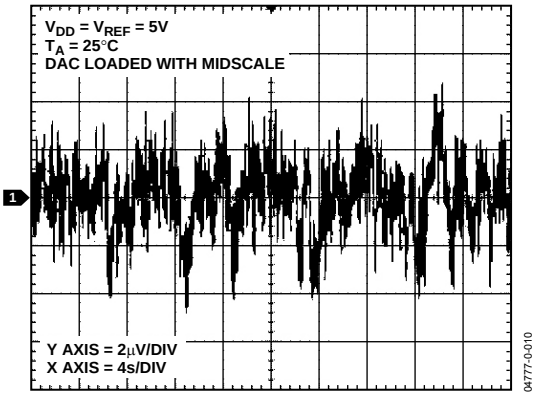

Figure 26. 0.1 Hz to 10 Hz Output Noise Plot

GENERAL DESCRIPTION

D/A SECTION

The AD5662 DAC is fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Figure 27 shows a block diagram of the DAC architecture.

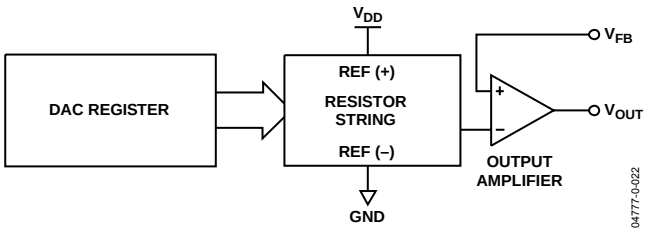

Figure 27. DAC Architecture

Since the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = VREF \times \left(\frac{D}{65{,}536} \right)$$

where *D* is the decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535.

RESISTOR STRING

The resistor string section is shown in Figure 28. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

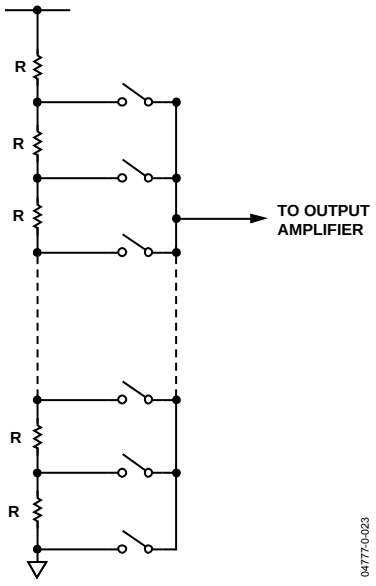

Figure 28. Resistor String

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output which gives an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 10 and Figure 11. The slew rate is 1 V/μs with a half-scale settling time of 8 μs with the output unloaded.

SERIAL INTERFACE

The AD5662 has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line is clocked into the 24-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the AD5662compatible with high speed DSPs. On the 24th falling clock edge, the last data bit is clocked in and the programmed function is executed (i.e., a change in DAC register contents and/or a change in the mode of operation). At this stage, the $\overline{\text{SYNC}}$ line may be kept low or be brought high. In either case, it must be brought high for a minimum of 33 ns before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. Since the $\overline{\text{SYNC}}$ buffer draws more current when V_{IN} = 2.4 V than it does when V_{IN} = 0.8 V, $\overline{\text{SYNC}}$ should be idled low between write sequences for even lower power operation. As is mentioned previously, however, it must be brought high again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 24 bits wide (see Figure 29). The first six bits are don't cares. The next two are control bits that control the part's mode of operation (normal mode or any one of three power-down modes). See the Power-On Reset section for a more complete description of the various modes. The next 16 bits are the data bits. These are transferred to the DAC register on the 24th falling edge of SCLK.

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 24 falling edges of SCLK, and the DAC is updated on the 24th falling edge. However if $\overline{\text{SYNC}}$ is brought high before the 24th falling edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs—see Figure 30.

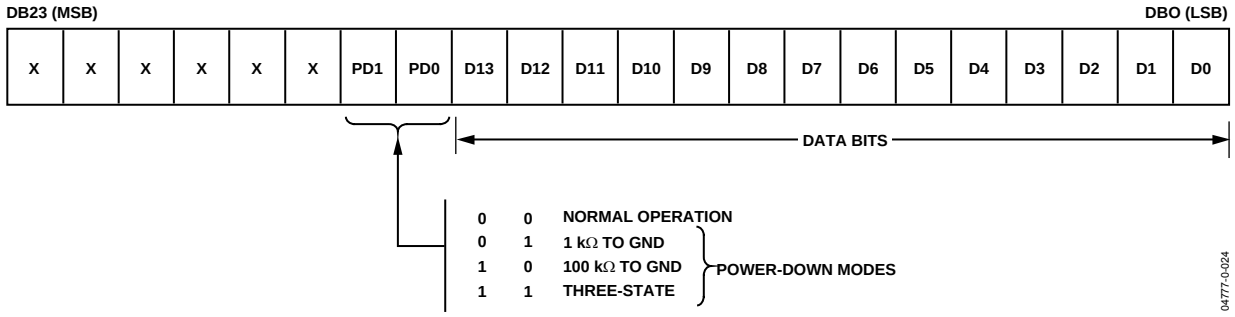

Figure 29. Input Register Contents

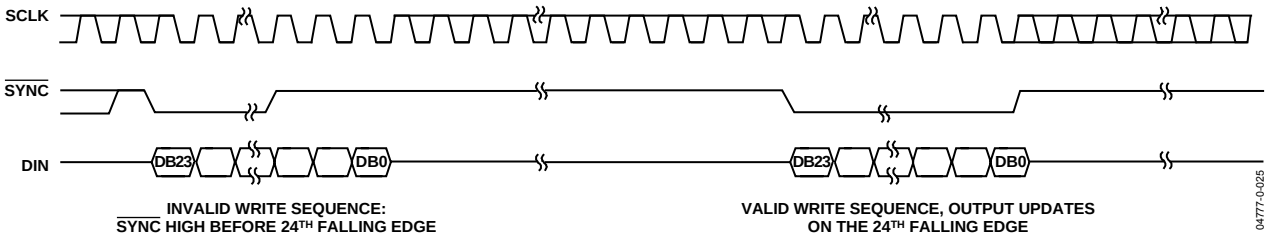

Figure 30. $\overline{SYNC}$ Interrupt Facility

POWER-ON RESET

The AD5662 family contains a power-on-reset circuit that controls the output voltage during power-up. The AD5662x-1 DAC output powers up to 0 V, and the AD5662x-2 DAC output powers up to midscale. The output remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

POWER-DOWN MODES

The AD5662 contains four separate modes of operation. These modes are software-programmable by setting two bits (DB17 and DB16) in the control register. Table 5 shows how the state of the bits corresponds to the device's mode of operation.

Table 5. Modes of Operation for the AD5662

DB17	DB16	Operating Mode
0	0	Normal Operation
		Power-Down Modes
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-State

When both bits are set to 0, the part works normally with its normal power consumption of 250 μA at 5 V. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through a 1 kΩ or 100 kΩ resistor, or is left open-circuited (three-state). The output stage is illustrated in Figure 31.

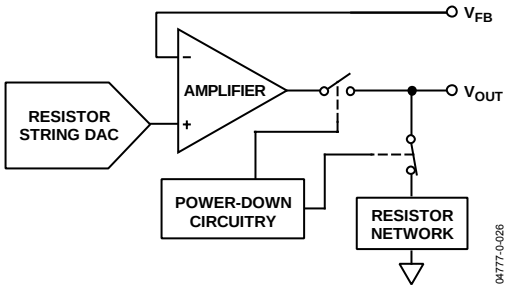

Figure 31. Output Stage during Power-Down

The bias generator, the output amplifier, the resistor string, and other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 μs for V_{DD} = 5 V and 5 μs for V_{DD} = 3 V. See Figure 20 for a plot.

MICROPROCESSOR INTERFACING

AD5662 to ADSP-2101/ADSP-2103 Interface

Figure 32 shows a serial interface between the AD5662 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in SPORT transmit alternate framing mode. The ADSP-2101/ADSP-2103 SPORT is programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, 24-bit word length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled.

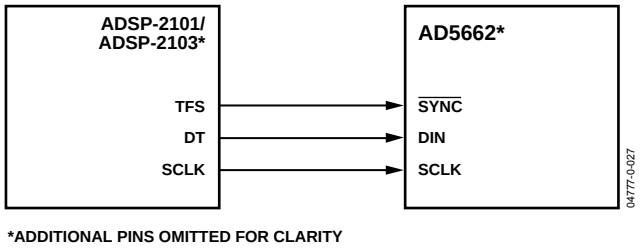

Figure 32. AD5662 to ADSP-2101/ADSP-2103 Interface

AD5662 to 68HC11/68L11 Interface

Figure 33 shows a serial interface between the AD5662 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5662, while the MOSI output drives the serial data line of the DAC.

The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: the 68HC11/68L11 should be configured with its CPOL bit as a 0 and its CPHA bit as a 1. When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). When the 68HC11/68L11 is configured as described above, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data to the AD5662, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC; PC7 is taken high at the end of this procedure.

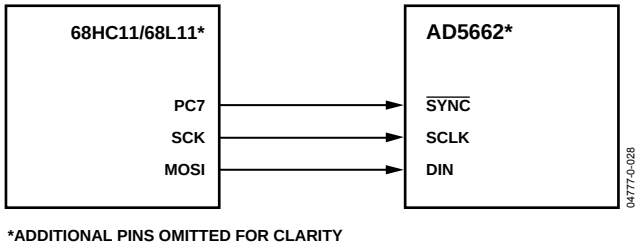

Figure 33. AD5662 to 68HC11/68L11 Interface

AD5662 to 80C51/80L51 Interface

Figure 34 shows a serial interface between the AD5662 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TXD of the 80C51/80L51 drives SCLK of the AD5662, while RXD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is again derived from a bit programmable pin on the port. In this case, port line P3.3 is used. When data is to be transmitted to the AD5662, P3.3 is taken low. The 80C51/80L51 transmits data only in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in a format that has the LSB first. The AD5662 requires its data with the MSB as the first bit received. The 80C51/80L51 transmit routine should take this into account.

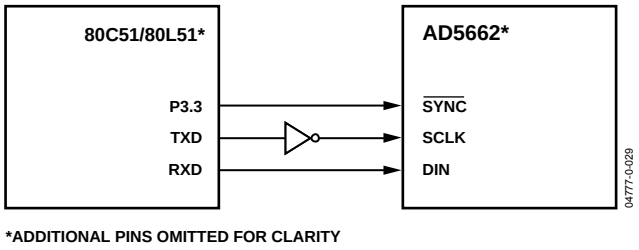

Figure 34. AD5662 to 80C51/80L51 Interface

AD5662 to MICROWIRE Interface

Figure 35 shows an interface between the AD5320 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5320 on the rising edge of the SK.

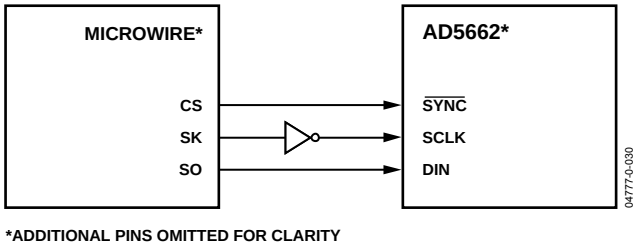

Figure 35. AD5662 to MICROWIRE Interface

APPLICATIONS

USING REF19x AS A POWER SUPPLY FOR AD5662

Because the supply current required by the AD5662 is extremely low, an alternative option is to use a REF19x voltage reference (REF195 for 5 V, REF193 for 3 V) to supply the required voltage to the part—see Figure 36. This is especially useful if the power supply is quite noisy, or if the system supply voltages are at some value other than 5 V or 3 V, for example, 15 V. The REF19x outputs a steady supply voltage for the AD5662. If the low dropout REF195 is used, it must supply 250 µA of current to the AD5662. This is with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is

250 µA + (5 V/5 kΩ) = 1.25 mA

The load regulation of the REF195 is typically 2 ppm/mA, which results in a 2.5 ppm (12.5 µV) error for the 1.25 mA current drawn from it. This corresponds to a 0.164 LSB error.

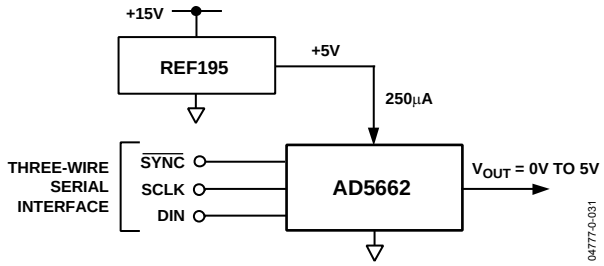

Figure 36. REF195 as Power Supply to AD5662

BIPOLAR OPERATION USING THE AD5662

The AD5662 has been designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 37. The circuit below gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{65{,}536} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 to 65535). With V_{DD} = 5 V, $R1 = R2$ = 10 kΩ,

$$V_O = \left(\frac{10 \times D}{65{,}536} \right) - 5\text{V}$$

This is an output voltage range of ±5 V, with 0x0000 corresponding to a −5 V output and 0xFFFF corresponding to a 5 V output.

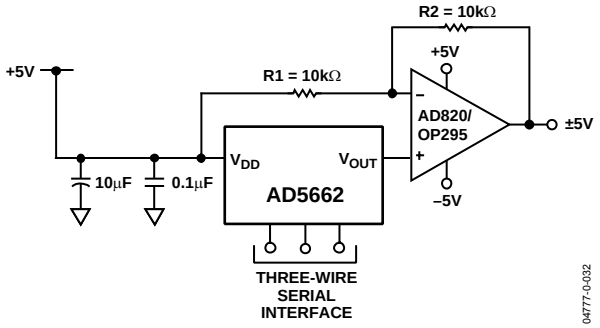

Figure 37. Bipolar Operation with the AD5662

USING AD5662 WITH A GALVANICALLY ISOLATED INTERFACE

In process-control applications in industrial environments, it is often necessary to use a galvanically isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur in the area where the DAC is functioning. Isocouplers provide isolation in excess of 3 kV. The AD5662 uses a 3-wire serial logic interface so the ADuM130x 3-channel digital isolator provides the required isolation (see Figure 38). The power supply to the part also needs to be isolated. This is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5662.

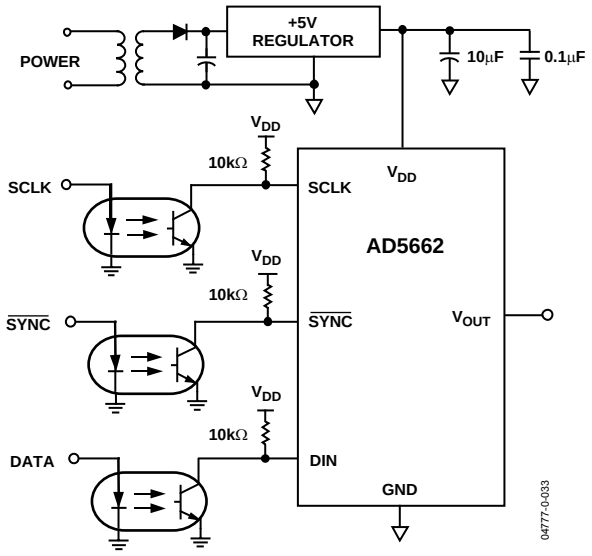

Figure 38. AD5662 with an Opto-Isolated Interface

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5662 should have separate analog and digital sections, each having its own area of the board. If the AD5662 is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5662.

The power supply to the AD5662 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should be located as close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has low effective series resistance (ESR) and effective series inductance (ESI), for example, common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

OUTLINE DIMENSIONS

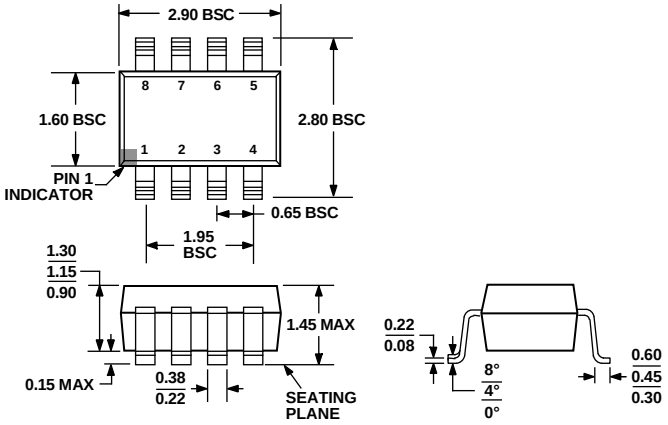

Figure 39. 8-Lead SOT-23
(RJ-8)
Dimensions shown in millimeters

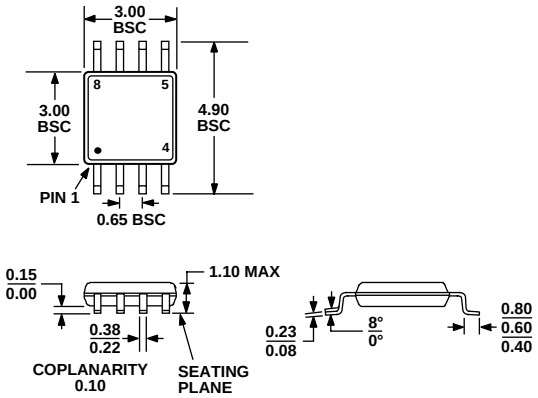

Figure 40. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Grade	Power-On Reset to Code	Branding	Package Options[1]	Description	Temperature Range
AD5662ARJ-1	A	Zero	D38	RJ-8	±32 LSB INL	−40°C to +125°C
AD5662ARJ-2	A	Midscale	D39	RJ-8	±32 LSB INL	−40°C to +125°C
AD5662ARM	A	Zero	D38	RM-8	±32 LSB INL	−40°C to +125°C
AD5662BRJ-1	B	Zero	D36	RJ-8	±16 LSB INL	−40°C to +125°C
AD5662BRJ-2	B	Midscale	D37	RJ-8	±16 LSB INL	−40°C to +125°C
AD5662BRM	B	Zero	D36	RM-8	±16 LSB INL	−40°C to +125°C

[1]RJ = SOT-23, RM = MSOP

NOTES

NOTES

PR04777–0–10/04(PrA)