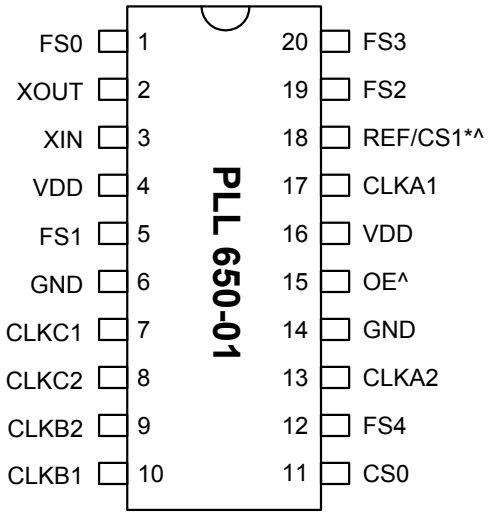
PLL650-01

Low EMI Network LAN Clock

FEATURES

- Full CMOS output swing with 25 mA output drive capability at TTL levels.
- Advanced, low power, sub-micron CMOS process.
- 25.0MHz fundamental crystal or reference clock signal.
- Six output clocks with selectable frequencies.
- SDRAM frequencies of 67,83,100, and 133MHz.
- Spread Spectrum Technology selectable for EMI Reduction from ±0.25% to ±0.5% center.
- Buffered crystal reference output.
- Ideal for Network switches.
- 3.3V operation.
- Available in 150mil 20-Pin SSOP.

PIN CONFIGURATION

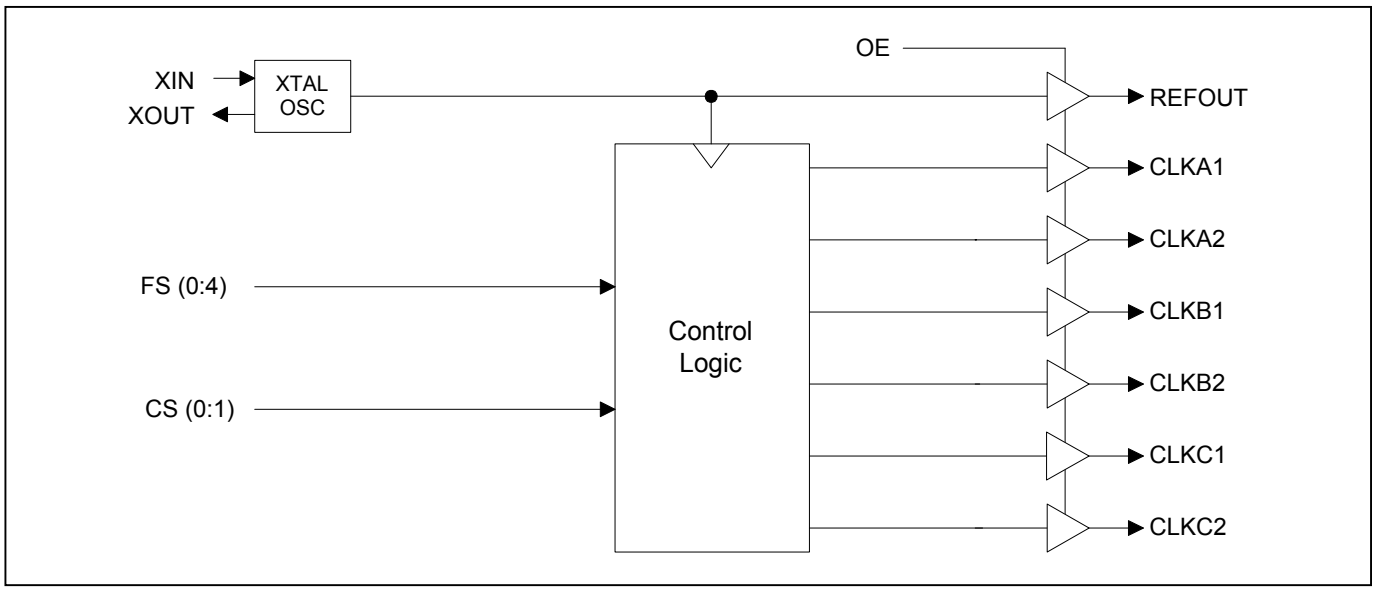


DESCRIPTION

The PLL650-01 is a low cost, low jitter, high performance clock synthesizer. With PhaseLink's proprietary analog Phase Locked Loop techniques, the chip accepts 25.0MHz from a crystal or a reference clock, and produces multiple outputs clocks for network chips, PCI devices, SDRAM, and ASICs.

Note: ^: 100kΩ internal pull-up. *: Bi-directional pin. The value of CS1 is latched upon power-up. When no external pull-down resistor is connected to the pin, the internal pull-up results in a default high value for CS1. An external 10kΩ pull-down resistor is recommended to set CS1 to low.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Number	Type	Description
CLKA1	17	O	Clock A Output. Frequency Select pin selectable via (FS0 ~ FS4).
CLKA2	13	O	Clock A Output. Frequency Select pin selectable via (FS0 ~ FS4).
CLKB1	10	O	Clock B Output. Frequency Select pin selectable via (FS0 ~ FS4).
CLKB2	9	O	Clock B Output. Frequency Select pin selectable via (FS0 ~ FS4).
CLKC1	7	O	Clock C Output. Selectable from jumper CS0 and table CS1 output.
CLKC2	8	O	Clock C Output. Selectable from jumper CS0 and table CS1 output.
XIN	3	I	Crystal input to be connected to a fundamental crystal or clock input.
XOUT	2	O	Crystal Connection.
FS2	19	I	Frequency Select 2. Select outputs per table on page 3.
FS3	20	I	Frequency Select 3. Select outputs per table on page 3.
CS0	11	I	Clock C select pin. Select outputs for CLKC1, CLKC2.
FS0	1	I	Frequency Select 0. Select outputs per table on page 3.
FS1	5	I	Frequency Select 1. Select outputs per table on page 3.
FS4	12	I	Frequency Select 4. Select outputs per table on page 3.
OE	15	I	Output Enable. When low, Tri-states all outputs.
REF/CS1	18	B	Buffered Reference Clock Outputs. Same frequency as crystal or clock input. This pin latches CS1 value at power up and select outputs for CLKC1, CLKC2 (See table on page 3). Has internal pull-up resistor.
VDD	4,16	P	3.3V power supply.
GND	6,14	P	Ground.

FREQUENCY (MHz) SELECTION TABLE (For a 25MHz Crystal or Clock Input)

FS0	FS1	FS2	FS3	FS4	CLKA1	CLKA2	CLKB1	CLKB2	SST*
0	0	0	0	0	100.0	OFF	66.667	33.333	OFF
0	0	0	0	1	100.0	OFF	100.0	50.0	OFF
0	0	0	1	0	100.0	OFF	83.333	41.667	OFF
0	0	0	1	1	100.0	OFF	133.333	66.667	OFF
0	0	1	0	0	75.0	OFF	66.667	33.333	OFF
0	0	1	0	1	75.0	OFF	100.0	50.0	OFF
0	0	1	1	0	75.0	OFF	83.333	41.667	OFF
0	0	1	1	1	66.667	OFF	133.333	66.667	OFF
0	1	0	0	0	33.333	16.667	66.667	33.333	OFF
0	1	0	0	1	33.333	16.667	100.0	50.0	OFF
0	1	0	1	0	33.333	16.667	83.333	41.667	OFF
0	1	0	1	1	33.333	16.667	133.333	66.667	OFF
0	1	1	0	0	66.667	33.333	66.667	33.333	OFF
0	1	1	0	1	66.667	33.333	100.0	50.0	OFF
0	1	1	1	0	66.667	33.333	83.333	41.667	OFF
0	1	1	1	1	66.667	33.333	133.333	66.667	OFF
1	0	0	0	0	100.0	OFF	OFF	OFF	±0.25%
1	0	0	0	1	100.0	OFF	OFF	OFF	±0.5%
1	0	0	1	0	133.333	OFF	OFF	OFF	±0.25%
1	0	0	1	1	133.333	OFF	OFF	OFF	±0.5%
1	0	1	0	0	133.333	OFF	66.667	33.333	±0.25%
1	0	1	0	1	133.333	OFF	66.667	33.333	±0.5%
1	0	1	1	0	133.333	OFF	66.667	33.333	OFF
1	0	1	1	1	100.0	OFF	100.0	50.0	±0.25%
1	1	0	0	0	100.0	OFF	100.0	OFF	OFF
1	1	0	0	1	125.0	OFF	OFF	OFF	±0.25%
1	1	0	1	0	83.333	OFF	83.333	OFF	±0.5%
1	1	0	1	1	125.0	OFF	OFF	OFF	OFF
1	1	1	0	0	Test	Test	Test	Test	Test
1	1	1	0	1	100.0	OFF	100.0	OFF	±0.25%
1	1	1	1	0	125.0	OFF	OFF	OFF	±0.5%
1	1	1	1	1	133.333	OFF	133.333	OFF	±0.25%

Note: SST = Spread Spectrum Technology for EMI Reduction

CS1	CS0	CLKC1	CLKC2
0	0	125.0	125.0
0	1	75.0	75.0
1	0	125.0	50.0
1	1	100.0	OFF

FUNCTIONAL DESCRIPTION

Selectable spread spectrum and output frequencies

The PLL650-01 provides selectable spread spectrum modulation and selectable output frequencies, as well as an "output enable" selection input (pin 15). Selection is made by connecting specific pins to a logical "zero" or "one", according to the frequency selection tables shown on page 3.

In order to reduce the number of pins on the chip, the PLL650-01 uses pin 18 (REF/CS1) as a bi-directional pin that serves as input (CS1) upon power-up, and as output (REF) as soon as the input has been latched.

Pins 1 (FS0), 5 (FS1), 19 (FS2), 20 (FS3), and 12 (FS4) are used as inputs to select the CLKA1, CLKA2, CLKB1, CLKB2 output frequencies and spread spectrum (SST) modulations (as detailed in the frequency selection table on page 3). Pins 11 (CS0) and 18 (REF/CS1) are used to select the CLKC1 and CLKC2 frequency outputs. As said above, pin 18 is a bi-directional pin.
Pin 15 (OE) is the output enable selection input that tri-states (disables) all outputs when selected to "low" (logical "zero").

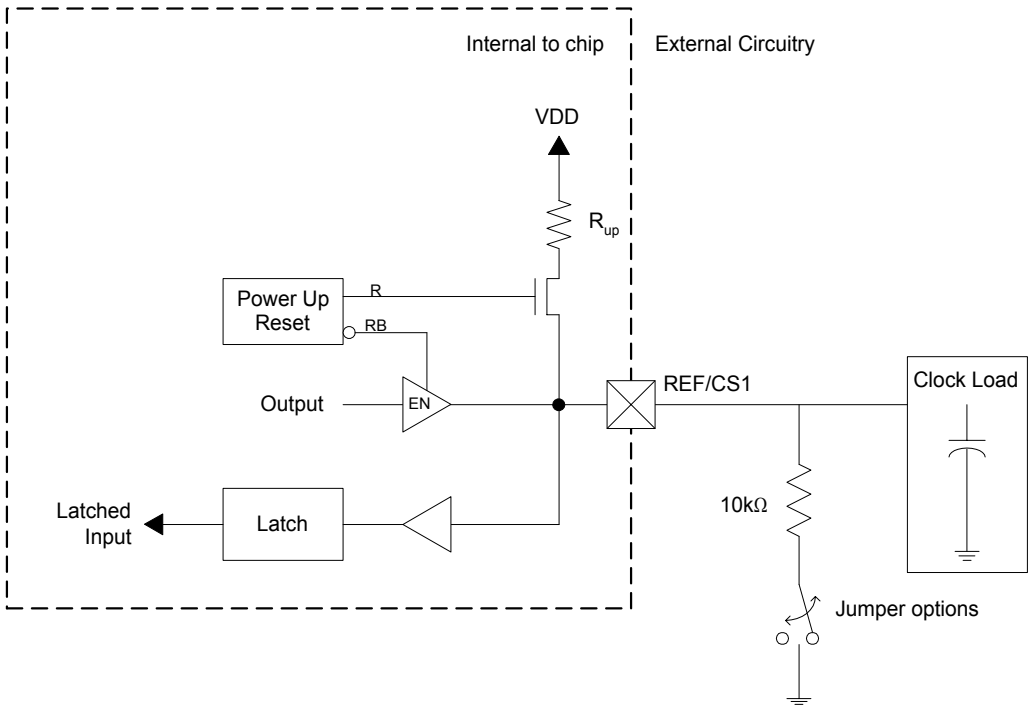
Connecting a selection pin to a logical "one"

In order to connect pins 1 (FS0), 5 (FS1), 19 (FS2), 20 (FS3), and 12 (FS4) to "high" (logical "one), the pins simply need to be connected to VDD. Pins 15 and 18 have an internal pull-up resistor of 100kΩ. This internal pull-up resistor will pull the input value to a logical "one" (pull-up) by default, i.e. when no resistive load is connected between the pin and GND. For pins 15 and 18, no external pull-up resistor is therefore required for connecting a logical "one" upon. ***Note:*** *since pin18 also is used as an output, it may happen that the output load present a low impedance in comparison to the internal pull-up resistor. In this case, the internal pull-up resistor may not be sufficient to pull the input up to a logical "one", and an external pull-up resistor may be required.*

Connecting a selection pin to a logical "zero"

Except for pin 18 (REF/CS1) that is bi-directional, all other input pins are input only. In order to connect them to a logical "zero", the pins simply need to be grounded. Connecting pin 18 to a logical "zero" will however require the use of an external loading resistor between the pin and GND that has to be sufficiently small (compared to the internal pull-up resistor) so that the pin voltage be pulled below 0.8V (logical "zero"). In order to avoid loading effects when the pin serves as output, the value of the external pull-down resistor should however be kept as large as possible. In general, it is recommended to use an external resistor of around 10kΩ (see Application Diagram). ***Note:*** *when the output is used to drive a load presenting an small resistance between the output pin and VDD, this resistance is in essence connected in parallel to the internal pull-up resistor. In such a case, the external pull-down resistor may have to be dimensioned smaller to guarantee that the pin voltage will be low enough to achieve the desired logical "zero". This is particularly true when driving 74FXX TTL components.*

APPLICATION DIAGRAM FOR SETTING CS1 (PIN 18)



NOTE: Rup=100kΩ . R starts from 1 to 0 while RB starts from 0 to 1.

Electrical Specifications

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. AC Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency		10	12.5 or 25	27	MHz
Output Rise Time	0.8V to 2.0V with no load			1.5	ns
Output Fall Time	2.0V to 0.8V with no load			1.5	ns
Duty Cycle	At VDD/2	45	50	60	%
Max. Absolute Jitter	Short term		±150		ps
Max. Jitter, cycle to cycle				80	ps

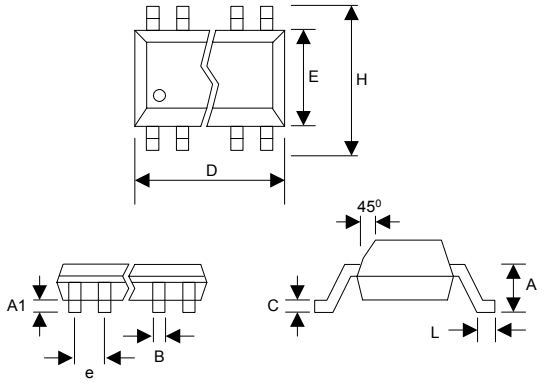
3. DC Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	V_{DD}		2.97		3.63	V
Input High Voltage	V_{IH}			V_{DD} /2		V
Input Low Voltage	V_{IL}			V_{DD} /2	V_{DD} /2 - 1	V
Input High Voltage	V_{IH}	For all Tri-level input	V_{DD} -0.5			V
Input Low Voltage	V_{IL}	For all Tri-level input			0.5	V
Input High Voltage	V_{IH}	For all normal input	2			V
Input Low Voltage	V_{IL}	For all normal input			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -25mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25mA			0.4	V
Output High Voltage At CMOS Level	V_{OH}	I_{OH} = -8mA	V_{DD} -0.4			V
Operating Supply Current	I_{DD}	No Load		35		mA
Short-circuit Current	I_S			±50		mA
Internal pull-up resistor	R_{up}	OE, CS1		100		kΩ

PACKAGE INFORMATION

20 PIN Narrow SSOP (inches)

	SSOP	
Symbol	Min.	Max.
A	0.053	0.069
A1	0.004	0.010
B	0.008	0.012
C	0.007	0.010
D	0.337	0.344
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
e	0.025 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL650-01 X C

PART NUMBER

TEMPERATURE
C=COMMERCIAL
I=INDUSTRAL

PACKAGE TYPE
X=SSOP

Order Number	Marking	Package Option
PLL650-01XC-R	P650-01XC	SSOP - Tape and Reel
PLL650-01XC	P650-01XC	SSOP - Tube