LTC1860/LTC1861

µPower, 12-Bit, 250ksps 1- and 2-Channel ADCs in MSOP

FEATURES

- **12-Bit 250ksps ADCs in MSOP Package**
- Single 5V Supply
- Low Supply Current: 850µA (Typ)
- Auto Shutdown Reduces Supply Current to 2µA at 1ksps
- True Differential Inputs
- 1-Channel (LTC1860) or 2-Channel (LTC1861) Versions
- SPI/MICROWIRE™ Compatible Serial I/O
- High Speed Upgrade to LTC1286/LTC1298
- Pin Compatible with 16-Bit LTC1864/LTC1865

APPLICATIONS

- High Speed Data Acquisition
- Portable or Compact Instrumentation
- Low Power Battery-Operated Instrumentation
- Isolated and/or Remote Data Acquisition

DESCRIPTION

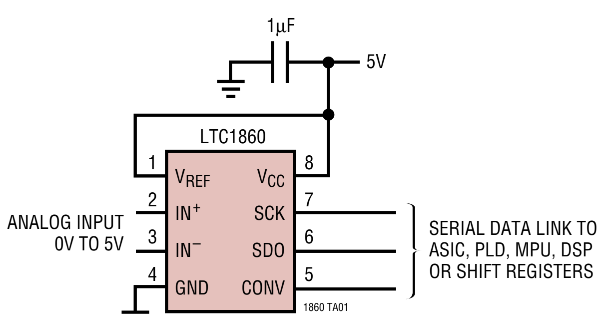
The LTC®1860/LTC1861 are 12-bit A/D converters that are offered in MSOP and SO-8 packages and operate on a single 5V supply. At 250ksps, the supply current is only 850µA. The supply current drops at lower speeds because the LTC1860/LTC1861 automatically power down to a typical supply current of 1nA between conversions. These 12-bit switched capacitor successive approximation ADCs include sample-and-holds. The LTC1860 has a differential analog input with an adjustable reference pin. The LTC1861 offers a software-selectable 2-channel MUX and an adjustable reference pin on the MSOP version.

The 3-wire, serial I/O, MSOP or SO-8 package and extremely high sample rate-to-power ratio make these ADCs ideal choices for compact, low power, high speed systems.

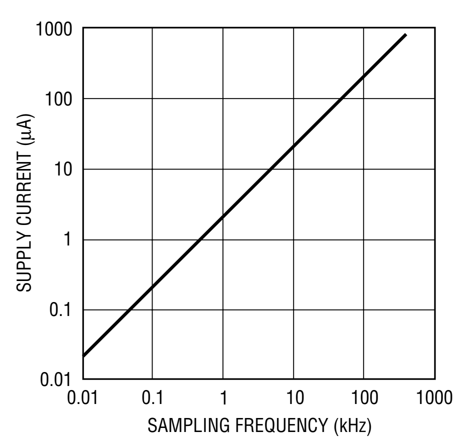
These ADCs can be used in ratiometric applications or with external references. The high impedance analog inputs and the ability to operate with reduced spans down to 1V full scale, allow direct connection to signal sources in many applications, eliminating the need for external gain stages.

TYPICAL APPLICATION

Single 5V Supply, 250ksps, 12-Bit Sampling ADC



Supply Current vs Sampling Frequency

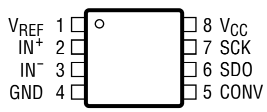


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{CC}) 7V
Ground Voltage Difference
AGND, DGND LTC1861 MSOP Package .... ±0.3V
Analog Input .... (GND – 0.3V) to (V_{CC} + 0.3V)
Digital Input .... (GND – 0.3V) to 7V
Digital Output .... (GND – 0.3V) to (V_{CC} + 0.3V)
Power Dissipation 400mW
Operating Temperature Range
LTC1860C/LTC1861C .... 0°C to 70°C
LTC1860I/LTC1861I .... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

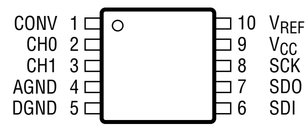


MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 210°C/W

ORDER PART NUMBER
LTC1860CMS8 LTC1860IMS8
MS8 PART MARKING
LTWR LTWS

TOP VIEW

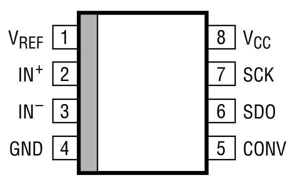


MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 210°C/W

ORDER PART NUMBER
LTC1861CMS LTC1861IMS
MS PART MARKING
LTWT LTWU

TOP VIEW

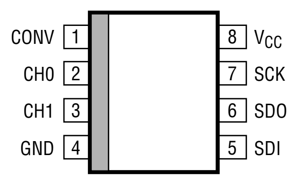


S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER PART NUMBER
LTC1860CS8 LTC1860IS8
S8 PART MARKING
1860 1860I

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER PART NUMBER
LTC1861CS8 LTC1861IS8
S8 PART MARKING
1861 1861I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, f_{SCK} = $f_{SCK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution		●	12			Bits
No Missing Codes Resolution		●	12			Bits
INL	(Note 3)	●			±1	LSB
Transition Noise				0.07		LSB_{RMS}
Gain Error		●			±20	mV
Offset Error	LTC1860 SO-8 and MSOP, LTC1861 MSOP LTC1861 SO-8	● ●		±2 ±3	±5 ±7	mV mV
Input Differential Voltage Range	$V_{IN} = IN^+ – IN^–$	●	0		V_{REF}	V
Absolute Input Range	IN^+ Input $IN^–$ Input		–0.05 –0.05		V_{CC} + 0.05 $V_{CC}/2$	V V
V_{REF} Input Range	LTC1860 SO-8 and MSOP, LTC1861 MSOP		1		V_{CC}	V
Analog Input Leakage Current	(Note 4)	●			±1	µA
C_{IN} Input Capacitance	In Sample Mode During Conversion			12 5		pF pF

DYNAMIC ACCURACY

T_A = 25°C. V_{CC} = 5V, f_{SAMPLE} = 250kHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio			72		dB
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal		71		dB
THD	Total Hamonic Distortion Up to 5th Harmonic	100kHz Input Signal		77		dB
	Full Power Bandwidth			20		MHz
	Full Linear Bandwidth	S/(N + D) ≥ 68dB		125		kHz

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	μA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			−2.5	μA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = 10μA V_{CC} = 4.75V, I_O = 360μA	● ●	4.5 2.4	4.74 4.72		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	CONV = V_{CC}	●			±3	μA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−25		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			20		mA
I_{REF}	Reference Current (LTC1860 SO-8, MSOP and LTC1861 MSOP)	CONV = V_{CC} $f_{SMPL} = f_{SMPL(MAX)}$	● ●		0.001 0.05	3 0.1	μA mA
I_{CC}	Supply Current	CONV = V_{CC} After Conversion $f_{SMPL} = f_{SMPL(MAX)}$	● ●		0.001 0.85	3 1.3	μA mA
P_D	Power Dissipation	$f_{SMPL} = f_{SMPL(MAX)}$			4.25		mW

RECOMMENDED OPERATING CONDITIONS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage			4.75		5.25	V
f_{SCK}	Clock Frequency		●	DC		20	MHz
t_{CYC}	Total Cycle Time			12 • SCK + t_{CONV}			μs
t_{SMPL}	Analog Input Sampling Time	LTC1860 LTC1861		12 10			SCK SCK
t_{suCONV}	Setup Time CONV↓ Before First SCK↑, (See Figure 1)			30			ns
t_{hDI}	Holdtime SDI After SCK↑	LTC1861		15			ns
t_{suDI}	Setup Time SDI Stable Before SCK↑	LTC1861		15			ns
t_{WHCLK}	SCK High Time	$f_{SCK} = f_{SCK(MAX)}$		40%			$1/f_{SCK}$
t_{WLCLK}	SCK Low Time	$f_{SCK} = f_{SCK(MAX)}$		40%			$1/f_{SCK}$
t_{WHCONV}	CONV High Time Between Data Transfer Cycles			t_{CONV}			μs
t_{WLCONV}	CONV Low Time During Data Transfer			12			SCK
t_{hCONV}	Hold Time CONV Low After Last SCK↑			13			ns

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, f_{SCK} = $f_{SCK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time (See Figure 1)		●		2.75	3.2	µs
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●	250			kHz
t_{dDO}	Delay Time, SCK↓ to SDO Data Valid	C_{LOAD} = 20pF	 ●		15	20 25	ns ns
t_{dis}	Delay Time, CONV↑ to SDO Hi-Z		●		30	60	ns
t_{en}	Delay Time, CONV↓ to SDO Enabled	C_{LOAD} = 20pF	●		30	60	ns
t_{hDO}	Time Output Data Remains Valid After SCK↓	C_{LOAD} = 20pF	●	5	10		ns
t_r	SDO Rise Time	C_{LOAD} = 20pF			8		ns
t_f	SDO Fall Time	C_{LOAD} = 20pF			4		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

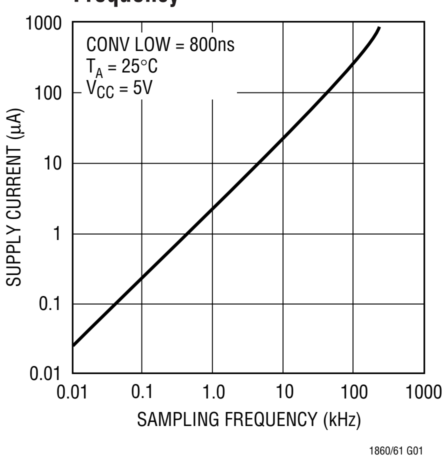
Note 2: All voltage values are with respect to GND.

Note 3: Integral nonlinearity is defined as deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

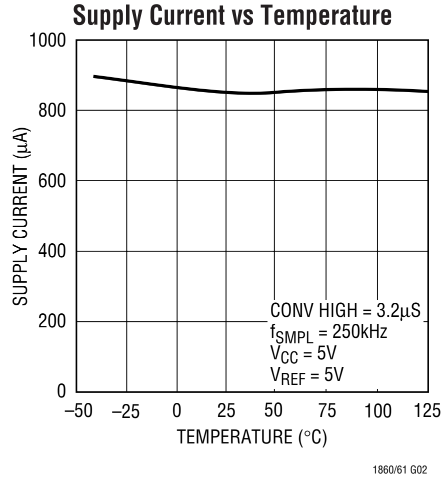
Note 4: Channel leakage current is measured while the part is in sample mode.

TYPICAL PERFORMANCE CHARACTERISTICS

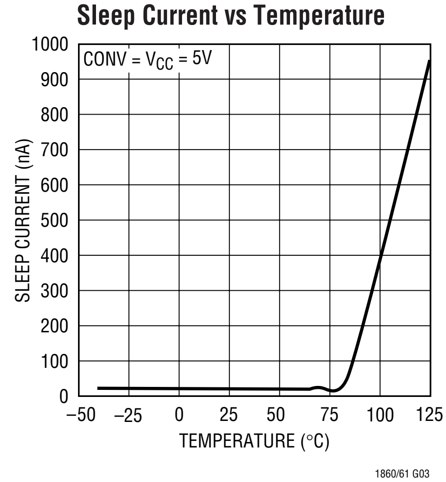
Supply Current vs Sampling Frequency



Supply Current vs Temperature

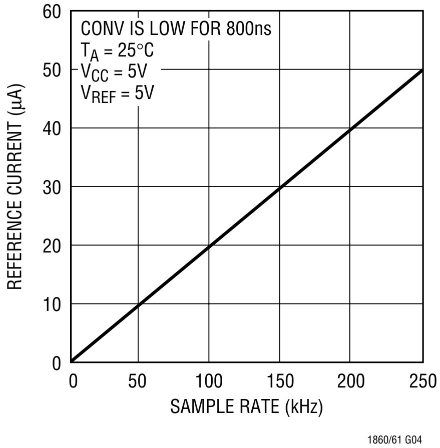


Sleep Current vs Temperature

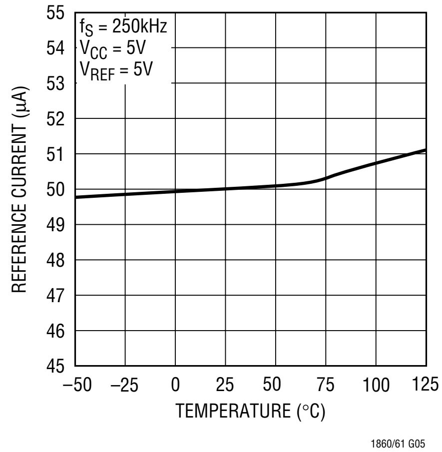


TYPICAL PERFORMANCE CHARACTERISTICS

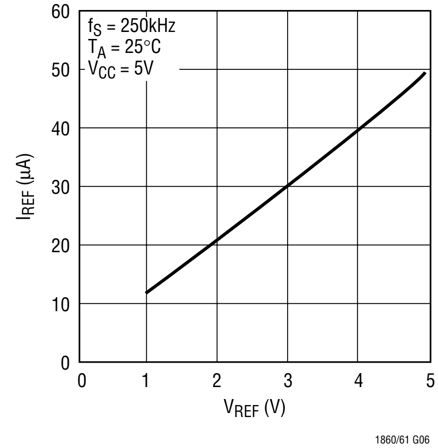
Reference Current vs Sample Rate



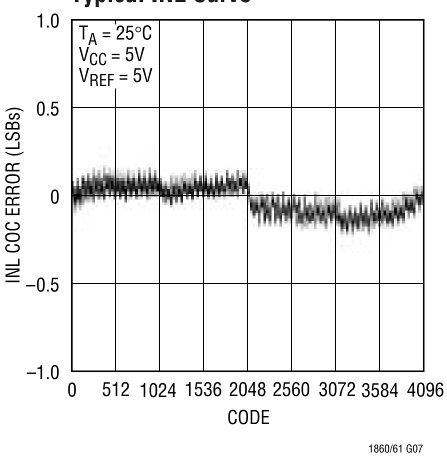
Reference Current vs Temperature



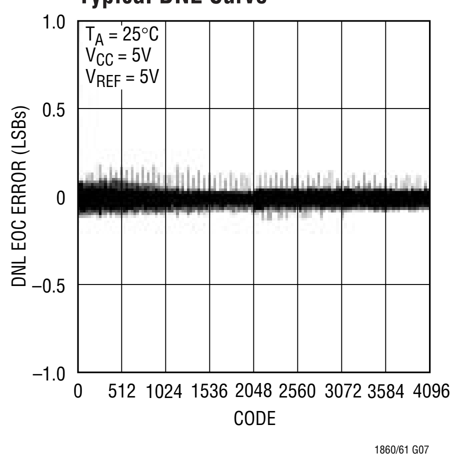
Reference Current vs Reference Voltage



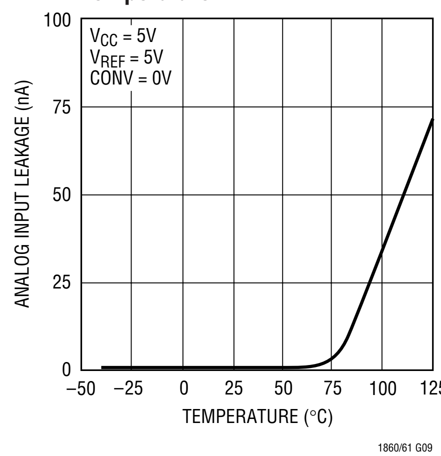
Typical INL Curve



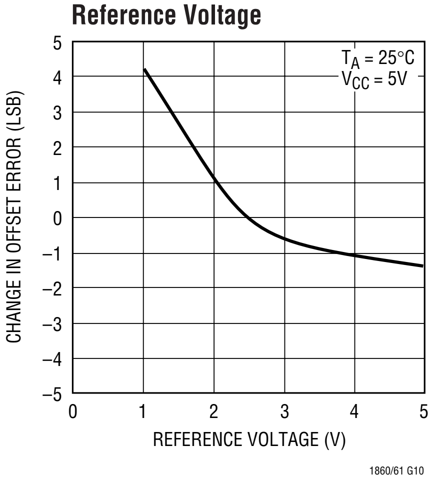
Typical DNL Curve



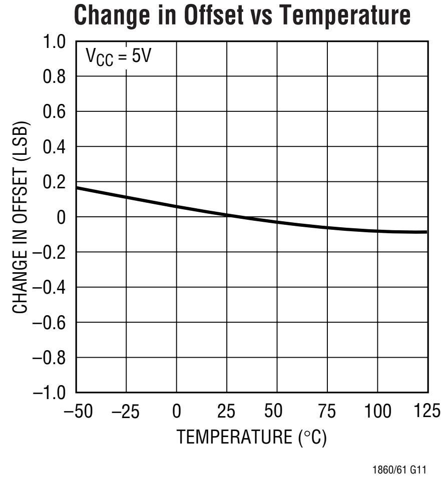
Analog Input Leakage vs Temperature



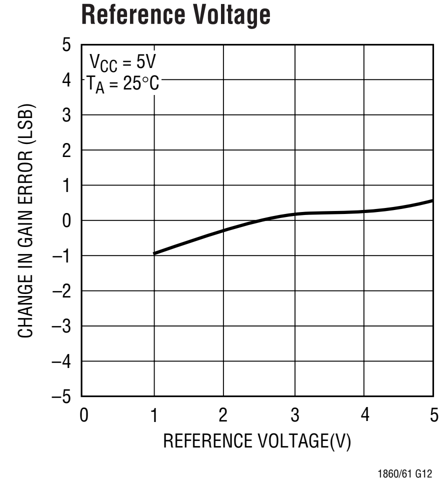
Change in Offset Error vs Reference Voltage



Change in Offset vs Temperature

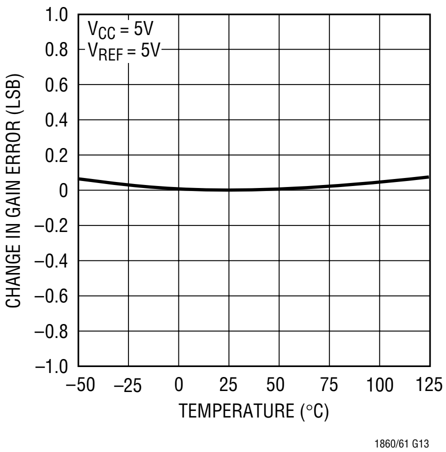


Change in Gain Error vs Reference Voltage

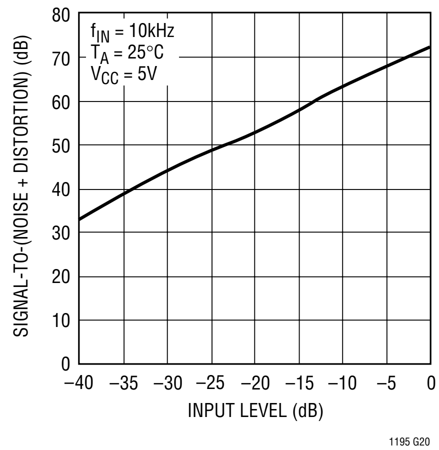


TYPICAL PERFORMANCE CHARACTERISTICS

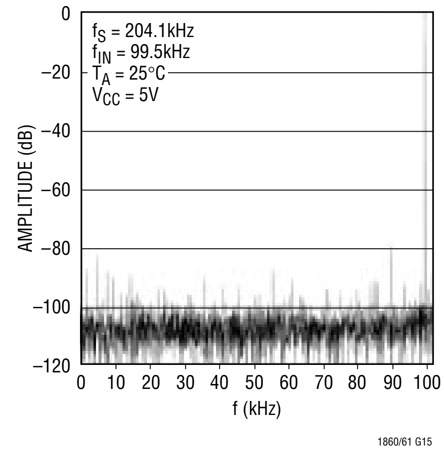
Change in Gain Error vs Temperature



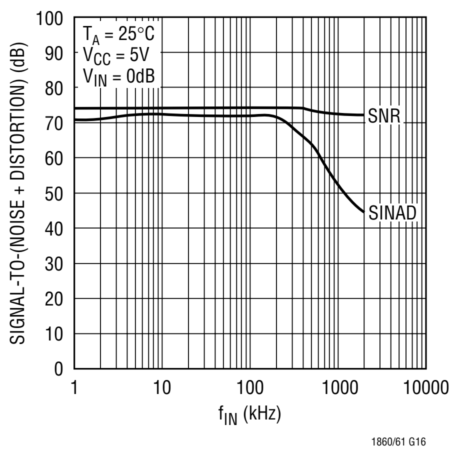
Signal-to-(Noise + Distortion) vs Input Level



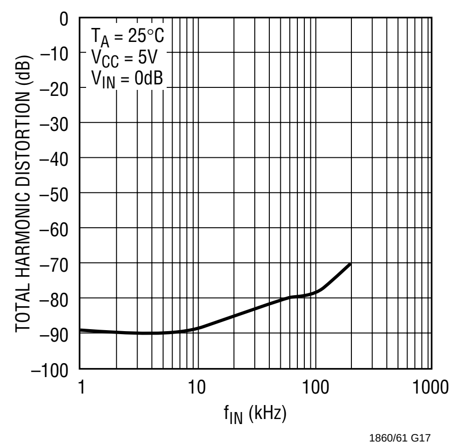
4096 Point FFT



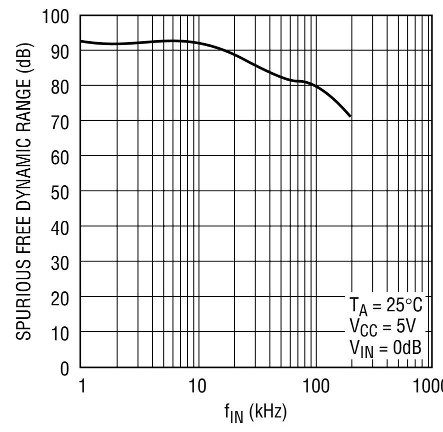
Signal-to-(Noise + Distortion) vs f_{IN}



Total Harmonic Distortion vs f_{IN}



Spurious Free Dynamic Range vs f_{IN}



PIN FUNCTIONS LTC1860

V_{REF} (Pin 1): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

IN^+, IN^- (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

CONV (Pin 5): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

SDO (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this pin.

SCK (Pin 7): Shift Clock Input. This clock synchronizes the serial data transfer.

V_{CC} (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

PIN FUNCTIONS

LTC1861 (MSOP Package)

CONV (Pin 1): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

CH0, CH1 (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to AGND.

AGND (Pin 4): Analog Ground. AGND should be tied directly to an analog ground plane.

DGND (Pin 5): Digital Ground. DGND should be tied directly to an analog ground plane.

SDI (Pin 6): Digital Data Input. The A/D configuration word is shifted into this input.

SDO (Pin 7): Digital Data Output. The A/D conversion result is shifted out of this output.

SCK (Pin 8): Shift Clock Input. This clock synchronizes the serial data transfer.

V_{CC} (Pin 9): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

V_{REF} (Pin 10): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to AGND.

LTC1861 (SO-8 Package)

CONV (Pin 1): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

CH0, CH1 (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

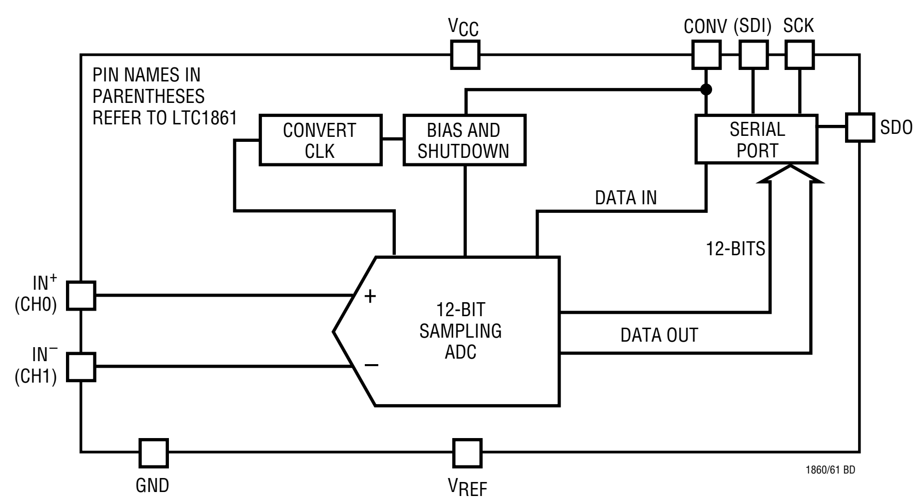
SDI (Pin 5): Digital Data Input. The A/D configuration word is shifted into this input.

SDO (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

SCK (Pin 7): Shift Clock Input. This clock synchronizes the serial data transfer.

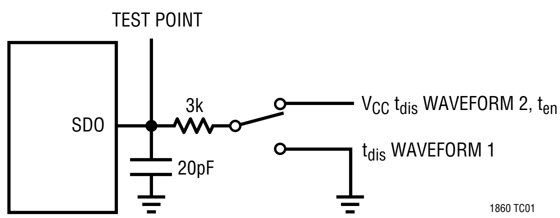
V_{CC} (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane. V_{REF} is tied internally to this pin.

FUNCTIONAL BLOCK DIAGRAM

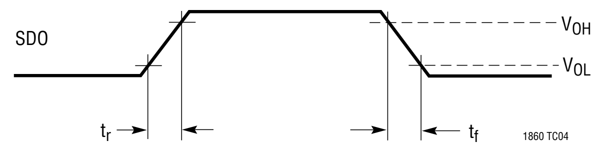


TEST CIRCUITS

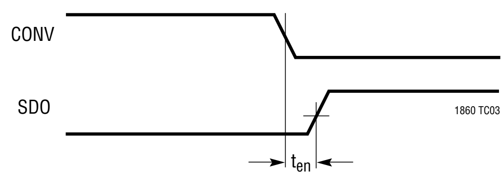
Load Circuit for t_{dDO}, t_r, t_f, t_{dis} and t_{en}



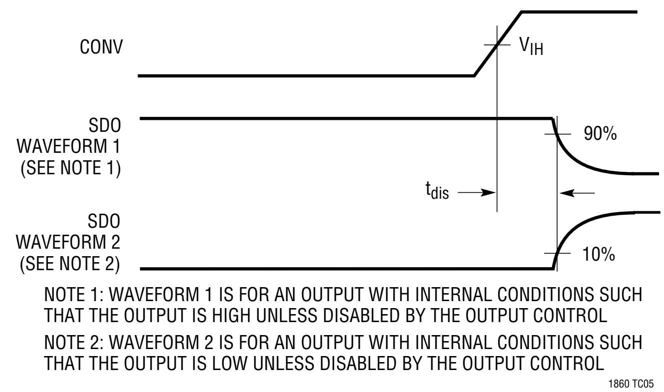
Voltage Waveforms for SDO Rise and Fall Times, t_r, t_f



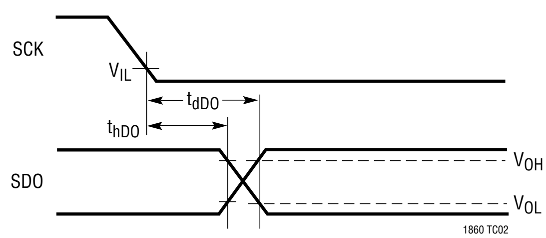
Voltage Waveforms for t_{en}



Voltage Waveforms for t_{dis}



Voltage Waveforms for SDO Delay Times, t_{dDO} and t_{hDO}



APPLICATIONS INFORMATION

LTC1860 OPERATION

Operating Sequence

The LTC1860 conversion cycle begins with the rising edge of CONV. After a period equal to t_{CONV}, the conversion is finished. If CONV is left high after this time, the LTC1860 goes into sleep mode drawing only leakage current. On the falling edge of CONV, the LTC1860 goes into sample mode and SDO is enabled. SCK synchronizes the data transfer with each bit being transmitted from SDO on the falling SCK edge. The receiving system should capture the data from SDO on the rising edge of SCK. After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 1.

Analog Inputs

The LTC1860 has a unipolar differential analog input. The converter will measure the voltage between the "IN^+" and "IN^-" inputs. A zero code will occur when IN^+ minus IN^- equals zero. Full scale occurs when IN^+ minus IN^- equals V_{REF} minus 1LSB. See Figure 2. Both the "IN^+" and "IN^-" inputs are sampled at the same time, so common mode noise on the inputs is rejected by the ADC. If "IN^-" is grounded and V_{REF} is tied to V_{CC}, a rail-to-rail input span will result on "IN^+" as shown in Figure 3.

Reference Input

The voltage on the reference input of the LTC1860 (and the LTC1861 MSOP package) defines the full-scale range of the A/D converter. These ADCs can operate with reference voltages from V_{CC} to 1V.

APPLICATIONS INFORMATION

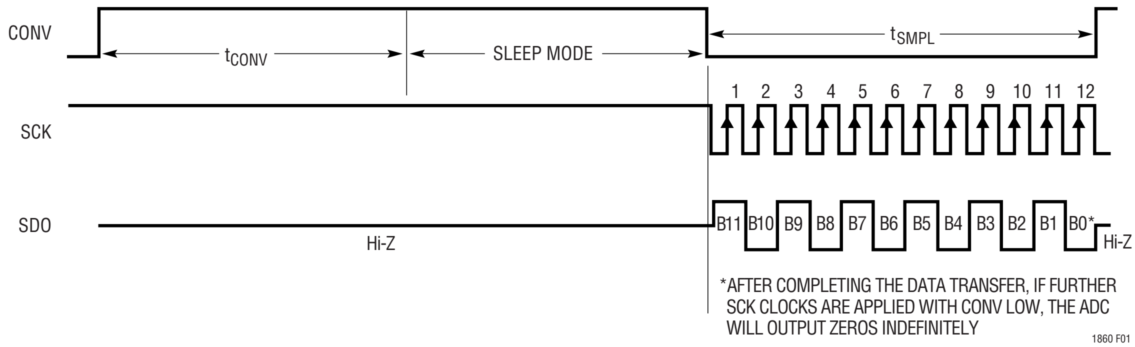


Figure 1. LTC1860 Operating Sequence

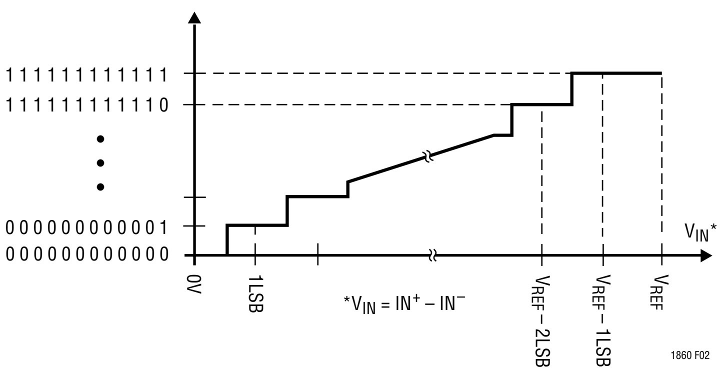


Figure 2. LTC1860 Transfer Curve

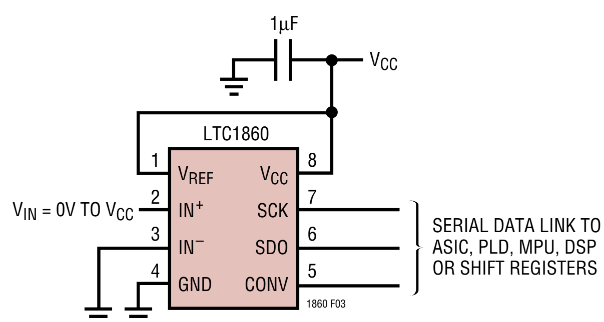


Figure 3. LTC1860 with Rail-to-Rail Input Span

LTC1861 OPERATION

Operating Sequence

The LTC1861 conversion cycle begins with the rising edge of CONV. After a period equal to t_{CONV}, the conversion is finished. If CONV is left high after this time, the LTC1861 goes into sleep mode. The LTC1861's 2-bit data word is clocked into the SDI input on the rising edge of SCK after CONV goes low. Additional inputs on the SDI pin are then ignored until the next CONV cycle. The shift clock (SCK) synchronizes the data transfer with each bit being transmitted on the falling SCK edge and captured on the rising SCK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex). After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 4.

Analog Inputs

The two bits of the input word (SDI) assign the MUX configuration for the next requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "–" signs in the selected row of the following table. In single-ended mode, all input channels are measured with respect to GND (or AGND). A zero code will occur when the "+" input minus the "–" input equals zero. Full scale occurs when the "+" input minus the "–" input equals V_{REF} minus 1LSB. See Figure 5. Both the "+" and "–" inputs are sampled at the same time so common mode noise is rejected. The input span in the SO-8 package is fixed at $V_{REF} = V_{CC}$. If the "–" input in differential mode is grounded, a rail-to-rail input span will result on the "+" input.

Reference Input

The reference input of the LTC1861 SO-8 package is internally tied to V_{CC}. The span of the A/D converter is therefore equal to V_{CC}. The voltage on the reference input of the LTC1861 MSOP package defines the span of the A/D converter. The LTC1861 MSOP package can operate with reference voltages from 1V to V_{CC}.

APPLICATIONS INFORMATION

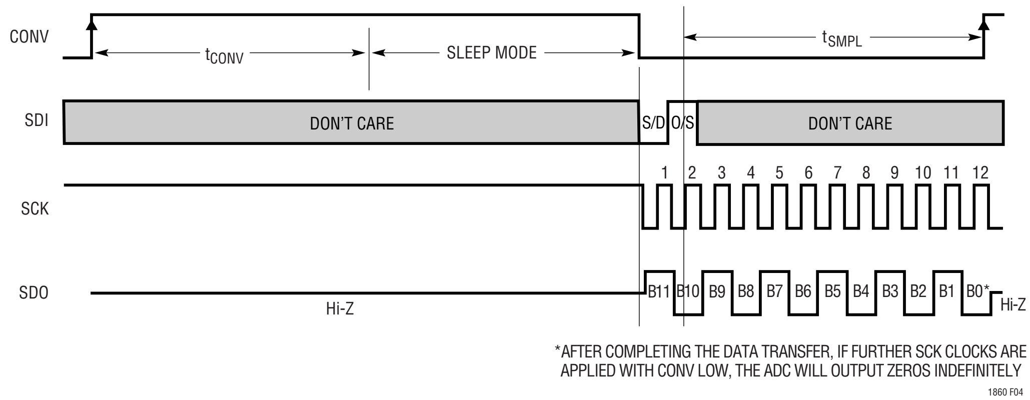


Figure 4. LTC1861 Operating Sequence

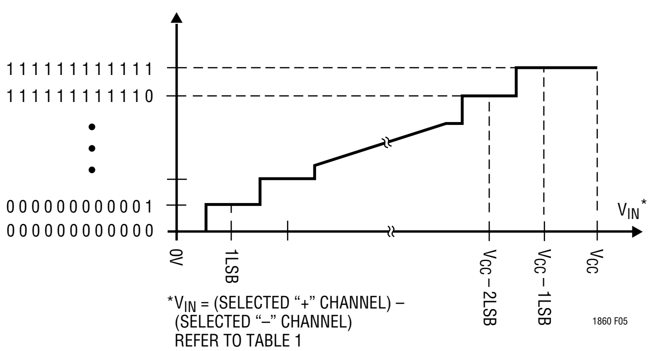


Figure 5. LTC1861 Transfer Curve

Table 1. Multiplexer Channel Selection

	MUX ADDRESS		CHANNEL #		
	SGL/DIFF	ODD/SIGN	0	1	GND
SINGLE-ENDED MUX MODE	1	0	+		–
	1	1		+	–
DIFFERENTIAL MUX MODE	0	0	+	–	
	0	1	–	+	

186465 TBL1

GENERAL ANALOG CONSIDERATIONS

Grounding

The LTC1860/LTC1861 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance, use a printed circuit board. The ground pins (AGND and DGND for the LTC1861 MSOP package and GND for the LTC1860 and LTC1861 SO-8 package) should be tied directly to the analog ground plane with minimum lead length.

Bypassing

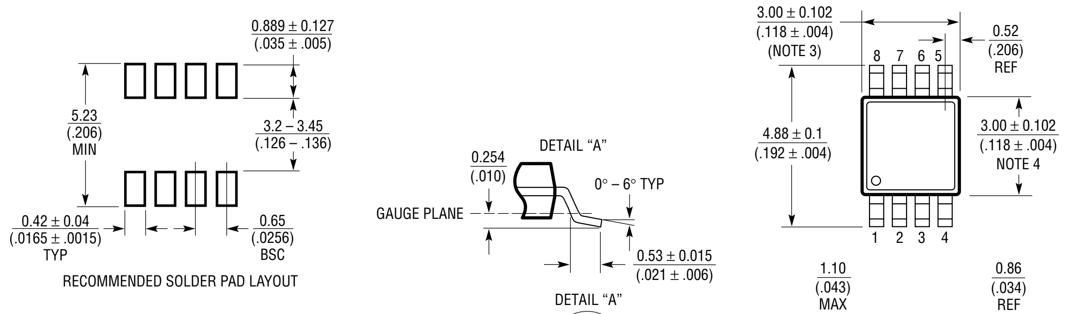
For good performance, the V_{CC} and V_{REF} pins must be free of noise and ripple. Any changes in the V_{CC}/V_{REF} voltage with respect to ground during the conversion cycle can induce errors or noise in the output code. Bypass the V_{CC} and V_{REF} pins directly to the analog ground plane with a minimum of 1μF tantalum. Keep the bypass capacitor leads as short as possible.

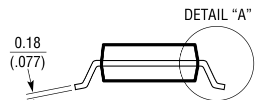
Analog Inputs

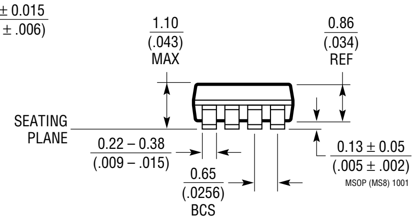
Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1860/LTC1861 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem if source resistances are less than 200Ω or high speed op amps are used (e.g., the LT®1211, LT1469, LT1807, LT1810, LT1630, LT1226 or LT1215). But if large source resistances are used, or if slow settling op amps drive the inputs, take care to ensure the transients caused by the current spikes settle completely before the conversion begins.

PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)

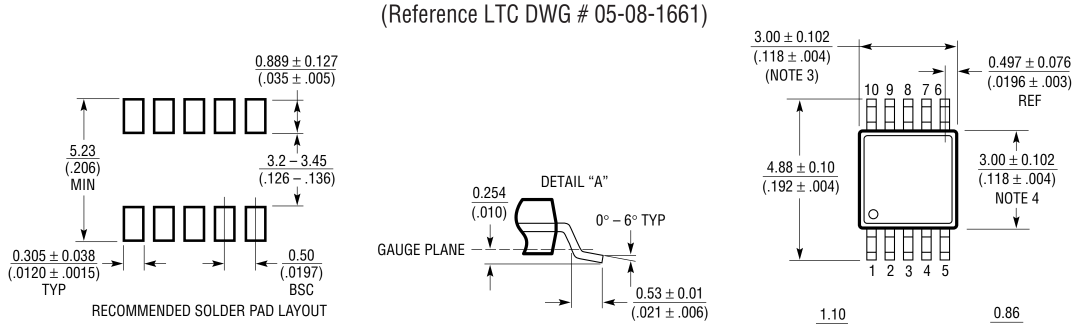


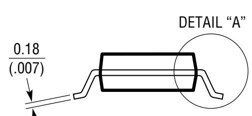


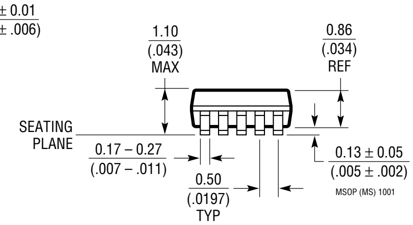


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)







NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
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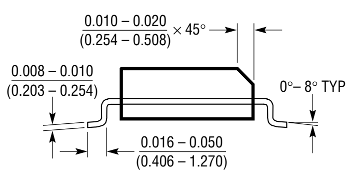
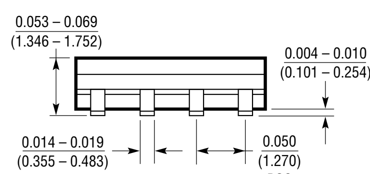
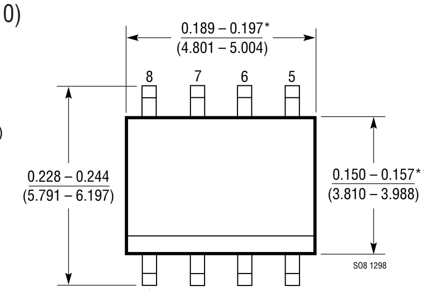
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)





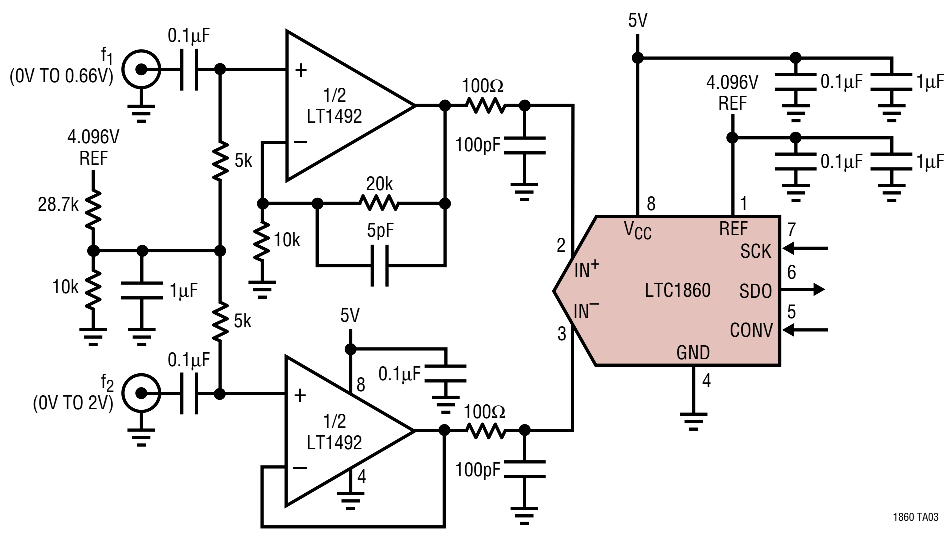


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

Sample Two Channels Simultaneously with a Single Input ADC



RELATED PARTS

PART NUMBER	SAMPLE RATE	POWER DISSIPATION	DESCRIPTION
12-Bit Serial I/O ADCs			
LTC1286/LTC1298	12.5ksps/11.1ksps	1.3mW/1.7mW	1-Channel with Ref. Input (LTC1286), 2-Channel (LTC1298), 5V
LTC1400	400ksps	75mW	1-Channel, Bipolar or Unipolar Operation, Internal Reference, 5V
LTC1401	200ksps	15mW	SO-8 with Internal Reference, 3V
LTC1402	2.2Msps	90mW	Serial I/O, Bipolar or Unipolar, Internal Reference
LTC1404	600ksps	25mW	SO-8 with Internal Reference, Bipolar or Unipolar, 5V
14-Bit Serial I/O ADCs			
LTC1417	400ksps	20mW	16-Pin SSOP, Unipolar or Bipolar, Reference, 5V
LTC1418	200ksps	15mW	Serial/Parallel I/O, Internal Reference, 5V
16-Bit Serial I/O ADCs			
LTC1609	200ksps	65mW	Configurable Bipolar or Unipolar Input Ranges, 5V
LTC1864/LTC1865	250ksps	4.25mW	SO-8, MS8, 1-Channel, 5V/SO-8, MS10, 2-Channel, 5V
References			
LT1460	Micropower Precision Series Reference		Bandgap, 130µA Supply Current, 10ppm/°C, Available in SOT-23
LT1790	Micropower Low Dropout Reference		60µA Supply Current, 10ppm/°C, SOT-23

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