LINEAR TECHNOLOGY

Dual 90MHz, 22V/µs
16-Bit Accurate Operational Amplifier

FEATURES

- **90MHz Gain Bandwidth, f = 100kHz**
- **Maximum Input Offset Voltage: 125µV**
- **Settling Time: 900ns (A_V = –1, 150µV, 10V Step)**
- **22V/µs Slew Rate**
- Low Distortion: –96.5dB for 100kHz, $10V_{P-P}$
- Maximum Input Offset Voltage Drift: 3µV/°C
- Maximum Inverting Input Bias Current: 10nA
- Minimum DC Gain: 300V/mV
- Minimum Output Swing into 2k: ±12.8V
- Unity-Gain Stable
- Input Noise Voltage: 5nV/$\sqrt{Hz}$
- Input Noise Current: 0.6pA/$\sqrt{Hz}$
- Total Input Noise Optimized for 1kΩ < R_S < 20kΩ
- Specified at ±5V and ±15V Supplies

APPLICATIONS

- Precision Instrumentation
- High Accuracy Data Acquisition Systems
- 16-Bit DAC Current-to-Voltage Converter
- ADC Buffer
- Low Distortion Active Filters
- Photodiode Amplifiers

DESCRIPTION

The LT®1469 is a dual, precision high speed operational amplifier with 16-bit accuracy and 900ns settling to 150µV for 10V steps. This unique blend of precision and AC performance makes the LT1469 the optimum choice for high accuracy applications such as DAC current-to-voltage conversion and ADC buffers. The initial accuracy and drift characteristics of the input offset voltage and inverting input bias current are tailored for inverting applications.

The 90MHz gain bandwidth ensures high open-loop gain at frequency for reducing distortion. In noninverting applications such as an ADC buffer, the low distortion and DC accuracy allow full 16-bit AC and DC performance.

The 22V/µs slew rate of the LT1469 improves large signal performance compared to other precision op amps in applications such as active filters and instrumentation amplifiers.

The LT1469 is available in a space saving 4mm × 4mm leadless package, as well as in small outline and DIP packages. A single version, the LT1468, is also available.
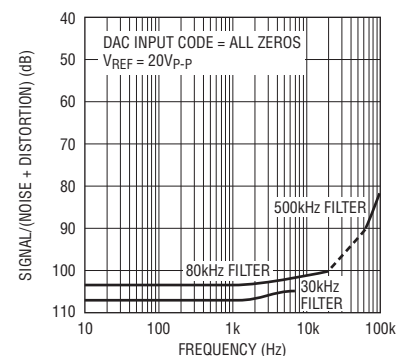
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TYPICAL APPLICATION

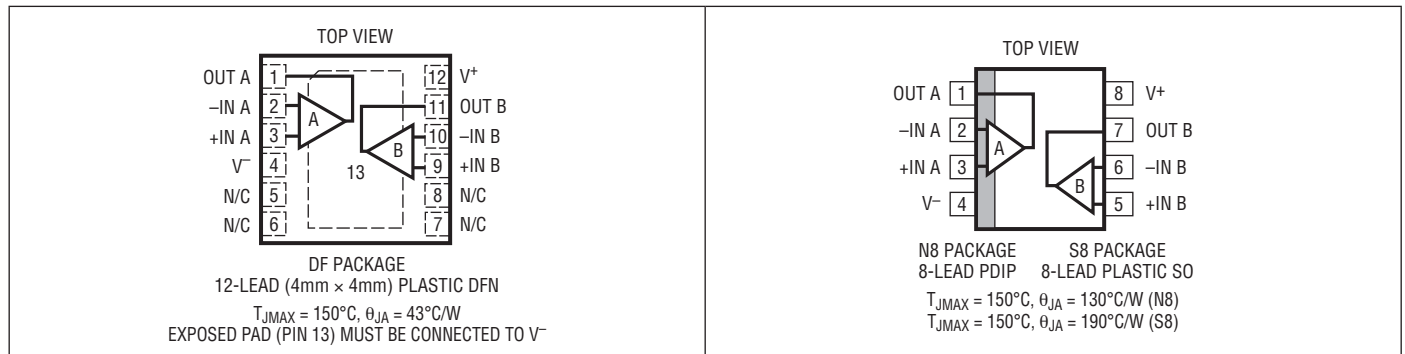16-Bit DAC I-to-V Converter and Reference Inverter for Bipolar Output Swing (V_{OUT} = –10V to 10V)
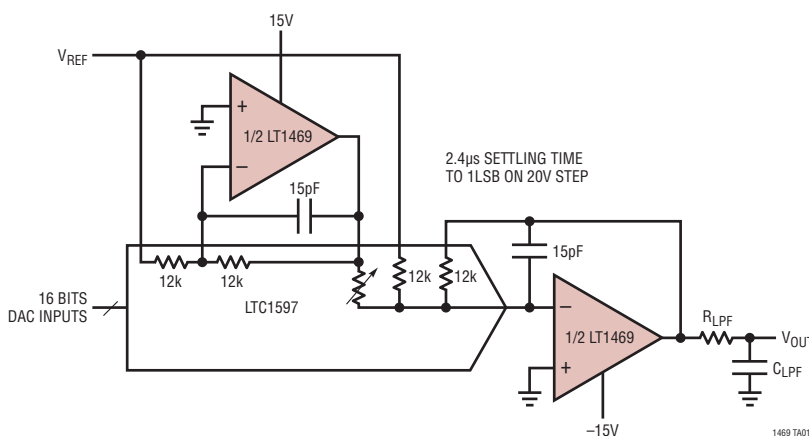
Bipolar Multiplying Mode (LTC1597)
Signal-to-(Noise + Distortion)

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LT1469

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V⁺ to V⁻)................................36V
Input Current (Note 2)..±10mA
Output Short-Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range (Note 4).... −40°C to 85°C

Specified Temperature Range (Note 5) .... −40°C to 85°C
Maximum Junction Temperature.......................... 150°C
Storage Temperature Range................... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)
     S8 and N8 Package.. 300°C

PIN CONFIGURATION

TOP VIEW

OUT A [1] ... [12] V⁺
−IN A [2] ... [11] OUT B
+IN A [3] ... [10] −IN B
V⁻ [4] 13 [9] +IN B
N/C [5] ... [8] N/C
N/C [6] ... [7] N/C

DF PACKAGE
12-LEAD (4mm × 4mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) MUST BE CONNECTED TO V⁻

TOP VIEW

OUT A [1] ... [8] V+
−IN A [2] ... [7] OUT B
+IN A [3] ... [6] −IN B
V⁻ [4] ... [5] +IN B

N8 PACKAGE   S8 PACKAGE
8-LEAD PDIP   8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S8)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1469CN8#PBF	NA	LT1469CN8	8-Lead PDIP	0°C to 70°C
LT1469IN8#PBF	NA	LT1469IN8	8-Lead PDIP	−40°C to 85°C
LT1469CS8#PBF	LT1469CS8#TRPBF	1469	8-Lead Plastic Small Outline	0°C to 70°C
LT1469IS8#PBF	LT1469IS8#TRPBF	1469I	8-Lead Plastic Small Outline	−40°C to 85°C
LT1469ACDF#PBF	LT1469ACDF#TRPBF	1469	12-Lead (4mm × 4mm) Plastic DFN	0°C to 70°C
LT1469AIDF#PBF	LT1469AIDF#TRPBF	1469	12-Lead (4mm × 4mm) Plastic DFN	−40°C to 85°C
LT1469CDF#PBF	LT1469CDF#TRPBF	1469	12-Lead (4mm × 4mm) Plastic DFN	0°C to 70°C
LT1469IDF#PBF	LT1469IDF#TRPBF	1469	12-Lead (4mm × 4mm) Plastic DFN	−40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT1469CN8	NA	LT1469CN8	8-Lead PDIP	0°C to 70°C
LT1469IN8	NA	LT1469IN8	8-Lead PDIP	−40°C to 85°C
LT1469CS8	LT1469CS8#TR	1469	8-Lead Plastic Small Outline	0°C to 70°C
LT1469IS8	LT1469IS8#TR	1469I	8-Lead Plastic Small Outline	−40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

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ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	N8, S8 Packages	±15V ±5V		50 50	125 200	µV µV
		LT1469A, DF Package	±15V ±5V		50 50	125 200	µV µV
		LT1469, DF Package	±15V ±5V		100 150	225 300	µV µV
I_{OS}	Input Offset Current		±5V to ±15V		13	±50	nA
I_B-	Inverting Input Bias Current		±5V to ±15V		3	±10	nA
I_B+	Noninverting Input Bias Current		±5V to ±15V		−10	±40	nA
	Input Noise Voltage	0.1Hz to 10Hz	±5V to ±15V		0.3		$µV_{P-P}$
e_n	Input Noise Voltage Density	f = 10kHz	±5V to ±15V		5		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz	±5V to ±15V		0.6		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	Common Mode, $V_{CM} = ±12.5V$ Differential	±15V ±15V	100 50	240 150		MΩ kΩ
C_{IN}	Input Capacitance		±15V		4		pF
V_{CM}	Input Voltage Range (Positive)	Guaranteed by CMRR	±15V ±5V	12.5 2.5	13.5 3.6		V V
	Input Voltage Range (Negative)	Guaranteed by CMRR	±15V ±5V		−14.3 −4.4	−12.5 −2.5	V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = ±12.5V$ $V_{CM} = ±2.5V$	±15V ±5V	96 96	110 112		dB dB
	Minimum Supply Voltage	Guaranteed by PSRR			±2.5	±4.5	V
PSRR	Power Supply Rejection Ratio	$V_S = ±4.5V$ to ±15V		100	112		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = ±12.5V$, $R_L = 10k$ $V_{OUT} = ±12.5V$, $R_L = 2k$ $V_{OUT} = ±2.5V$, $R_L = 10k$ $V_{OUT} = ±2.5V$, $R_L = 2k$	±15V ±15V ±5V ±5V	300 300 200 200	2000 2000 8000 8000		V/mV V/mV V/mV V/mV
V_{OUT}	Maximum Output Swing	$R_L = 10k$, 1mV Overdrive $R_L = 2k$, 1mV Overdrive $R_L = 10k$, 1mV Overdrive $R_L = 2k$, 1mV Overdrive	±15V ±15V ±5V ±5V	±13.0 ±12.8 ±3.0 ±2.8	±13.6 ±13.5 ±3.7 ±3.6		V V V V
I_{OUT}	Maximum Output Current	$V_{OUT} = ±12.5V$, 1mV Overdrive $V_{OUT} = ±2.5V$, 1mV Overdrive	±15V ±5V	±15 ±15	±22 ±22		mA mA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0V$, 0.2V Overdrive (Note 3)	±15V	±25	±40		mA
SR	Slew Rate	$A_V = −10$, $R_L = 2k$ (Note 6)	±15V ±5V	15 11	22 17		V/µs V/µs
FPBW	Full-Power Bandwidth	10V Peak, (Note 7) 3V Peak, (Note 7)	±15V ±5V		350 900		kHz kHz
GBW	Gain Bandwidth Product	f = 100kHz, $R_L = 2k$	±15V ±5V	60 55	90 88		MHz MHz
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10% to 90%, 0.1V Step	±15V ±5V		11 12		ns ns
OS	Overshoot	$A_V = 1$, 0.1V Step	±15V ±5V		30 35		% %
t_{PD}	Propagation Delay	$A_V = 1$, 50% V_{IN} to 50% V_{OUT}, 0.1V Step	±15V ±5V		9 10		ns ns

ELECTRICAL CHARACTERISTICS T_A = 25°C. V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
t_S	Settling Time	10V Step, 0.01%, A_V = −1	±15V		760		ns
		10V Step, 150µV, A_V = −1	±15V		900		ns
		5V Step, 0.01%, A_V = −1	±5V		770		ns
THD	Total Harmonic Distortion	A_V = −1, V_{OUT} = 10V$_{P-P}$, f = 100kHz	±15V		−96.5		dB
		A_V = 1, V_{OUT} = 20V$_{P-P}$, f = 1kHz	±15V		−125		dB
R_{OUT}	Output Resistance	A_V = 1, f = 100kHz	±15V		0.02		Ω
	Channel Separation	V_{OUT} = ±12.5V, R_L = 2k	±15V	100	130		dB
		V_{OUT} = ±2.5V, R_L = 2k	±5V	100	130		dB
I_S	Supply Current	Per Amplifier	±15V		4.1	5.2	mA
			±5V		3.8	5	mA
ΔV_{OS}	Input Offset Voltage Match	S8, DF A-Grade	±15V		30	225	µV
			±5V		50	350	µV
ΔI_B−	Inverting Input Bias Current Match		±5V to ±15V		2	18	nA
ΔI_B+	Noninverting Input Bias Current Match		±5V to ±15V		5	78	nA
ΔCMRR	Common Mode Rejection Match	V_{CM} = ±12.5V (Note 9)	±15V	93	113		dB
		V_{CM} = ±2.5V (Note 9)	±5V	93	115		dB
ΔPSRR	Power Supply Rejection Match	V_S = ±4.5V to ±15V (Note 9)		97	115		dB

The ● denotes the specifications which apply over the full operating temperature range, 0°C ≤ T_A ≤ 70°C. V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	N8, S8 Packages	±15V	●			350	µV
			±5V	●			350	µV
		LT1469A, DF Package	±15V	●			225	µV
			±5V	●			275	µV
		LT1469, DF Package	±15V	●			450	µV
			±5V	●			450	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 8)	±15V	●		1	5	µV/°C
			±5V	●		1	3	µV/°C
I_{OS}	Input Offset Current		±5V to ±15V	●			±80	nA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 8)	±5V to ±15V	●		60		pA/°C
I_B−	Inverting Input Bias Current		±5V to ±15V	●			±20	nA
ΔI_B−/ΔT	Inverting Input Bias Current Drift	(Note 8)	±5V to ±15V	●		40		pA/°C
I_B+	Noninverting Input Bias Current		±5V to ±15V	●			±60	nA
V_{CM}	Input Voltage Range (Positive)	Guaranteed by CMRR	±15V	●	12.5			V
			±5V	●	2.5			V
	Input Voltage Range (Negative)	Guaranteed by CMRR	±15V	●			−12.5	V
			±5V	●			−2.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12.5V	±15V	●	94			dB
		V_{CM} = ±2.5V	±5V	●	94			dB
	Minimum Supply Voltage	Guaranteed by PSRR		●			±4.5	V
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±15V		●	95			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12.5V, R_L = 10k	±15V	●	100			V/mV
		V_{OUT} = ±12.5V, R_L = 2k	±15V	●	100			V/mV
		V_{OUT} = ±2.5V, R_L = 10k	±5V	●	100			V/mV
		V_{OUT} = ±2.5V, R_L = 2k	±5V	●	100			V/mV

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, 0°C ≤ T_A ≤ 70°C. V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OUT}	Maximum Output Swing	R_L = 10k, 1mV Overdrive	±15V	●	±12.9			V
		R_L = 2k, 1mV Overdrive	±15V	●	±12.7			V
		R_L = 10k, 1mV Overdrive	±5V	●	±2.9			V
		R_L = 2k, 1mV Overdrive	±5V	●	±2.7			V
I_{OUT}	Maximum Output Current	V_{OUT} = ±12.5V, 1mV Overdrive	±15V	●	±12.5			mA
		V_{OUT} = ±2.5V, 1mV Overdrive	±5V	●	±12.5			mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V, 0.2V Overdrive (Note 3)	±15V	●	±17			mA
SR	Slew Rate	A_V = –10, R_L = 2k (Note 6)	±15V	●	13			V/µs
			±5V	●	9			V/µs
GBW	Gain Bandwidth Product	f = 100kHz, R_L = 2k	±15V	●	55			MHz
			±5V	●	50			MHz
	Channel Separation	V_{OUT} = ±12.5V, R_L = 2k	±15V	●	98			dB
		V_{OUT} = ±2.5V, R_L = 2k	±5V	●	98			dB
I_S	Supply Current	Per Amplifier	±15V	●			6.5	mA
			±5V	●			6.3	mA
ΔV_{OS}	Input Offset Voltage Match	S8, DF A-Grade	±15V	●			600	µV
			±5V	●			600	µV
ΔI_B–	Inverting Input Bias Current Match		±5V to ±15V	●			38	nA
ΔI_B+	Noninverting Input Bias Current Match		±5V to ±15V	●			118	nA
ΔCMRR	Common Mode Rejection Match	V_{CM} = ±12.5V (Note 9)	±15V	●	91			dB
		V_{CM} = ±2.5V (Note 9)	±5V	●	91			dB
ΔPSRR	Power Supply Rejection Match	V_S = ±4.5V to ±15V (Note 9)		●	92			dB

The ● denotes the specifications which apply over the full operating temperature range, –40°C ≤ T_A ≤ 85°C, V_{CM} = 0V unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	N8, S8 Packages	±15V	●			500	µV
			±5V	●			500	µV
		LT1469A, DF Package	±15V	●			300	µV
			±5V	●			350	µV
		LT1469, DF Package	±15V	●			600	µV
			±5V	●			600	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 8)	±15V	●		1	6	µV/°C
			±5V	●		1	5	µV/°C
I_{OS}	Input Offset Current		±5V to ±15V	●			±120	nA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 8)	±5V to ±15V	●		120		pA/°C
I_B–	Inverting Input Bias Current		±5V to ±15V	●			±40	nA
ΔI_B–/ΔT	Inverting Input Bias Current Drift	(Note 8)	±5V to ±15V	●		80		pA/°C
I_B+	Noninverting Input Bias Current		±5V to ±15V	●			±80	nA
V_{CM}	Input Voltage Range (Positive)	Guaranteed by CMRR	±15V	●	12.5			V
			±5V	●	2.5			V
	Input Voltage Range (Negative)	Guaranteed by CMRR	±15V	●			–12.5	V
			±5V	●			–2.5	V

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LT1469

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, $-40°C \leq T_A \leq 85°C$, V_{CM} = 0V unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_SUPPLY		MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm12.5V$ $V_{CM} = \pm2.5V$	±15V ±5V	● ●	92 92		 ±4.5	dB dB
	Minimum Supply Voltage	Guaranteed by PSRR		●				V
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm15V$		●	93			dB
A_VOL	Large-Signal Voltage Gain	$V_{OUT} = \pm12.5V$, $R_L = 10k$ $V_{OUT} = \pm12.5V$, $R_L = 2k$ $V_{OUT} = \pm2.5V$, $R_L = 10k$ $V_{OUT} = \pm2.5V$, $R_L = 2k$	±15V ±15V ±5V ±5V	● ● ● ●	75 75 75 75			V/mV V/mV V/mV V/mV
V_OUT	Maximum Output Swing	$R_L = 10k$, 1mV Overdrive $R_L = 2k$, 1mV Overdrive $R_L = 10k$, 1mV Overdrive $R_L = 2k$, 1mV Overdrive	±15V ±15V ±5V ±5V	● ● ● ●	±12.8 ±12.6 ±2.8 ±2.6			V V V V
I_OUT	Maximum Output Current	$V_{OUT} = \pm12.5V$, 1mV Overdrive $V_{OUT} = \pm2.5V$, 1mV Overdrive	±15V ±5V	● ●	±7 ±7			mA mA
I_SC	Output Short-Circuit Current	$V_{OUT} = 0V$, 0.2V Overdrive (Note 3)	±15V	●	±12			mA
SR	Slew Rate	$A_V = -10$, $R_L = 2k$ (Note 6)	±15V ±5V	● ●	9 6			V/µs V/µs
GBW	Gain Bandwidth Product	$f = 100kHz$, $R_L = 2k$	±15V ±5V	● ●	45 40			MHz MHz
	Channel Separation	$V_{OUT} = \pm12.5V$, $R_L = 2k$ $V_{OUT} = \pm2.5V$, $R_L = 2k$	±15V ±5V	● ●	96 96			dB dB
I_S	Supply Current	Per Amplifier	±15V ±5V	● ●			7 6.8	mA mA
ΔV_OS	Input Offset Voltage Match	S8, DF A-Grade	±15V ±5V	● ●			800 800	µV µV
ΔI_B−	Inverting Input Bias Current Match		±5V to ±15V	●			78	nA
ΔI_B+	Noninverting Input Bias Current Match		±5V to ±15V	●			158	nA
ΔCMRR	Common Mode Rejection Match	$V_{CM} = \pm12.5V$ (Note 9) $V_{CM} = \pm2.5V$ (Note 9)	±15V ±5V	● ●	89 89			dB dB
ΔPSRR	Power Supply Rejection Match	$V_S = \pm4.5V$ to $\pm15V$ (Note 9)		●	90			dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes and two 100Ω series resistors. If the differential input voltage exceeds 0.7V, the input current should be limited to less than 10mA. Input voltages outside the supplies will be clamped by ESD protection devices and input currents should also be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: The LT1469C and LT1469I are guaranteed functional over the operating temperature range of −40°C to 85°C.

Note 5: The LT1469C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet specified performance from −40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1469I is guaranteed to meet specified performance from −40°C to 85°C.

Note 6: Slew rate is measured between ±8V on the output with ±12V swing for ±15V supplies and ±2V on the output with ±3V swing for ±5V supplies.

Note 7: Full-power bandwidth is calculated from the slew rate. FPBW = $SR/2\pi V_P$.

Note 8: This parameter is not 100% tested.

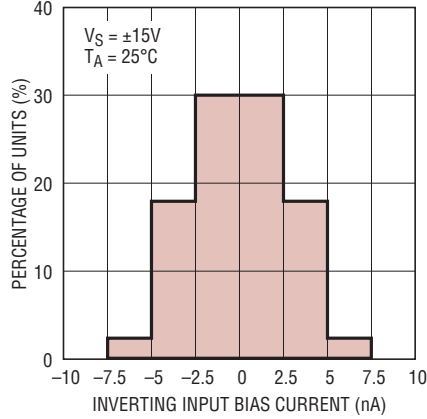**Note 9:** ΔCMRR and ΔPSRR are defined as follows: 1) CMRR and PSRR are measured in µV/V on each amplifier; 2) the difference between the two sides is calculated in µV/V; 3) the result is converted to dB.
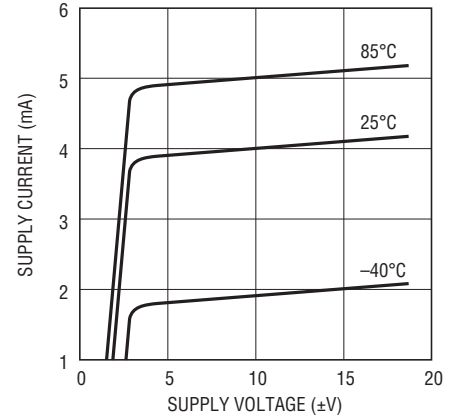
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TYPICAL PERFORMANCE CHARACTERISTICS
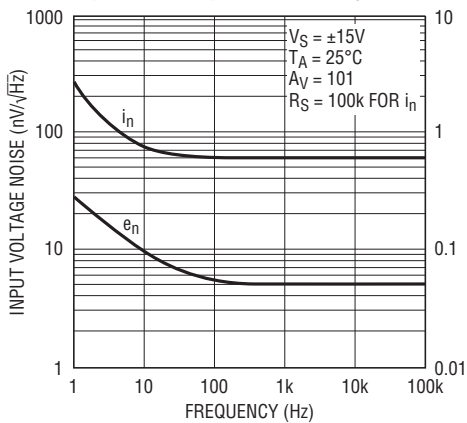
Distribution of Input Offset Voltage
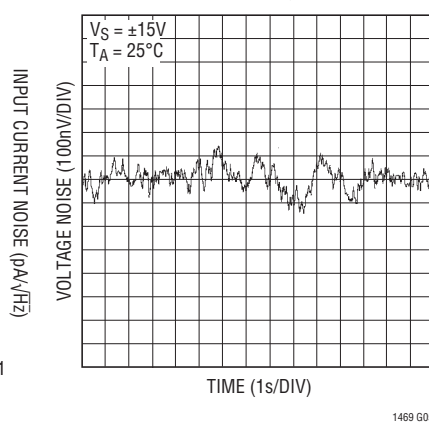

1469 G01
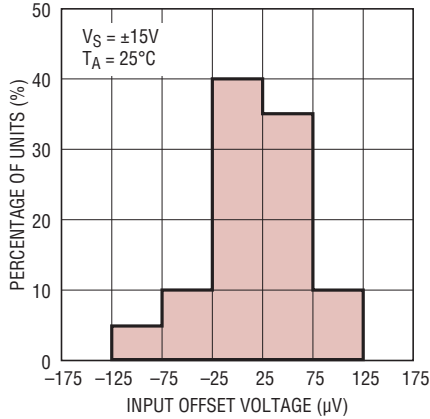
Distribution of Inverting Input Bias Current

1469 G02

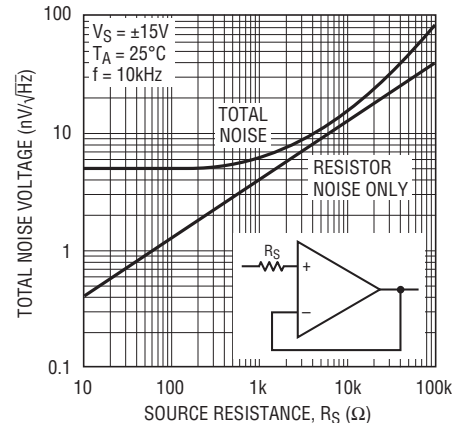**Supply Current vs Supply Voltage and Temperature**

1469 G03
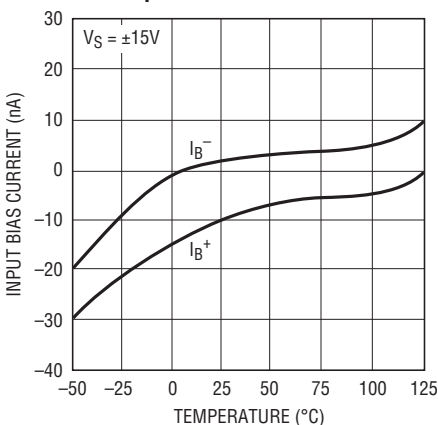
Input Noise Spectral Density

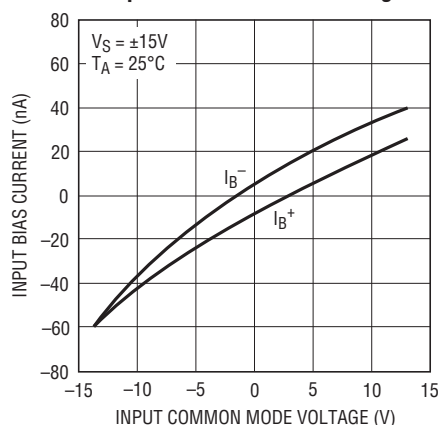1469 G04

0.1Hz to 10Hz Voltage Noise

1469 G05

Total Noise vs Unmatched Source Resistance

1469 G06

Input Bias Current vs Temperature
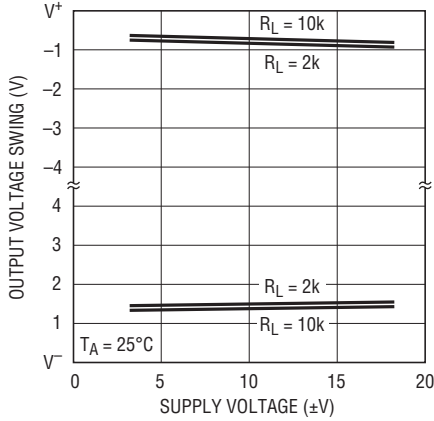

1469 G07

Input Bias Current vs Input Common Mode Voltage

1469 G08

Input Common Mode Range vs Supply Voltage

1469 G09

1469fa
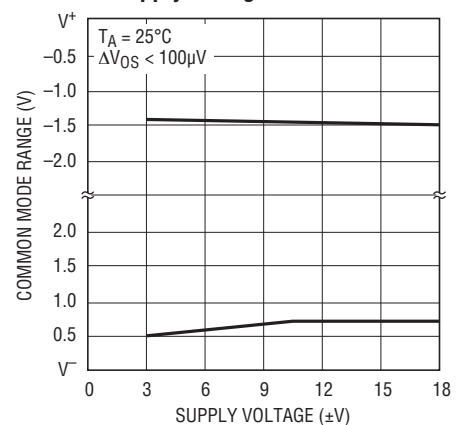
LT1469

TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage Swing vs Supply Voltage

1469 G10

Output Voltage Swing vs Load Current
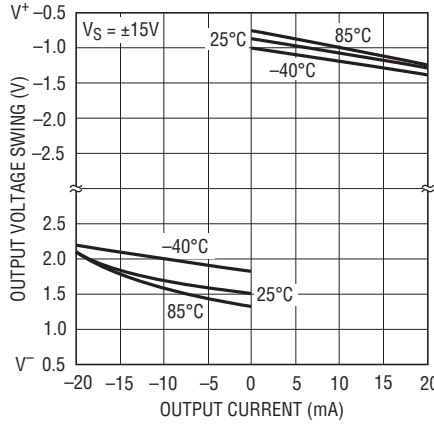
1469 G11

Output Short-Circuit Current vs Temperature
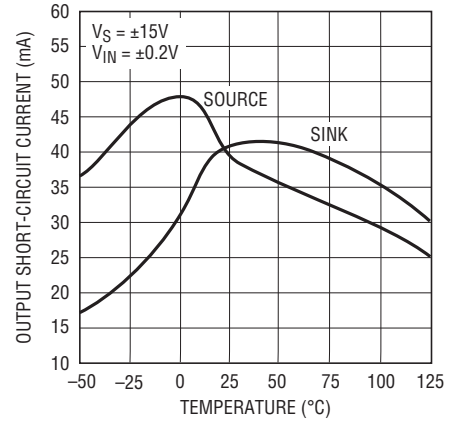
1469 G12

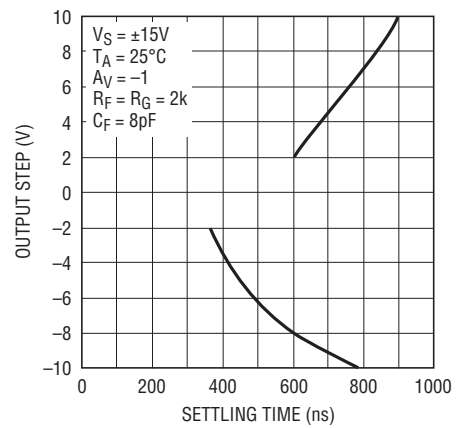**Settling Time to 0.01% vs Output Step, V_S = ±15V**
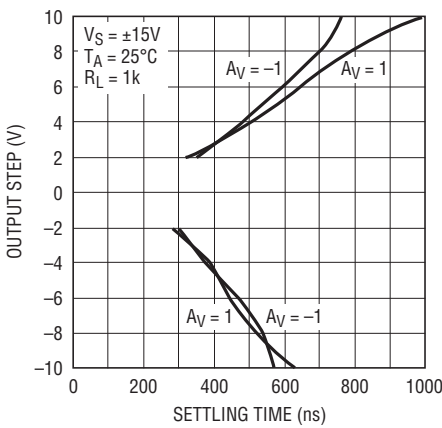
1469 G13
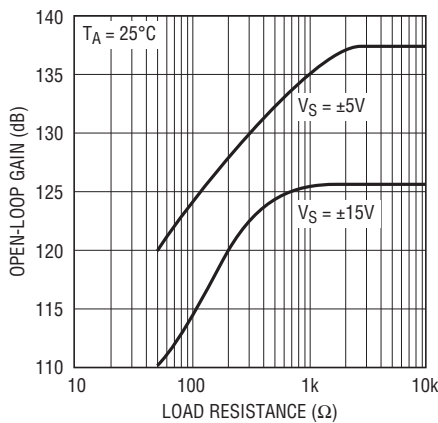
Settling Time to 0.01% vs Output Step, V_S = ±5V
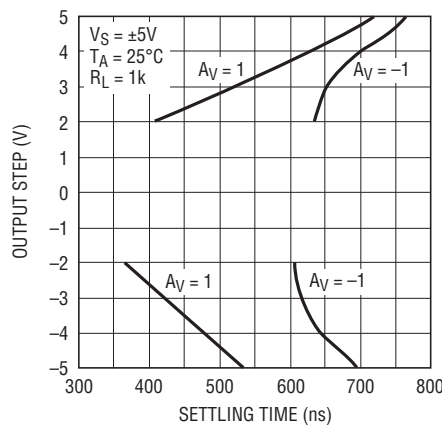
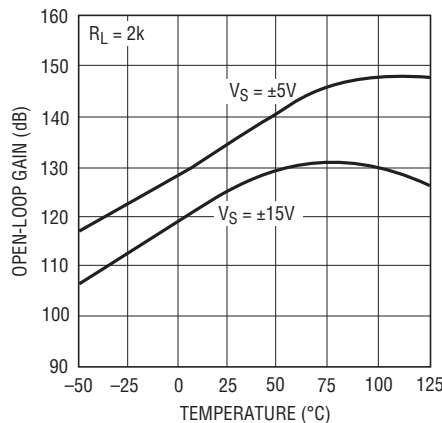1469 G14

Settling Time to 150µV vs Output Step
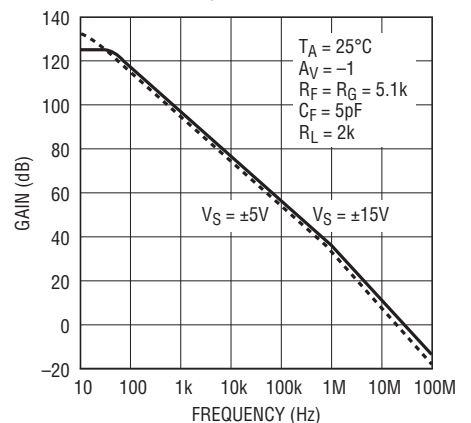
1469 G15

Open-Loop Gain vs Resistive Load

1469 G16

Open-Loop Gain vs Temperature

1469 G17

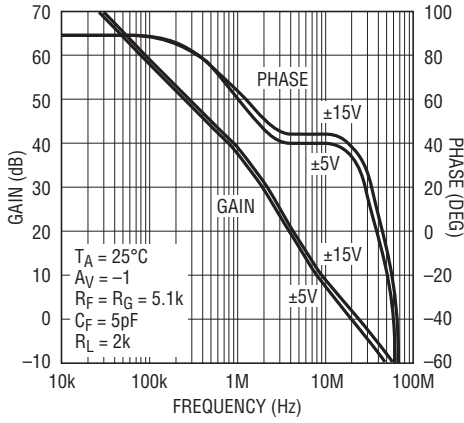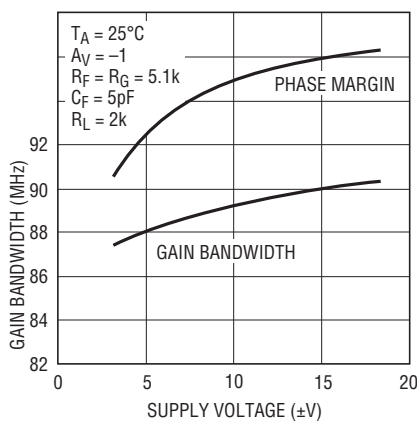**Open-Loop Gain vs Frequency**

1469 G18

1469fa

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TYPICAL PERFORMANCE CHARACTERISTICS

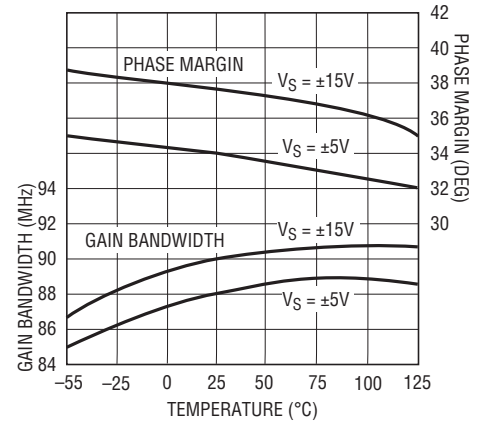### Open-Loop Gain and Phase vs Frequency

1469 G19

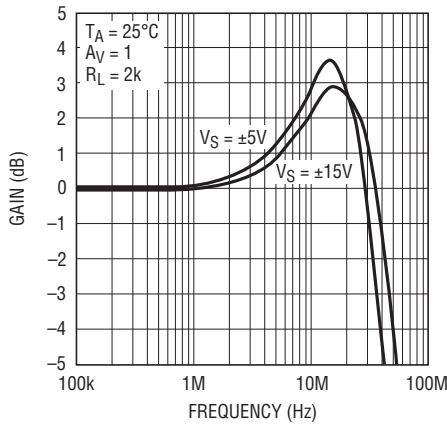### Gain Bandwidth and Phase Margin vs Supply Voltage

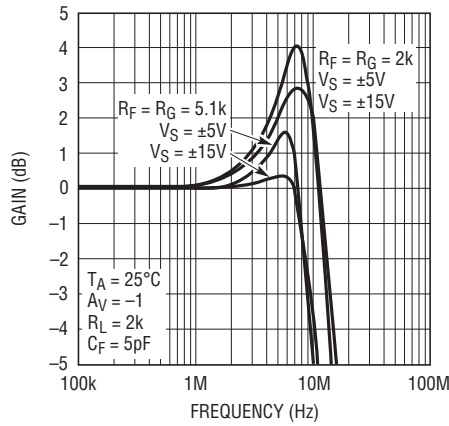1469 G20

Gain Bandwidth and Phase Margin vs Temperature

1469 G21

Gain vs Frequency, $A_V = 1$
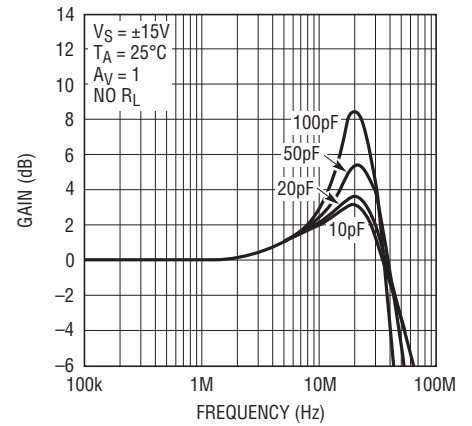

1469 G22

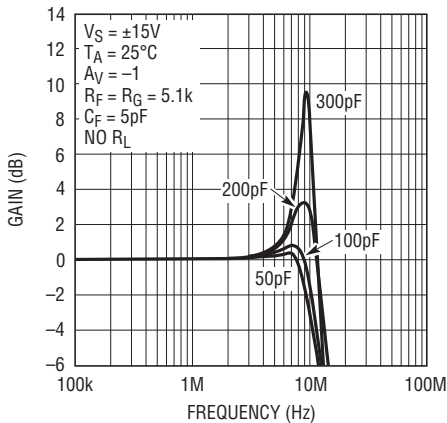### Gain vs Frequency, $A_V = -1$

1469 G23
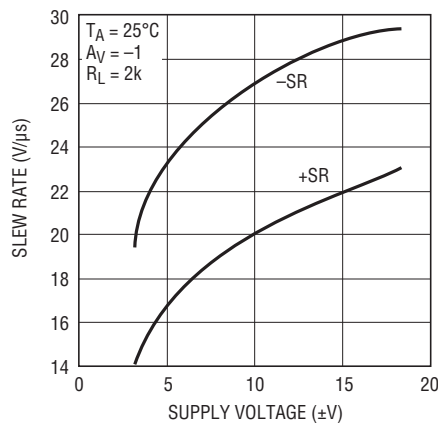
Gain vs Frequency, $A_V = 1$

1469 G24

Gain vs Frequency, $A_V = -1$

1469 G25

Slew Rate vs Supply Voltage

1469 G26

Slew Rate vs Temperature

1469 G27

1469fa
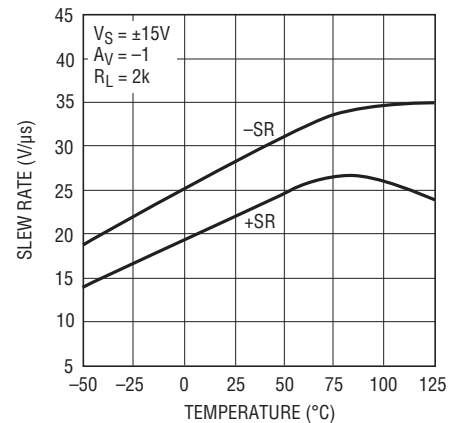
TYPICAL PERFORMANCE CHARACTERISTICS

Power Supply Rejection Ratio vs Frequency
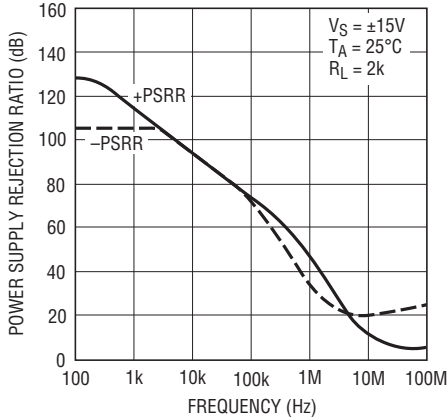
1469 G28

Common Mode Rejection Ratio vs Frequency
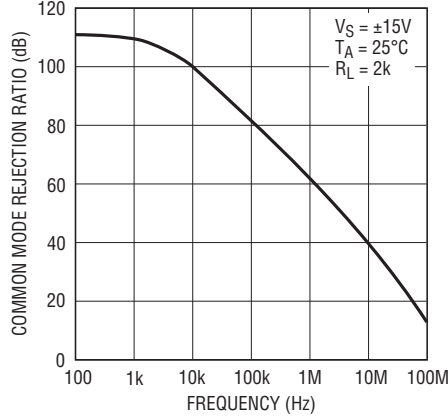
1469 G29

Channel Separation vs Frequency
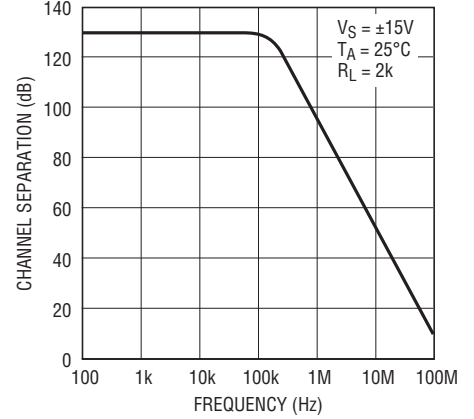
1469 G30

Undistorted Output Swing vs Frequency, $V_S = \pm 5V$

1469 G31

Undistorted Output Swing vs Frequency, $V_S = \pm 15V$

1469 G32

Output Impedance vs Frequency

1469 G33

Total Harmonic Distortion vs Frequency

1469 G34

Total Harmonic Distortion + Noise vs Amplitude

1469 G35

Warm-Up Drift vs Time

1469 G36

1469fa
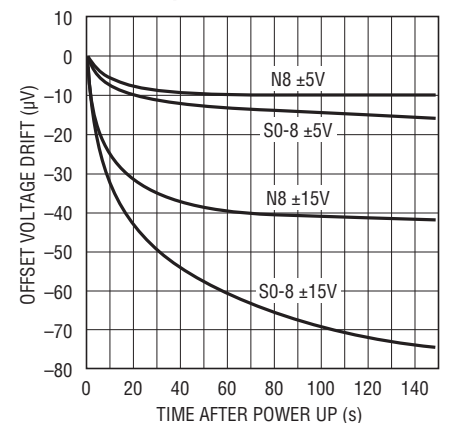
TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient, $A_V = 1$
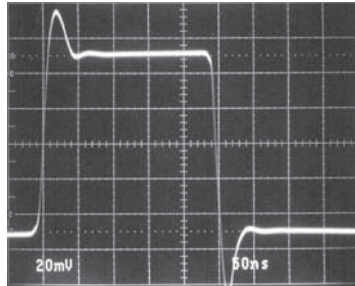
$V_S = \pm15V$ 1469 G37

Small-Signal Transient, $A_V = -1$
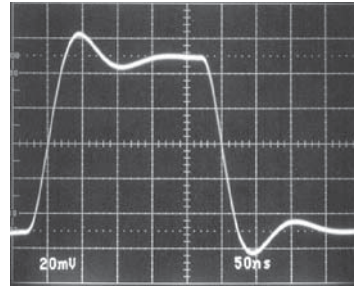
$V_S = \pm15V$ 1469 G38

Large-Signal Transient, $A_V = 1$
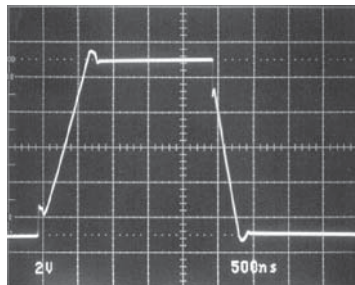
$V_S = \pm15V$ 1469 G39

Large-Signal Transient, $A_V = -1$
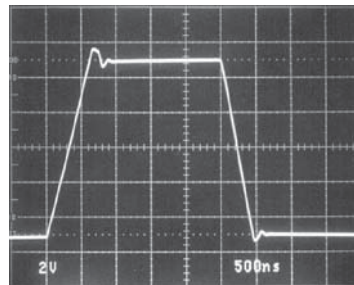
$V_S = \pm15V$ 1469 G40
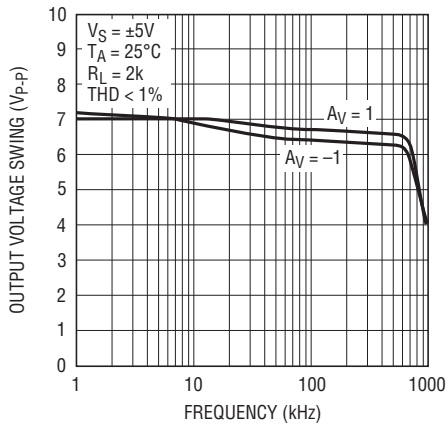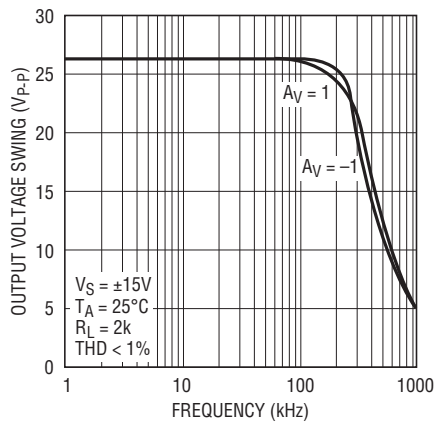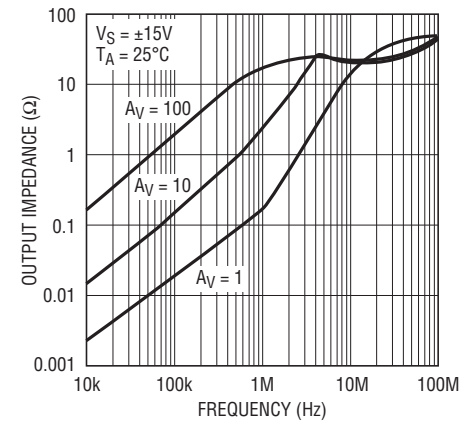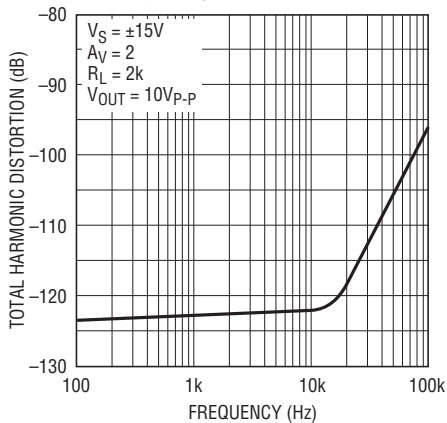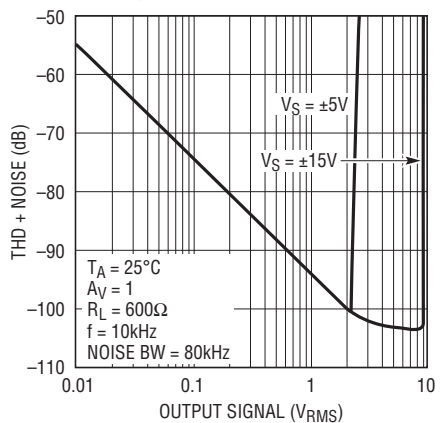
APPLICATIONS INFORMATION

Layout and Passive Components

The LT1469 requires attention to detail in board layout in order to maximize DC and AC performance. For best AC results (for example, fast settling time) use a ground plane, short lead lengths and RF quality bypass capacitors (0.01µF to 0.1µF) in parallel with low ESR bypass capacitors (1µF to 10µF tantalum). For best DC performance, use "star" grounding techniques, equalize input trace lengths and minimize leakage (e.g., 1.5GΩ of leakage between an input and a 15V supply will generate 10nA—equal to the maximum I_B- specification).

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: for inverting configurations tie the ring to ground, in noninverting connections tie the ring to the inverting input (note the input capacitance will increase which may require a compensating capacitor as discussed below).

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the inputs can exceed the inherent drift of

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APPLICATIONS INFORMATION

the amplifier. Air currents over device leads should be minimized, package leads should be short and the two input leads should be as close together as possible and maintained at the same temperature.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or even oscillations. For feedback resistors greater than 2k, a feedback capacitor of value $C_F > R_G \cdot C_{IN}/R_F$ should be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is one, and a large feedback resistor is used, C_F should be greater than or equal to C_{IN}. An example would be a DAC I-to-V converter as shown on the front page of the data sheet where the DAC can have many tens of picofarads of output capacitance. Another example would be a gain of –1 with 5k resistors; a 5pF to 10pF capacitor should be added across the feedback resistor.

Input Considerations

Each input of the LT1469 is protected with a 100Ω series resistor and back-to-back diodes across the bases of the input devices. If large differential input voltages are anticipated, limit the input current to less than 10mA with an external series resistor. Each input also has two ESD clamp diodes—one to each supply. If an input is driven beyond the supply, limit the current with an external resistor to less than 10mA.

The LT1469 employs bias current cancellation at the inputs. The inverting input current is trimmed at zero common mode voltage to minimize errors in inverting applications such as I-to-V converters. The noninverting input current is not trimmed and has a wider variation and therefore a larger maximum value. As the input offset current can be greater than either input current, the use of balanced source resistance is NOT recommended as it actually degrades DC accuracy and also increases noise.

The input bias currents vary with common mode voltage. The cancellation circuitry was not designed to track this common mode voltage because the settling time would have been adversely affected.

The LT1469 inputs can be driven to the negative supply and to within 0.5V of the positive supply without phase reversal. As the input moves closer than 0.5V to the positive supply, the output reverses phase.

Total Input Noise

The total input noise of the LT1469 is optimized for a source resistance between 1k and 20k. Within this range, the total input noise is dominated by the noise of the source resistance itself. When the source resistance is below 1k, voltage noise of the amplifier dominates. When the source resistance is above 20k, the input noise current is the dominant contributor.

Figure 1. Nulling Input Capacitance

Figure 2. Input Stage Protection

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APPLICATIONS INFORMATION

Capacitive Loading

The LT1469 drives capacitive loads of up to 100pF in unity-gain and 300pF in a gain of –1. When there is a need to drive a larger capacitive load, a small series resistor should be inserted between the output and the load. In addition, a capacitor should be added between the output and the inverting input as shown in Figure 3.

Settling Time

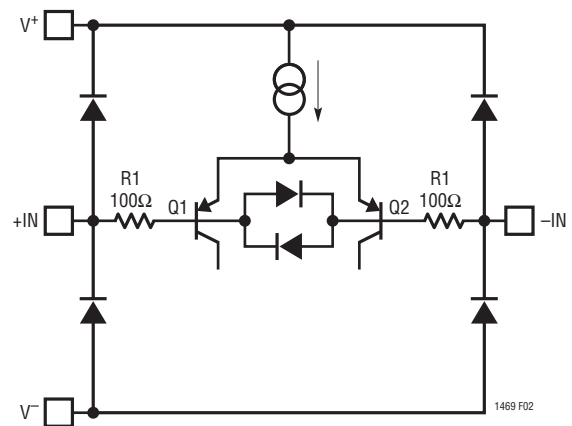The LT1469 is a single stage amplifier with an optimal thermal layout that leads to outstanding settling performance. Measuring settling even at the 12-bit level is very challenging, and at the 16-bit level requires a great deal of subtlety and expertise. Fortunately, there are two excellent Linear Technology reference sources for settling measurements—Application Notes 47 and 74. Appendix B of AN47 is a vital primer on 12-bit settling measurements and AN74 extends the state-of-the-art while concentrating on settling time with a 16-bit current output DAC input.

The settling of the DAC I-to-V converter on the front page was measured using the exact methods of AN74. The optimum nulling of the DAC output capacitance requires 15pF across the 12k feedback resistor. The theoretical limit for 16-bit settling is 11.1 times this RC time constant or 2µs. The actual settling time is 2.4µs at the output of the LT1469.

The RC output noise filter adds a slight settling time delay but reduces the noise bandwidth to 1.6MHz which increases the output resolution for 16-bit accuracy.

$$R_O \geq (1 + R_F/R_G)/(2\pi \bullet C_L \bullet 5\text{MHz})$$
$$R_F \geq 10R_O$$
$$C_F = (2R_O/R_F)C_L$$
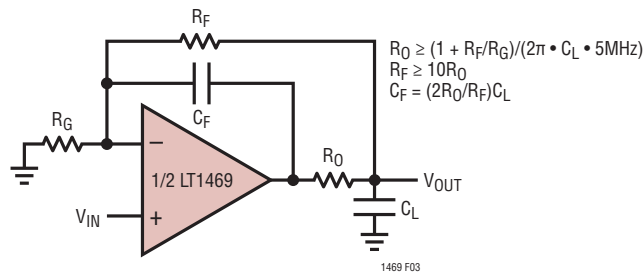
Figure 3. Driving Capacitive Loads

TYPICAL APPLICATIONS

Ultralow Distortion Balanced Audio Line Driver

1/2 LT1364

10k

2.1k

22pF

33.2Ω

+

1/2 LT1469

10k

1k

22pF

30.1Ω

820pF

INPUT

50 FEET SHIELDED
TWISTED PAIR CABLE

600Ω

Z_{IN} = 10kΩ

THD + N
MEASURED HERE

+

1/2 LT1469

20k

22.1k

22pF

30.1Ω

820pF

33.2Ω

V_S = ±15V
GAIN = 6dB

PARALLEL COMPOSITE TOPOLOGY:
LT1364 PROVIDES OUTPUT CURRENT;
LT1469 PRESERVES LINEARITY

+

1/2 LT1364

20k

24.3k

22pF
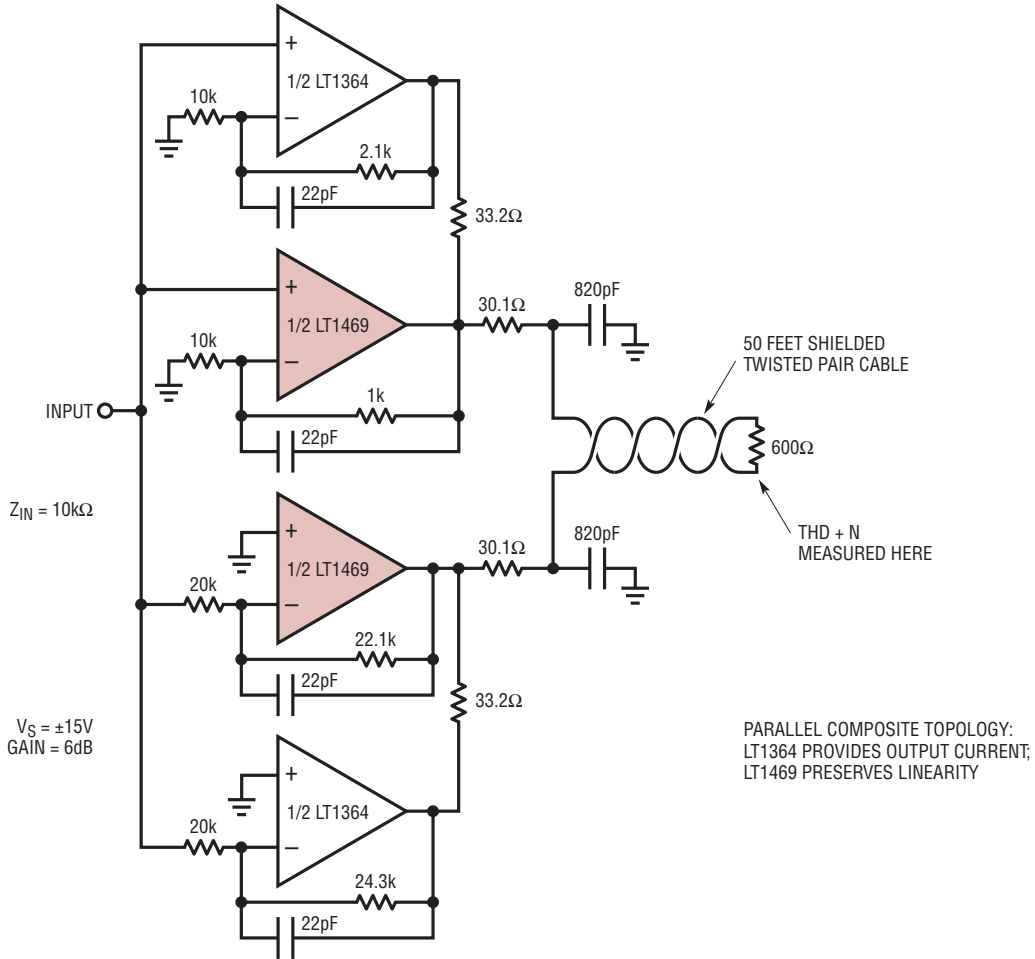
TOTAL HARMONIC DISTORTION + NOISE	V_{OUT}	FREQUENCY	MEASUREMENT BANDWIDTH
0.00025%	10V_{RMS}	1kHz	22kHz
0.0008%	10V_{RMS}	20Hz TO 20kHz	80kHz
0.0006%	26dBu	1kHz	22kHz

*1dBu = 1 milliwatt into 600Ω

1469 TA02

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TYPICAL APPLICATIONS

Extending 16-Bit DAC Performance to 200V Output Swing

$V_{OUT} = 200V_{P-P}$
$I_{OUT} = 25mA$
THD + N = –90dB at 100Hz

16 BITS — LTC1597

R_{FB}
100pF
1/2 LT1469

R_{SELECT}***
TYPICAL
6Ω

19.994k**

10k
330pF
15V
1/2 LT1469
–15V

1μF   125V
510Ω   330Ω
Q1 2N5415
Q3 2N3440*
50k   1M
Q5 2N2222   1k
1N4148   27Ω
1N4148   27Ω
50k   1M
Q6 2N2907   1k
Q3 2N5415*
Q2 2N3440
510Ω   330Ω
1μF   –125V

OUTPUT

*HEAT SINK
**VISHAY S102 RESISTOR 0.01%
***1% METAL FILM RESISTOR

NOTE: FOR FURTHER EXPLANATION,
REFER TO APPLICATION NOTE 74, APPENDIX H

50k**   50k**   50k**   50k**
15pF

1469 TA03

SIMPLIFIED SCHEMATIC

1469 SS

PACKAGE DESCRIPTION

DF Package
12-Lead Plastic DFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1773 Rev Ø)

2.50 REF

0.70 ±0.05

4.50 ± 0.05

3.38 ±0.05
2.65 ± 0.05

3.10 ± 0.05

PACKAGE OUTLINE

0.25 ±0.05
0.50 BSC

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
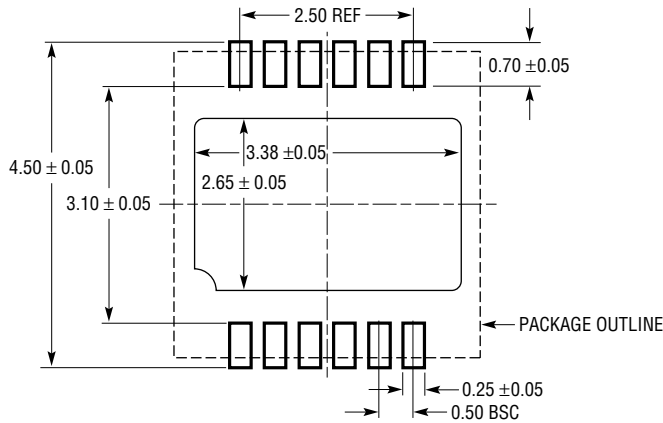APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

4.00 ± 0.10
(4 SIDES)

PIN 1
TOP MARK
(NOTE 6)

2.50 REF

7   12

0.40 ± 0.10

3.38 ±0.10
2.65 ± 0.10

PIN 1 NOTCH
R = 0.20 TYP OR
0.35 × 45°
CHAMFER
(DF12) DFN 0806 REV Ø

6
R = 0.115
TYP

0.25 ± 0.05
0.50 BSC

1

BOTTOM VIEW—EXPOSED PAD

0.200 REF

0.75 ± 0.05

0.00 – 0.05
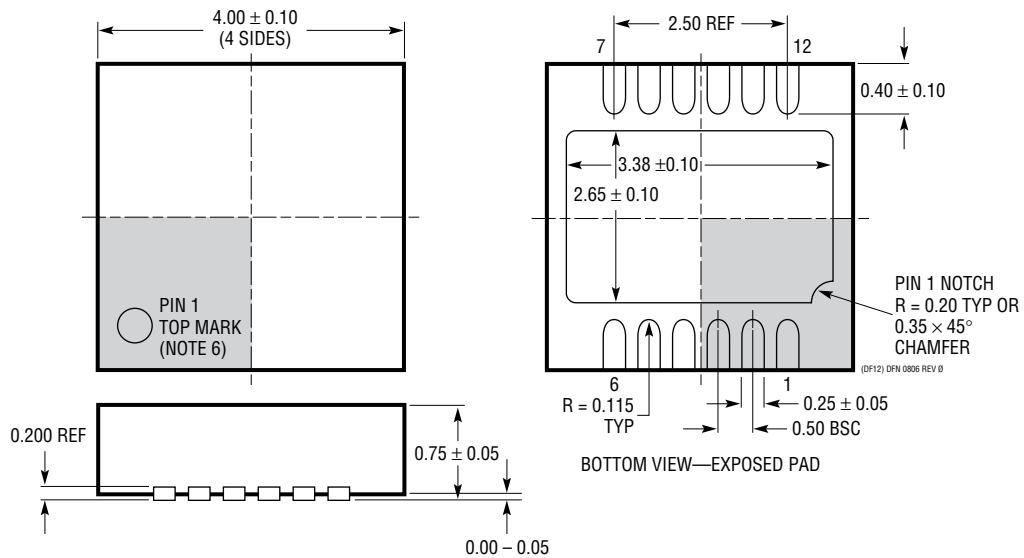
NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220
   VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
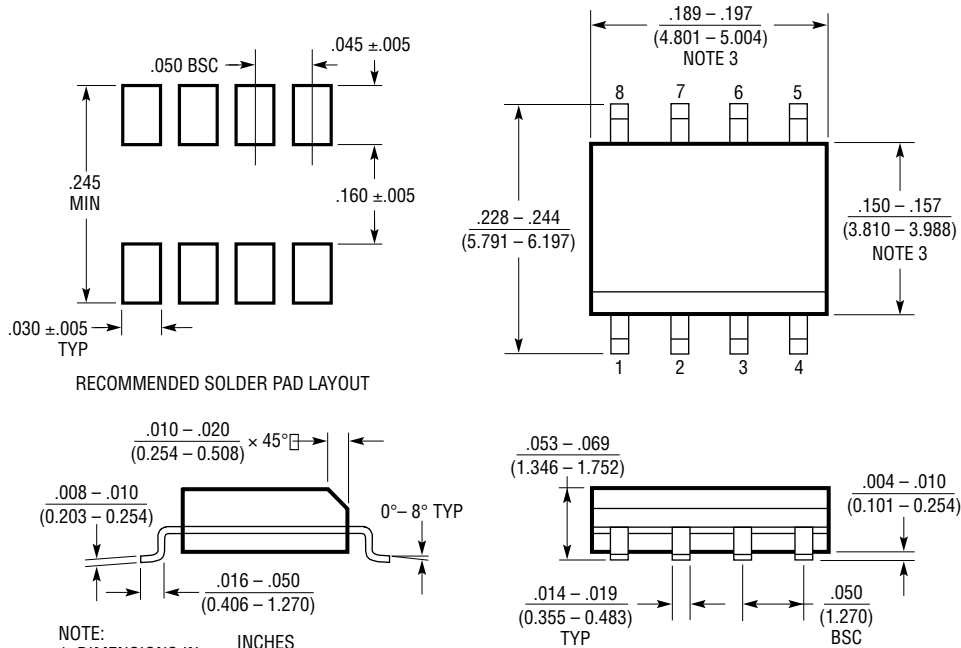   ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow 0.300)
(Reference LTC DWG # 05-08-1510)
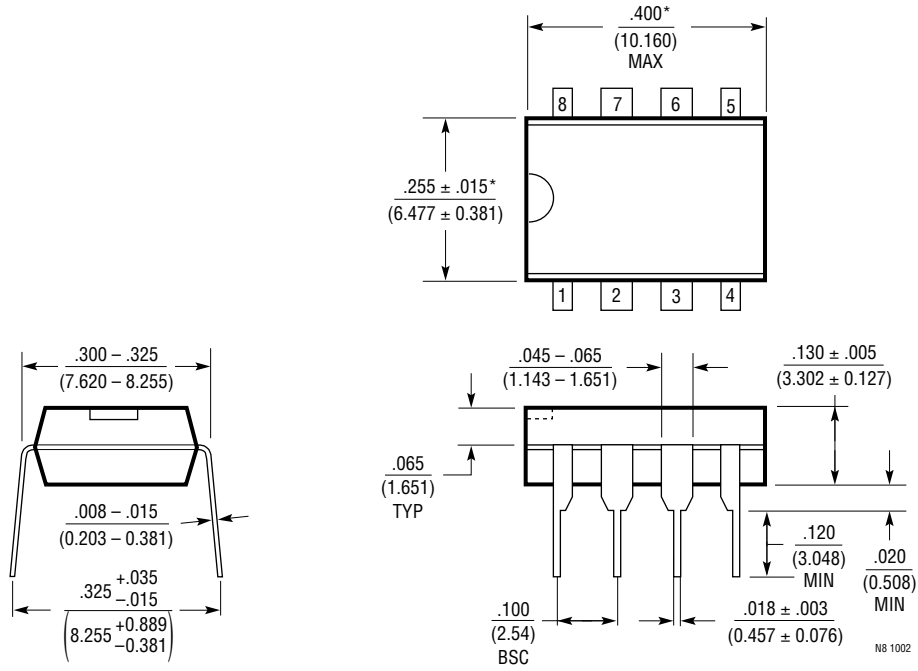
NOTE:
1. DIMENSIONS ARE $\frac{INCHES}{MILLIMETERS}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

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LINEAR
TECHNOLOGY

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(Reference LTC DWG # 05-08-1610)

.050 BSC

.045 ±.005

.245
MIN

.160 ±.005

.030 ±.005
TYP

RECOMMENDED SOLDER PAD LAYOUT

.189 – .197
(4.801 – 5.004)
NOTE 3

8   7   6   5

.228 – .244
(5.791 – 6.197)

.150 – .157
(3.810 – 3.988)
NOTE 3

1   2   3   4

.010 – .020
(0.254 – 0.508) × 45°

.008 – .010
(0.203 – 0.254)

0°– 8° TYP

.016 – .050
(0.406 – 1.270)

.053 – .069
(1.346 – 1.752)

.004 – .010
(0.101 – 0.254)
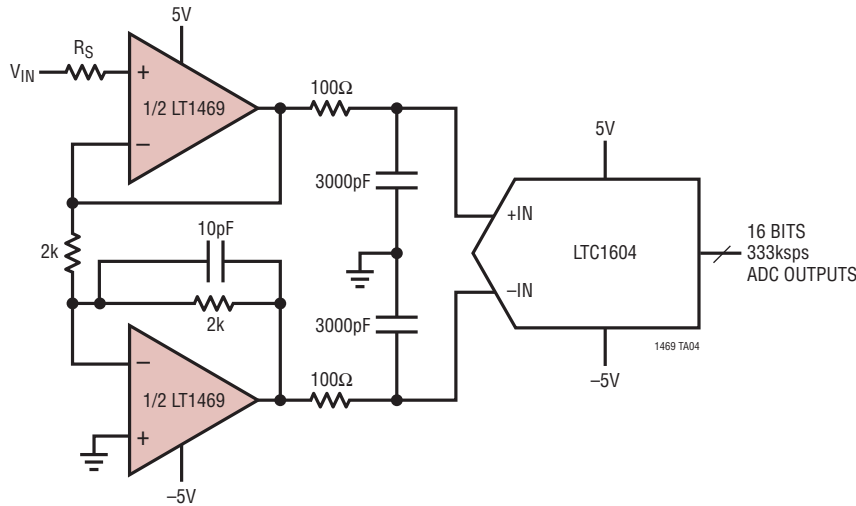
.014 – .019
(0.355 – 0.483)
TYP

.050
(1.270)
BSC

NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$

2. DRAWING NOT TO SCALE

3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
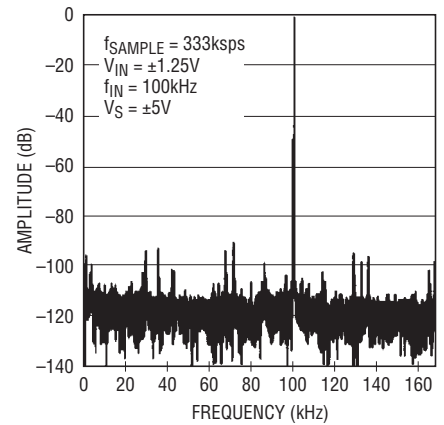   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

1469fa

TYPICAL APPLICATION

16-Bit Accurate Single Ended to Differential ADC Buffer

4096 Point FFT of ADC Output

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1167	Precision Instrumentation Amplifier	Single Resistor Gain Set, 0.04% Max Gain Error, 10ppm Max Gain Nonlinearity
LT1468	Single 90MHz, 22V/µs, 16-Bit Accurate Op Amp	75µV $V_{OS(MAX)}$, Single Version of LT1469
LT1468-2	Single 200MHz, 30V/µs, 16-Bit Accurate $A_V \geq 2$ Op Amp	75µV $V_{OS(MAX)}$
LT1469-2	Dual 200MHz, 30V/µs, 16-Bit Accurate $A_V \geq 2$ Op Amp	75µV $V_{OS(MAX)}$
LTC1595/LTC1596	16-Bit Serial Multiplying I_{OUT} DAC	±1LSB Max INL/DNL, Low Glitch, DAC8043 16-Bit Upgrade
LTC1597	16-Bit Parallel Multiplying I_{OUT} DAC	±1LSB Max INL/DNL, Low Glitch, On-Chip Bipolar Resistors
LTC1604	16-Bit, 333ksps Sampling ADC	±2.5V Input, SINAD = 90dB, THD = –100dB
LTC1605	Single 5V, 16-Bit, 100ksps Sampling ADC	Low Power, ±10V Inputs, Parallel/Byte Interface
LT1723	Dual 200MHz, 70V/µs Low Noise Precision Op Amp	$V_S \leq \pm 5V$, e_n = 3.8nV/$\sqrt{Hz}$, –85dBc at 1MHz
LT1801	Dual 80MHz, 25V/µs Low Power Rail-to-Rail Precision Op Amp	$V_S \leq \pm 5V$, I_{CC} = 1.6mA, $V_{OS} \leq 350$µV
LT6221	Dual 60MHz, 20V/µs Low Power Rail-to-Rail Precision Op Amp	$V_S \leq \pm 5V$, I_{CC} = 0.9mA, $V_{OS} \leq 350$µV
LTC6244HV	Dual 50MHz, Low Noise, Precision CMOS Op Amp	$V_S \leq \pm 5V$, $V_{OS} \leq 100$µV, $I_B \leq 75$pA