ICmic
IC MICROSYSTEMS

12/10/8-Bit Low Power Single DAC With Serial Interface and Voltage Output

FEATURES

- 12/10/8-Bit Single DAC in 08 Lead MSOP Package
- Ultra-Low Power Consumption
- Guaranteed Monotonic
- Wide Voltage Output Swing Buffer
- Three-wire SPI/QSP and Microwire Interface Compatible
- Three Software-Selectable Power-Down Output Impedances (1 K Ohm, 100 K Ohm and Hi-Z)
- Schmitt-Triggered Inputs for Direct Interfacing to Opto-couplers

APPLICATION

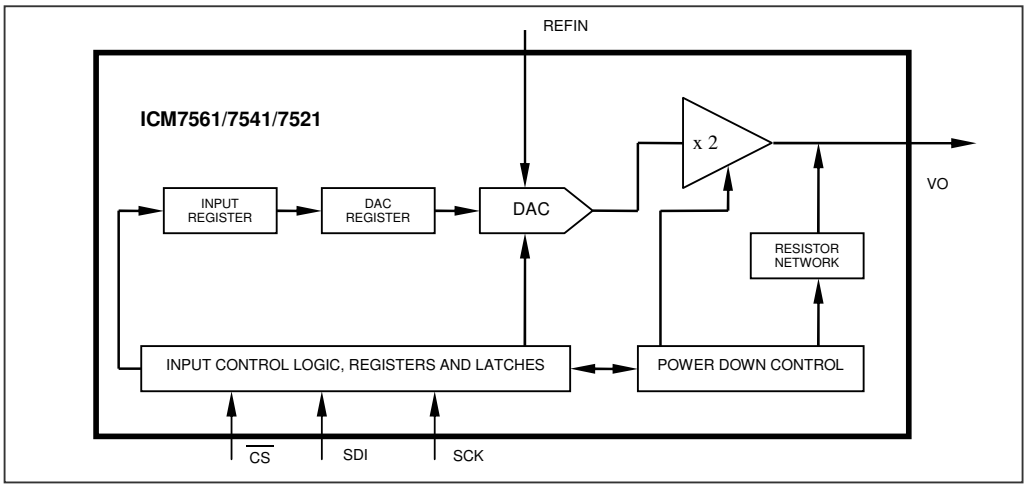
- Battery-Powered Applications
- Industrial Process Control
- Digital Gain and Offset Adjustment

OVERVIEW

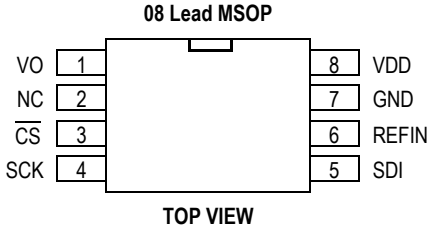
The ICM7561, ICM7541 and ICM7521 are 12-Bit, 10-Bit and 8-Bit Voltage Output, Low Power, Single DACs respectively, with guaranteed monotonic behavior. These DACs are available in 8 Lead MSOP package. They have three Software-Selectable Power-Down Output Impedances (1 K Ohm, 100 K Ohm and Hi-Z) as additional safety feature for applications that drive transducers or valves. The operating supply range is 2.7V to 5.5V.

The input interface is an easy to use three-wire SPI, QSPI and Microwire compatible interface. The DAC has Schmitt-Triggered Inputs for Direct Interfacing to Opto-couplers easily.

BLOCK DIAGRAM



PACKAGE



PIN DESCRIPTION (8 Lead MSOP)

Pin	Name	I/O	Description
1	VO	O	DAC Output Voltage
2	NC	-	No Connection
3	$\overline{CS}$	I	Active Low Chip Select (CMOS)
4	SCK	I	Serial Clock Input (CMOS)
5	SDI	I	Serial Data Input (CMOS)
6	REFIN	I	Reference Voltage Input
7	GND	I	Ground
8	VDD	I	Supply Voltage

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
I_{IN}	Input Current	+/- 25.0	mA
$V_{IN\_}$	Digital Input Voltage (SCK, SDI , $\overline{CLR}$, $\overline{CS}$)	-0.3 to 7.0	V
V_{IN_REF}	Reference Input Voltage	-0.3 to 7.0	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_{SOL}	Soldering Temperature	300	°C

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ORDERING INFORMATION

Part	Operating Temperature Range	Package
ICM7561	-40 °C to 85 °C	08-Lead MSOP
ICM7541	-40 °C to 85 °C	08-Lead MSOP
ICM7521	-40 °C to 85 °C	08-Lead MSOP

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
ICM7561						
N	Resolution		12			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.4	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		4.0	±12.0	LSB
ICM7541						
N	Resolution		10			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.1	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		1.0	±3.0	LSB
ICM7521						
N	Resolution		8			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.05	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		0.25	±0.75	LSB
STATIC ACCURACY						
GE	Gain Error				±0.5	% of FS
OE	Offset Error				±25	mV
POWER REQUIREMENTS						
V_{DD}	Supply Voltage		2.7	5	5.5	V
I_{DD}	Supply Current	Full Scale at VDD=5.5		90	150	µA
		Full Scale at VDD=3.6		75	100	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Vout	Output Voltage Range	(Note 3)	0		V_{DD}	V
VO_{SC}	Short Circuit Current			60	150	mA
Rout	Output Impedance	Power-Down at 1 K Ohm	0.9	1	1.1	KΩ
		Power-Down at 100 K Ohm	90	100	110	KΩ
	Output Line Regulation	V_{DD}=2.7V to 5.5V	-3.0	0.4	3.0	mV/V
LOGIC INPUTS						
V_{IH}	Digital Input High	(Note 2)	2.4			V
V_{IL}	Digital Input Low	(Note 2)			0.8	V
	Digital Input Leakage				5	

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SR	Slew Rate			2		V/µs
	Settling Time			8		µs
	Mid-scale Transition Glitch Energy			40		nV-S

Note 1: Linearity is defined from code 110 to 3990 (ICM7561)
Linearity is defined from code 16 to 1023 (ICM7541)
Linearity is defined from code 4 to 255 (ICM7521)
Note 2: Guaranteed by design; not tested in production
Note 3: See Applications Information

TIMING CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_1	SCK Cycle Time	(Note 2)	30			ns
t_2	Data Setup Time	(Note 2)	10			ns
t_3	Data Hold Time	(Note 2)	10			ns
t_4	SCK Falling edge to $\overline{CS}$ Rising	(Note 2)	0			ns
t_5	$\overline{CS}$ Falling Edge to SCK Rising Edge	(Note 2)	15			ns
t_6	$\overline{CS}$ Pulse Width	(Note 2)	20			ns

SERIAL INTERFACE TIMING AND OPERATION DIAGRAM

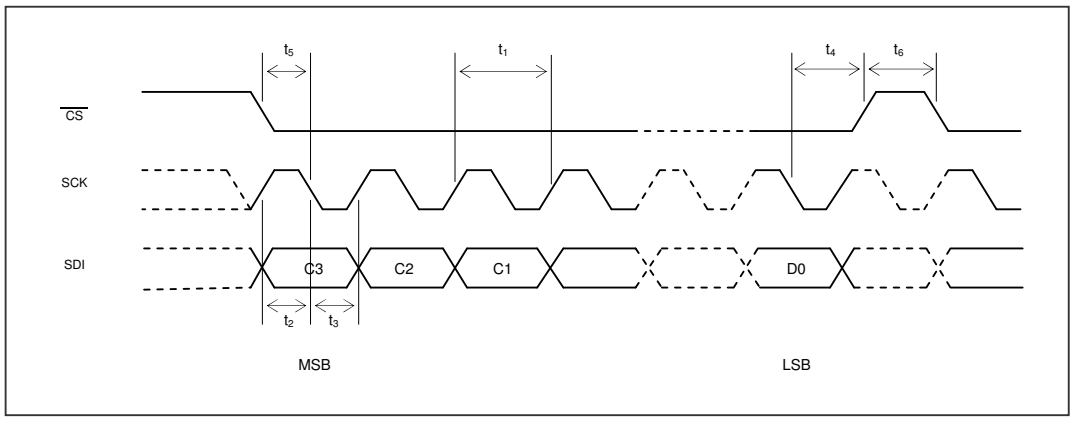


Figure 1. Serial Interface Timing Diagram

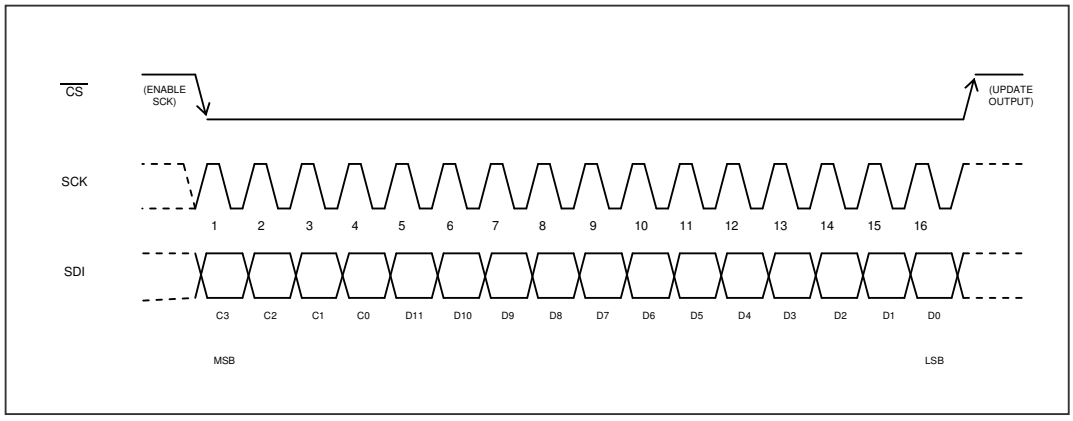


Figure 2. Serial Interface Operation Diagram

CONTENTS OF INPUT SHIFT REGISTER

DEVICE	BIT	CONTROL WORD				DATA WORD											
		MSB															LSB
ICM7561	12	C3	C2	C1	C0	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ICM7541	10	C3	C2	C1	C0	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	A1	A0
ICM7521	8	C3	C2	C1	C0	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	X	X	A1	A0

Figure 3. Contents of Input Shift Register

C3	C2	C1	C0	DATA (D11~D0:7561;D9~D0:7541;D7~D0:7521)	FUNCTION
0	0	0	0	Data	Input loaded into DAC, VO updated

Table 1. Serial Interface Input Word

CONTROL				DATA			FUNCTION
C3	C2	C1	C0	D11~D2 D9~D0 D7~D0	D1 A1 A1	D0 (7561) A0 (7541) A0 (7521)	
1	1	1	1	X	0	0	DAC O/P, wakeup
1	1	1	1	X	0	1	Floating Output
1	1	1	1	X	1	0	Output is terminated with 1KΩ
1	1	1	1	X	1	1	Output is terminated with100 KΩ

Table 2. Power Down Mode Control

DETAILED DESCRIPTION

The ICM7561 is a 12-bit voltage output DAC. The ICM7541 is the 10-bit version of this family and the ICM7521 is the 8-bit version. These devices have a 16-bit input shift register and the DAC has a double buffered digital input.

This family of DACs has a guaranteed monotonic behavior. The operating supply range is from 2.7V to 5.5V.

Reference Input

The reference input accepts positive DC and AC signals. The voltage at REFIN sets the full-scale output voltage of the DAC. The reference input voltage range is from 0 to VDD-1.5V. The impedance at this pin is very high (greater than 10 M Ohm). The DAC output amplifier is configured in a gain of 2 configuration. This means that the full-scale output of the DAC will be 2x V_{REF}. To determine the output voltage for any code, use the following equation.

$$V_{OUT} = 2 \times (V_{REF} \times (D / (2^n)))$$

Where D is the numeric value of DAC's decimal input code, V_{REF} is the reference voltage and n is number of bits, i.e. 12 for ICM7561, 10 for ICM7541 and 8 for ICM7521.

Output Buffer Amplifier

The DAC has an output amplifier connected in a gain of 2 configuration. This amplifier has a wide output voltage swing. The actual swing of the output amplifier will be limited by offset error and gain error. See the Applications Information Section for a more detailed discussion.

The output amplifier can drive a load of 2.0 K Ω to V_{DD} or GND in parallel with a 500 pF load capacitance.

The output amplifier has a full-scale typical settling time of 8 µs and it dissipates about 100 µA with a 3V supply voltage.

Serial Interface and Input Logic

This DAC family uses a standard 3-wire connection compatible with SPI/QSPI and Microwire interfaces. Data is always loaded in 16-bit words which consist of 4 control bits (MSBs) followed by 12 bits (see Figure 3). The ICM7561 uses the last two LSBs of the DAC data also for power down control. The ICM7541 and ICM7521 have the last 2 LSBs as power down control bits only and the data which gets loaded into the DAC register starts at location D0 (see tables 1 and 2).

Serial Data Input

SDI (Serial Data Input) pin is the data input pin for the DAC. Data is clocked in on the falling edge of SCK which has a schmitt trigger internally to allow for noise immunity on the SCK pin. This specially eases the use for opto-coupled interfaces.

The Chip Select pin which is the 3rd pin of 8 Lead MSOP package is active low. This pin frames the input data for synchronous loading and must be low when data is being clocked into the part. There is an onboard counter on the clock input and after the 16th clock pulse the data is automatically transferred to a 16-bit input latch and the 4 bit control word (C3~C0) is then decoded and the appropriate command is performed depending on the control word (see Table 1, 2). Chip Select pin must be pulled high (level-triggered) and back low for the next data word to be loaded in. This pin also disables the SCK pin internally when pulled high.

Power-Down Mode

The DACs have three Software-Selectable Power-Down Output Impedances (1 K Ohm, 100 K Ohm and Hi-Z) as additional safety feature for applications that drive transducers or valves. The power down (or wake up command) can be done by loading the control word with 1111 (C3 to C0). In power down mode, the selection of the output impedance of the DAC is controlled by the last two bits (D0 and D1 for the ICM7561, or A0 and A1 for the ICM7541/7521). See Table 1 and Table 2 for details of operation of this function.

Power-On Reset

There is a power-on reset on board that will clear the contents of all the latches to all 0s on power-up and the DAC voltage output will go to ground.

APPLICATIONS INFORMATION

Power Supply Bypassing and Layout Considerations

As in any precision circuit, careful consideration has to be given to layout of the supply and ground. The return path from the GND to the supply ground should be short with low impedance. Using a ground plane would be ideal. The supply should have some bypassing on it. A 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic with a low ESR can be used. Ideally these would be placed as close as possible to the device. Avoid crossing digital and analog signals, specially the reference, or running them close to each other.

Output Swing Limitations

The ideal rail-to-rail DAC would swing from GND to V_{DD}. However, offset and gain error limit this ability. Figure 4 illustrates how a negative offset error will affect the output. The output will limit close to ground since this is single supply part, resulting in a dead-band area. As a larger input is loaded into the DAC the output will eventually rise above ground. This is why the linearity is specified for a starting code greater than zero.

Figure 5 illustrates how a gain error or positive offset error will affect the output when it is close to V_{DD}. A positive gain error or positive offset will cause the output to be limited to the positive supply voltage resulting in a dead-band of codes close to full-scale.

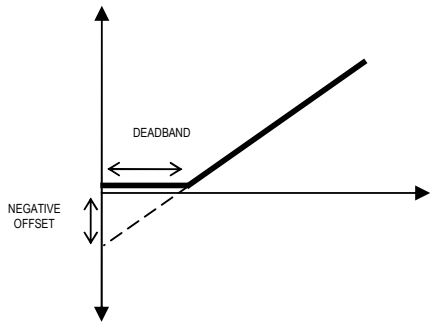


Figure 4. Effect of Negative Offset

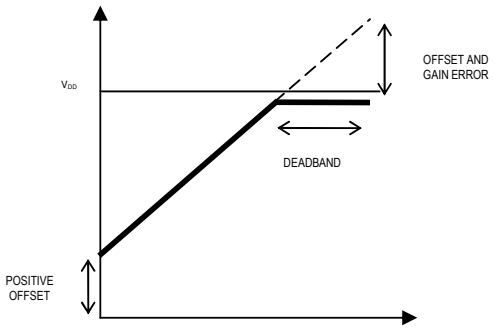
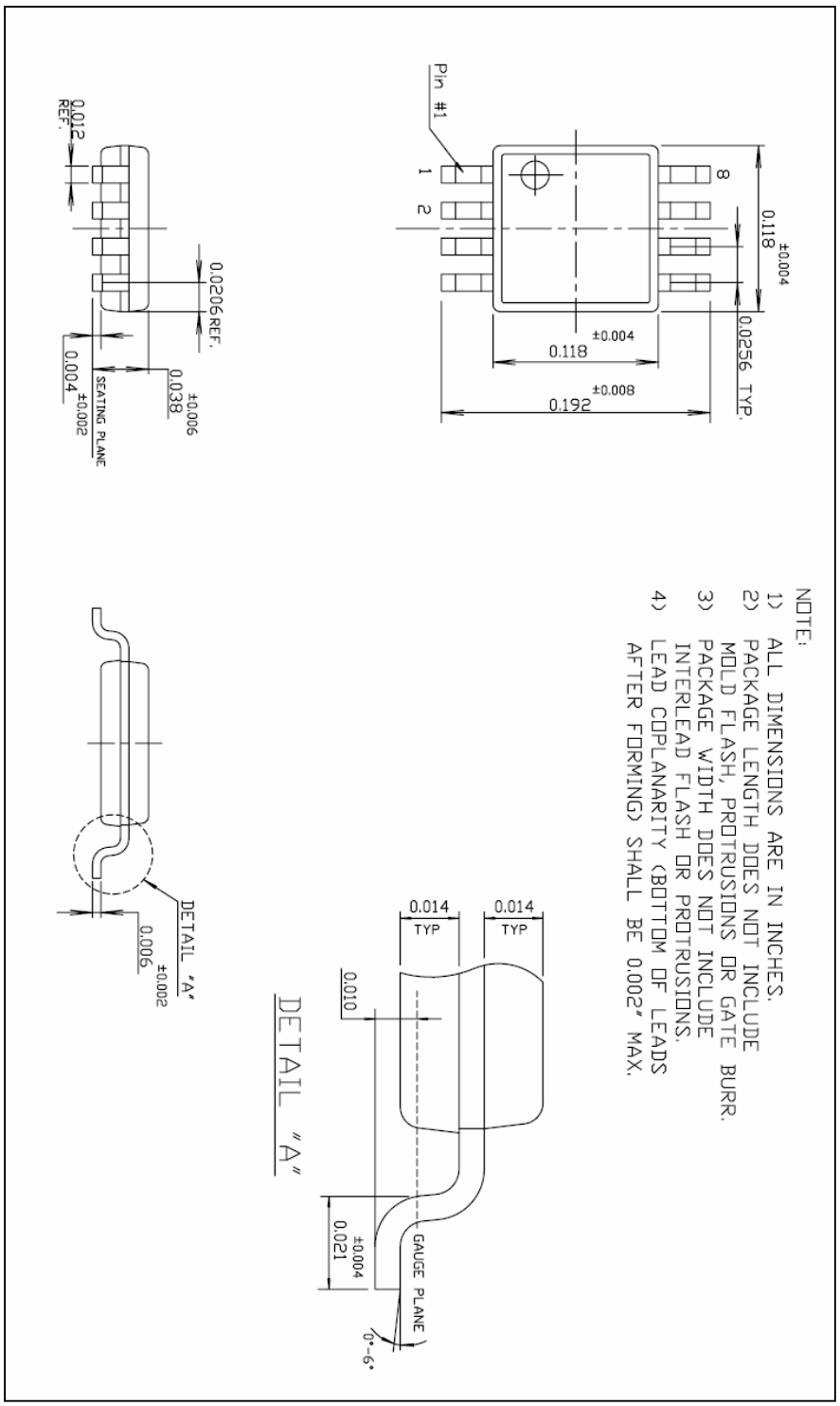


Figure 5. Effect of Gain Error and Positive Offset

PACKAGE INFORMATION

8 Lead MSOP



PACKAGE INFORMATION