ICM7361/7341/7321

SINGLE 12/10/8-BIT VOLTAGE-OUTPUT DACS

FEATURES

- 12/10/8-Bit Monotonic DACs in 6 lead SOT-23 Package
- Wide Output Voltage Swing
- Micro-Power
- On Board 1.25V Reference
- Serial Interface with three-wire SPI/QSPI and Microwire Interface Compatible
- 8µs Full-Scale Settling Time

APPLICATIONS

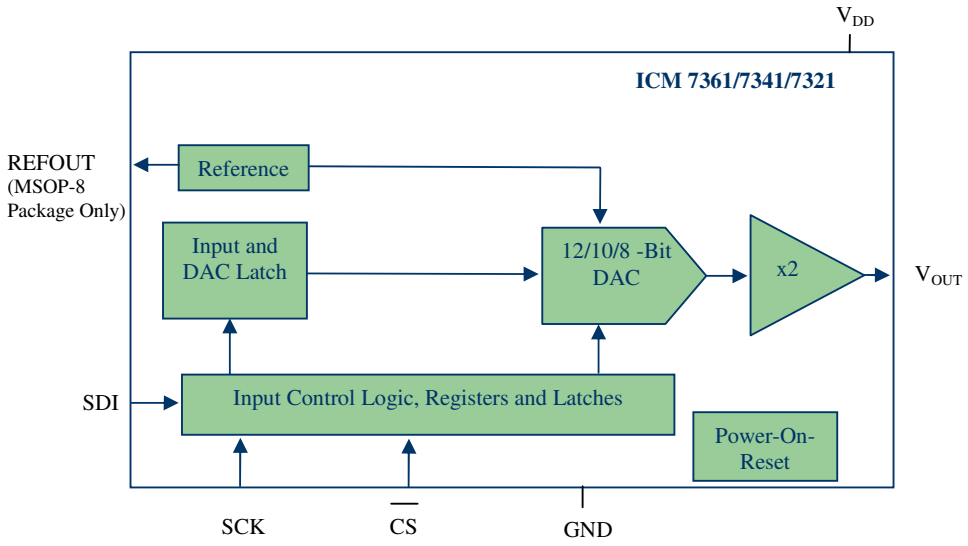
- Battery-Powered Applications
- Industrial Process Control
- Digital Gain and Offset Adjustment

OVERVIEW

The ICM7361, ICM7341 and ICM7321 are 12-Bit, 10-Bit and 8-Bit wide output voltage swing DACs respectively, with guaranteed monotonic behavior. These DACs are available in both a tiny 6-pin SOT-23 package and an 8-pin MSOP package. They include a 1.25V reference for ease of use and flexibility. The reference output is available on a separate pin, in the 8-pin package version, and can be used to drive external loads. The operating supply range is 2.7V to 5.5V.

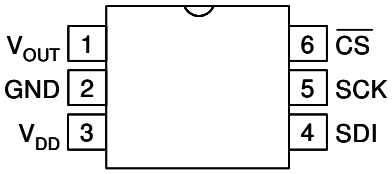
The input interface is an easy to use three-wire SPI/QSPI compatible interface. The DAC has a double buffered digital input.

BLOCK DIAGRAM

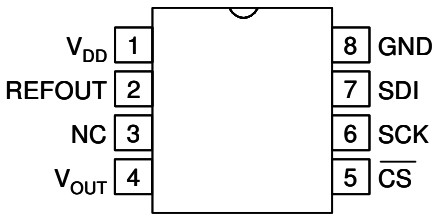


PACKAGE

SOT-23



8-Pin MSOP



PIN DESCRIPTION (MSOP-8 Package)

Pin No	Symbol	Description
1	V_{DD}	**Supply Voltage**
2	REFOUT	**Reference Output (1.25V)**
3	NC	**No Connect**
4	V_{OUT}	**DAC Output**
5	$\overline{CS}$	**Chip Select (TTL or CMOS)**
6	SCK	**Serial Clock Input (TTL or CMOS)**
7	SDI	**Serial Data Input (TTL or CMOS)**
8	GND	**Ground**

PIN DESCRIPTION (SOT-23 Package)

Pin No	Symbol	Description
1	V_{OUT}	**DAC Output**
2	GND	**Ground**
3	V_{DD}	**Supply Voltage**
4	SDI	**Serial Data Input (TTL or CMOS)**
5	SCK	**Serial Clock Input (TTL or CMOS)**
6	$\overline{CS}$	**Chip Select (TTL or CMOS)**

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
I_{IN}	Input Current	+/- 25.0	mA
$V_{IN\_}$	Digital Input Voltage (SCK, SDI, $\overline{CS}$)	-0.3 to 7.0	V
V_{IN_REF}	Reference Input Voltage	-0.3 to 7.0	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_{SOL}	Soldering Temperature	300	°C

Note: Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ORDERING INFORMATION

Part	Temperature Range	Package
ICM7361M	-40 °C to 85 °C	8-Pin MSOP
ICM7341M	-40 °C to 85 °C	8-Pin MSOP
ICM7321M	-40 °C to 85 °C	8-Pin MSOP

ORDERING INFORMATION

Part	Temperature Range	Package
ICM7361T	-40 °C to 85 °C	SOT-23
ICM7341T	-40 °C to 85 °C	SOT-23
ICM7321T	-40 °C to 85 °C	SOT-23

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V ; V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
ICM7361						
N	Resolution		12			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.4	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		4.0	±12.0	LSB
ICM7341						
N	Resolution		10			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.1	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		1.0	±3.0	LSB
ICM7321						
N	Resolution		8			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.05	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		0.25	±0.75	LSB
GE	Gain Error				±0.5	% of FS
OE	Offset Error				±25	mV
POWER REQUIREMENTS						
V_{DD}	Supply Voltage		2.7		5.5	V
I_{DD}	Supply Current	(Note 4)		0.2	0.5	mA

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
	Output Voltage Range	(Note 3)	0		V_{DD}	V
VO_{SC}	Short Circuit Current			60	150	mA
R_{OUT}	Amp Output Impedance	At Mid-scale (Note 2) At 0-scale (Note 2)		1.0 100	5.0 200	Ω Ω
	Output Line Regulation	V_{DD} =2.7 to 5.5 V		0.4	3.0	mV/V
LOGIC INPUTS						
V_{IH}	Digital Input High	(Note 2)	2.4			V
V_{IL}	Digital Input Low	(Note 2)			0.8	V
	Digital Input Leakage				5	μA

REFERENCE						
V_{REFOUT}	Reference Output		1.2	1.25	1.3	V
	Reference Output Line Regulation	V_{DD} =2.7 to 5.5 V		0.8	4.0	mV/V

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V; V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SR	Slew Rate			2		V/µs
	Settling Time	Full-scale settling		8		µs
	Mid-scale Transition Glitch Energy			40		nV-S

Note 1: Linearity is defined from code 64 to 4095 (ICM7361)
Linearity is defined from code 16 to 1023 (ICM7341)
Linearity is defined from code 4 to 255 (ICM7321)
Note 2: Guaranteed by design; not tested in production
Note 3: See Applications Information
Note 4: All digital inputs are either at GND or V_{DD}

TIMING CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_1	SCK Cycle Time	(Note 2)	30			ns
t_2	Data Setup Time	(Note 2)	10			ns
t_3	Data Hold Time	(Note 2)	10			ns
t_4	SCK Falling edge to $\overline{CS}$ Rising Edge	(Note 2)	0			ns
t_5	$\overline{CS}$ Falling Edge to SCK Rising Edge	(Note 2)	15			ns
t_6	$\overline{CS}$ Pulse Width	(Note 2)	20			ns

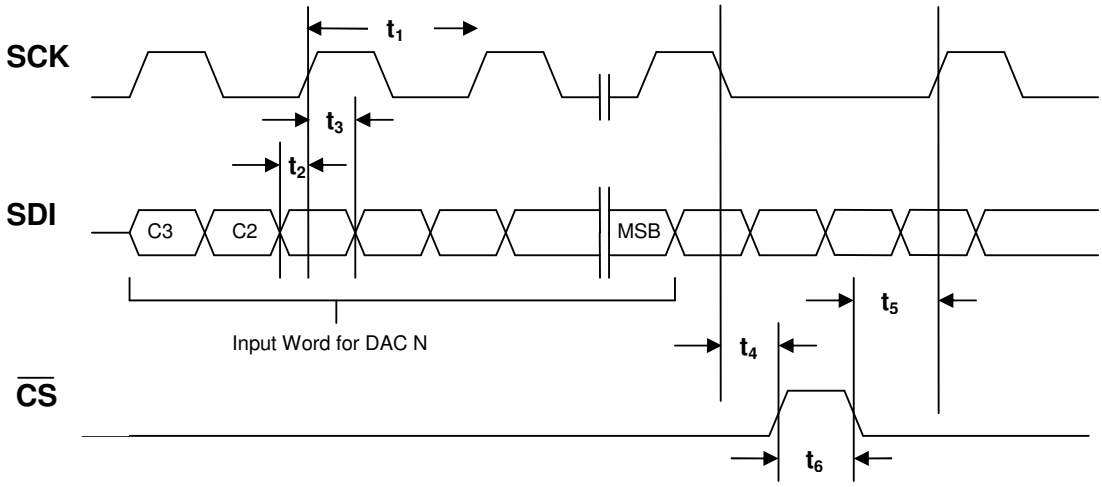


Figure 1: Serial Interface Timing Diagram

CONTENTS OF INPUT SHIFT REGISTER

ICM7361 (12-Bit DAC)

MSB															LSB
C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 2: Contents of ICM7361 Input Shift Register

ICM7341 (10-Bit DAC)

MSB															LSB
C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X

Figure 3: Contents of ICM7341 Input Shift Register

ICM7321 (8-Bit DAC)

MSB															LSB
C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

Figure 4: Contents of ICM7321 Input Shift Register

C3	C2	C1	C0	DATA	FUNCTION
0	0	0	0	Data	Load Input Latch
0	0	0	1	Data	Update DAC
0	0	1	0	Data	Load Input Latch and Update DAC
0	0	1	1	X	No Operation
0	1	0	0	X	No Operation
0	1	0	1	X	No Operation
0	1	1	0	X	No Operation
0	1	1	1	X	No Operation
1	0	0	0	X	No Operation
1	0	0	1	X	No Operation
1	0	1	0	X	No Operation
1	0	1	1	X	No Operation
1	1	0	0	X	No Operation
1	1	0	1	X	No Operation
1	1	1	0	X	No Operation
1	1	1	1	X	No Operation

Table 1: Serial Interface Control Command

DETAILED DESCRIPTION

The ICM7361 is a 12-bit voltage output DAC. The ICM7341 is the 10-bit version of this family and the ICM7321 is the 8-bit version.

This family of DACs has guaranteed monotonic behavior. There is a 1.25V onboard reference and an operating supply range of 2.7V to 5.5V.

Reference Output

There is an internal bandgap reference of 1.25V on these parts and there is a gain of two in the output amplifiers which means they swing from ground at code 0 to 2.5V at full-scale :

$$Vout = 2 \times (1.25 \times D)/2^n$$

Where D=digital input (decimal) and n= number of bits, i.e. 12 for ICM7361, 10 for ICM7341 and 8 for ICM7321.

The reference output is nominally 1.25V and is brought out to a separate pin, REFOUT (8-pin MSOP package only) and can be used to drive external loads. However, it is still internally connected to the DAC reference input. The outputs will nominally swing from 0 to 2.5V.

Output Amplifier

The DAC has an output amplifier with a wide output voltage swing. The actual swing of the output amplifier will be limited by offset error and gain error. See the Applications Information Section for a more detailed discussion.

The amplifier is configured in a gain of 2 with internal gain resistors of about 50 kΩ. The output swing will be from 0V to 2.5V at full-scale.

The output amplifier can drive a load of 2.0 kΩ to V_{DD} or GND in parallel with a 500 pF load capacitance.

The output amplifier has a full-scale typical settling time of 8 µs and it dissipates about 100 µA with a 3V supply voltage.

Serial Interface and Input Logic

This DAC family uses a standard 3-wire connection compatible with SPI/QSPI interfaces. Data is loaded in 16-bit words which consist of 4 address and control bits (MSBs) followed by 12 bits of data (see table 1). The ICM7341 has the last two LSBs as don't cares and the ICM7321 has the last 4 LSBs as don't cares. The DAC is double buffered with an input latch and a DAC latch.

All the digital inputs are CMOS/TTL compatible. The current dissipation of the device however, will be higher when the inputs are driven at TTL levels.

Data is clocked in on the rising edge of SCK which has a Schmitt trigger internally to allow for noise immunity on the SCK pin. This specially eases the use for opto-coupled interfaces.

The $\overline{CS}$ pin must be low when data is being clocked into the part. After the 16th clock pulse the $\overline{CS}$ pin must be pulled high (level-triggered) for the data to be transferred to an input bank of latches. The $\overline{CS}$ pin also disables the SCK pin internally when pulled high and the SCK pin must be low before the $\overline{CS}$ pin is pulled back low. As the $\overline{CS}$ pin is pulled high the shift register contents are transferred to a bank of 16 latches. The 4 bit control word (C3~C0) is then decoded and the DAC is updated or loaded depending on the control word (see Table 1).

The DAC has a double-buffered input with an input latch and a DAC latch. The DAC output will swing to its new value when data is loaded into the DAC latch. The user has three options: loading only the input latch, updating the DAC with data previously loaded into the input latch or loading the input latch and updating the DAC at the same time with a new code.

Power-On Reset

There is a power-on reset on board that will clear the contents of all the latches to all 0s on power-up and the DAC voltage output will go to ground.

APPLICATIONS INFORMATION

Power Supply Bypassing and Layout Considerations

As in any precision circuit, careful consideration has to be given to layout of the supply and ground. The return path from the GND to the supply ground should be short with low impedance. Using a ground plane would be ideal. The supply should have some bypassing on it. A 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic with a low ESR can be used. Ideally these would be placed as close as possible to the device. Avoid crossing digital and analog signals, specially the reference, or running them close to each other.

Output Swing Limitations

The ideal rail-to-rail DAC would swing from GND to V_{DD} however, offset and gain error limit this ability. Figure 5 illustrates how a negative offset error will affect the output. The output will limit close to ground since this is single supply part, resulting in a dead-band area. As a larger input is loaded into the DAC the output will eventually rise above ground. This is why the linearity is specified for a starting code greater than zero.

Figure 6 illustrates how a gain error or positive offset error will affect the output when it is close to V_{DD}. A positive gain error or positive offset will cause the output to be limited to the positive supply voltage resulting in a dead-band of codes close to full-scale.

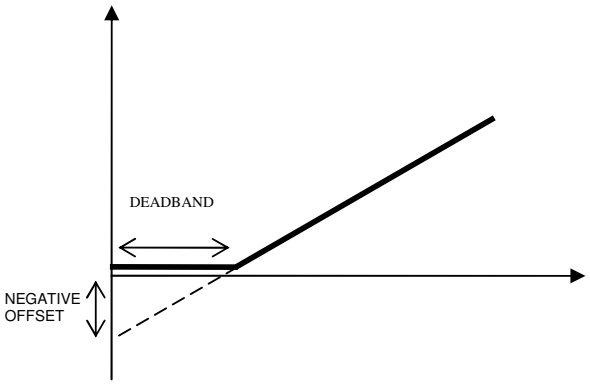


Figure 5: Effect of Negative Offset

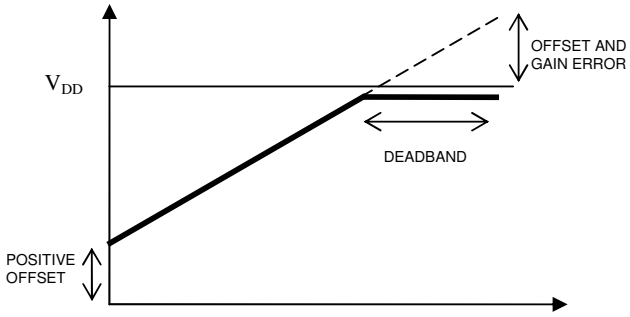
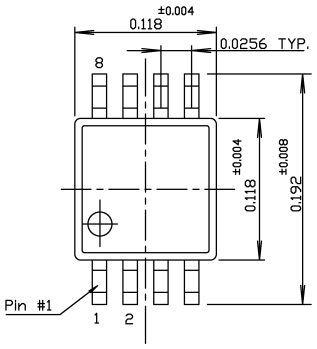


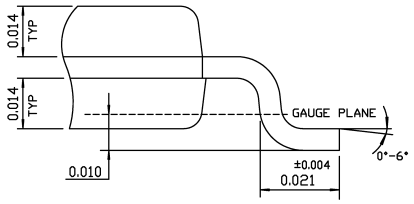
Figure 6: Effect of Gain Error and Positive Offset

PACKAGE INFORMATION

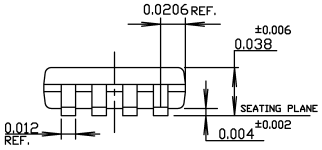
8-Pin MSOP Package

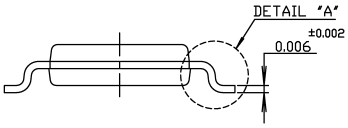


NOTE:
1) ALL DIMENSIONS ARE IN INCHES.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.002" MAX.

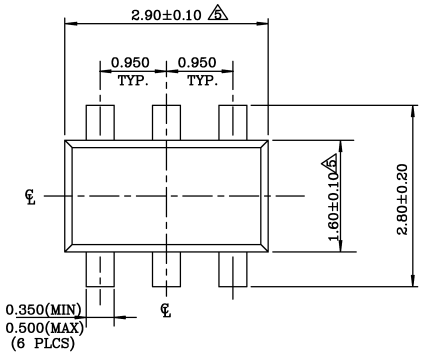


DETAIL "A"

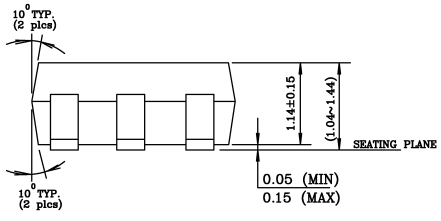


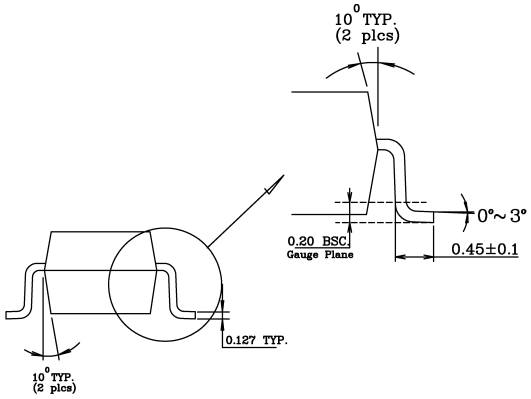


SOT-23 Package



NOTE:
1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
2. Package surface to be mirror finish.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the gauge plane method.
5. Dimensions are exclusive of mold flash and gate burr.





ORDERING INFORMATION