Dual, Matched Picoampere, Microvolt Input, Low Noise Op Amp

FEATURES

- *Guaranteed* Offset Voltage 50μV Max.
- *Guaranteed* Bias Current
  - 25°C 120pA Max.
  - −55°C to 125°C 700pA Max.
- *Guaranteed* Drift 1.5μV/°C Max.
- Low Noise, 0.1Hz to 10Hz 0.5μVp-p
- *Guaranteed* Supply Current 600μA Max.
- *Guaranteed* CMRR 112dB Min.
- *Guaranteed* PSRR 112dB Min.
- *Guaranteed* Voltage Gain with 5mA Load Current
- *Guaranteed* Matching Characteristics

APPLICATIONS

- Strain Gauge Signal Conditioner
- Dual Limit Precision Threshold Detection
- Charge Integrators
- Wide Dynamic Range Logarithmic Amplifiers
- Light Meters
- Low Frequency Active Filters
- Standard Cell Buffers
- Thermocouple Amplifiers

DESCRIPTION

The LT1024 dual, matched internally compensated universal precision operational amplifier can be used in practically all precision applications requiring multiple op amps. The LT1024 combines picoampere bias currents (which are maintained over the full −55°C to 125°C temperature range), microvolt offset voltage (and low drift with time and temperature), low voltage and current noise, and low power dissipation. Extremely high common-mode and power supply rejection ratios, practically immeasurable warm-up drift, and the ability to deliver 5mA load current with a voltage gain of a million round out the LT1024's superb precision specifications.

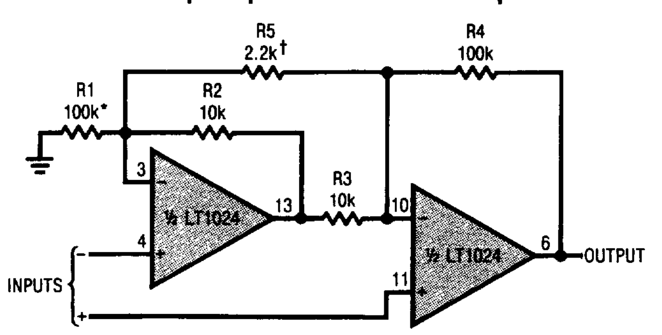
Tight matching is guaranteed on offset voltage, non-inverting bias currents and common-mode and power supply rejections.

The all-around excellence of the LT1024 eliminates the necessity of the time-consuming error analysis procedure of precision system design in many dual applications; the LT1024 can be stocked as the universal dual op amp in the 14-pin DIP configuration.

For a single op amp with similar specifications, see the LT1012 data sheet; for a single supply dual precision op amp in the 8-pin configuration, see the LT1013 data sheet.

2

Two Op Amp Instrumentation Amplifier

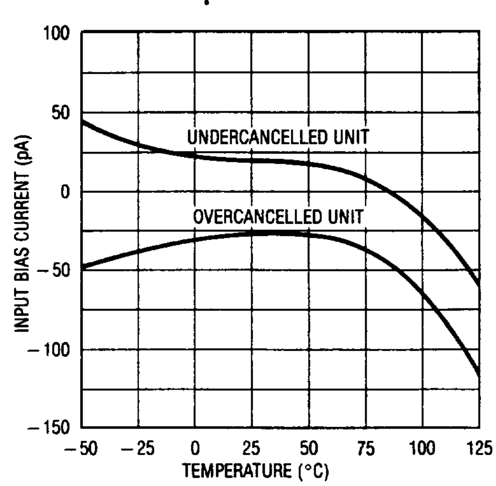


$$GAIN = \frac{R4}{R3}\left[1+\frac{1}{2}\left(\frac{R2}{R1}+\frac{R3}{R4}\right)+\frac{R2+R3}{R5}\right] \approx 100$$

*TRIM FOR COMMON-MODE REJECTION
†TRIM FOR GAIN

TYPICAL PERFORMANCE:
OFFSET VOLTAGE = 20μV
BIAS CURRENT = ±30pA
OFFSET CURRENT = 30pA

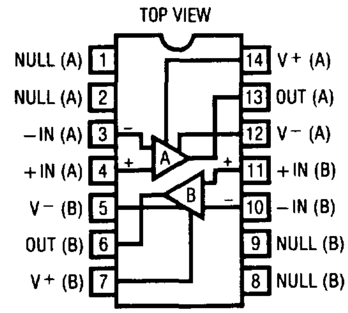
Input Bias Current vs Temperature



ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±20V
Differential Input Current (Note 1) .... ±10mA
Input Voltage .... ±20V
Output Short Circuit Duration .... Indefinite
Operating Temperature Range
LT1024AM/LT1024M .... −55°C to 125°C
LT1024AC/LT1024C .... 0°C to 70°C
Storage Temperature Range
All Devices .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



D PACKAGE
14 PIN HERMETIC
(SIDEBRAZED)

N PACKAGE
14 PIN PLASTIC

NOTE: DEVICE MAY BE OPERATED EVEN IF INSERTION IS REVERSED; THIS IS DUE TO INHERENT SYMMETRY OF PIN LOCATIONS OF AMPLIFIERS A AND B (NOTE 2).

ORDER PART NUMBER
LT1024AMD
LT1024MD
LT1024ACN
LT1024CN

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted

Individual Amplifiers

SYMBOL	PARAMETER	CONDITIONS	LT1024AM/LT1024AC MIN	LT1024AM/LT1024AC TYP	LT1024AM/LT1024AC MAX	LT1024M/LT1024C MIN	LT1024M/LT1024C TYP	LT1024M/LT1024C MAX	UNITS
V_{OS}	Input Offset Voltage			15	50		20	100	μV
	Long Term Input Offset Voltage Stability			0.3			0.3		μV/month
I_{OS}	Input Offset Current			20	100		25	180	pA
I_B	Input Bias Current			±25	±120		±30	±200	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5			0.5		μVp-p
e_n	Input Noise Voltage Density	$f_O = 10Hz$ (Note 3) $f_O = 1000Hz$ (Note 3)		17 14	33 24		17 14	33 24	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	$f_O = 10Hz$		20			20		fA/√Hz
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L \geq 10k\Omega$ $V_{OUT} = \pm10V$, $R_L \geq 2k\Omega$	250 150	2000 1000		180 100	2000 1000		V/mV V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm13.5V$	112	132		108	132		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2V$ to $\pm20V$	112	132		108	132		dB
	Input Voltage Range		±13.5	±14.0		±13.5	±14.0		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	±13	±14		±13	±14		V
	Slew Rate		0.1	0.2		0.1	0.2		V/μs
I_S	Supply Current per Amplifier			380	600		380	700	μA

Matching Specifications

SYMBOL	PARAMETER	CONDITIONS	LT1024AM/LT1024AC MIN	LT1024AM/LT1024AC TYP	LT1024AM/LT1024AC MAX	LT1024M/LT1024C MIN	LT1024M/LT1024C TYP	LT1024M/LT1024C MAX	UNITS
	Input Offset Voltage Match		—	20	75	—	25	150	μV
I_B^+	Average Non-Inverting Bias Current		—	±30	±150	—	±40	±250	pA
I_{OS}^+	Non-Inverting Offset Current		—	30	150	—	30	300	pA
ΔCMRR	Common Mode Rejection Ratio Match	$V_{CM} = \pm13.5V$	110	132	—	106	132	—	dB
ΔPSRR	Power Supply Rejection Ratio Match	$V_S = \pm2V$ to $20V$	110	132	—	106	132	—	dB
	Channel Separation	$f \leq 10Hz$ (Note 3)	134	150	—	134	150	—	dB

LINEAR TECHNOLOGY

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \le T_A \le 70°C$ for the LT1024AC and LT1024C; $-55°C \le T_A \le 125°C$ for the LT1024AM and LT1024M unless otherwise noted

Individual Amplifiers

SYMBOL	PARAMETER	CONDITIONS		LT1024AM/LT1024AC MIN	TYP	MAX	LT1024M/LT1024C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	0°C to 70°C −55°C to 125°C	● ●		30 40	120 200		35 50	200 300	μV μV
	Average Temperature Coefficient of Input Offset Voltage		●		0.25	1.5		0.3	2.0	μV/°C
I_{OS}	Input Offset Current	0°C to 70°C −55°C to 125°C	● ●		40 80	250 350		50 100	300 500	pA pA
	Average Temperature Coefficient of Input Offset Current		●		0.5	2.5		0.7	3	pA/°C
I_B	Input Bias Current	0°C to 70°C −55°C to 125°C	● ●		±40 ±100	±250 ±700		±50 ±200	±400 ±1300	pA pA
	Average Temperature Coefficient of Input Bias Current	0°C to 70°C −55°C to 125°C	● ●		0.4 1	3 6		0.5 2	4 12	pA/°C pA/°C
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L \ge 10k\Omega$ $V_{OUT} = \pm 10V$, $R_L \ge 2k\Omega$	● ●	150 100	1000 600		150 100	1000 600		V/mV V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	108	128		106	128		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 18V$	●	108	128		106	128		dB
	Input Voltage Range		●	±13.5			±13.5			V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13	±14		±13	±14		V
I_S	Supply Current		●		400	800		400	900	μA

Matching Specifications

SYMBOL	PARAMETER	CONDITIONS		LT1024AM/LT1024AC MIN	TYP	MAX	LT1024M/LT1024C MIN	TYP	MAX	UNITS
	Input Offset Voltage Match	0°C to 70°C −55°C to 125°C	● ●	 —	35 50	170 280	 —	45 70	300 500	μV μV
	Input Offset Voltage Tracking		●	—	0.3	2.0	—	0.4	3.5	μV/°C
I_B^+	Average Non-Inverting Bias Current	0°C to 70°C −55°C to 125°C	● ●	 —	±40 ±100	±300 ±800	 —	±50 ±200	±500 ±1400	pA pA
I_{OS}^+	Non-Inverting Offset Current	0°C to 70°C −55°C to 125°C	● ●	— —	40 80	300 800	— —	50 150	500 1500	pA pA
ΔCMRR	Common-Mode Rejection Ratio Match	$V_{CM} = \pm 13.5V$	●	106	128	—	104	128	—	dB
ΔPSRR	Power Supply Rejection Ratio Match	$V_S = \pm 2.5V$ to $\pm 18V$	●	106	128	—	104	128	—	dB

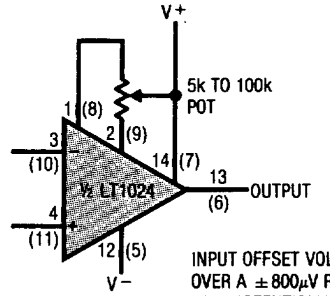
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Note 2: The V^+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V^- supply terminals are both connected to the common substrate and must be tied to the same voltage. Both V^- pins should be used.

Note 3: This parameter is tested on a sample basis only.

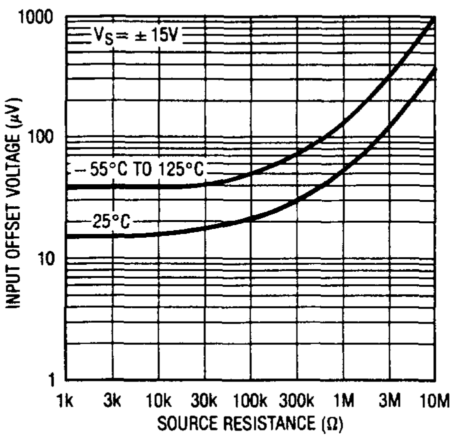
Optional Offset Nulling Circuit



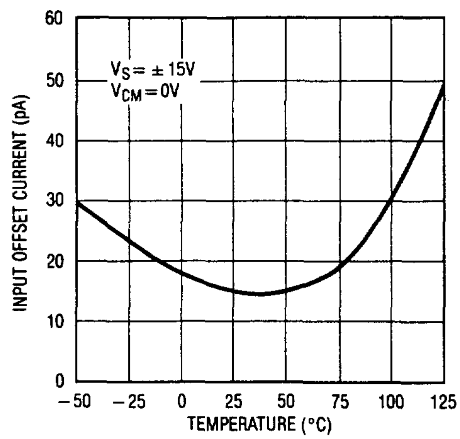
INPUT OFFSET VOLTAGE CAN BE ADJUSTED OVER A ±800μV RANGE WITH A 5k TO 100k POTENTIOMETER.

TYPICAL PERFORMANCE CHARACTERISTICS

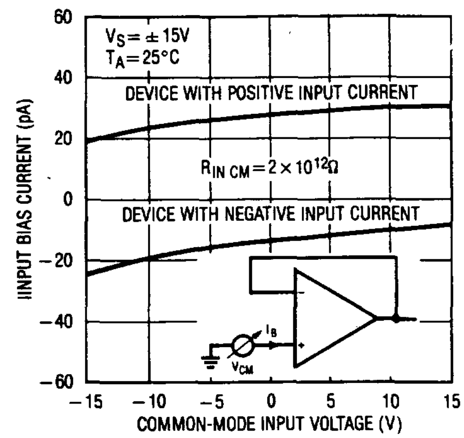
Offset Voltage vs Source Resistance (Balanced or Unbalanced)



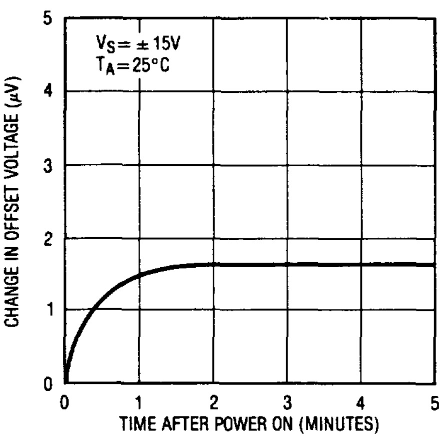
Input Offset Current vs Temperature



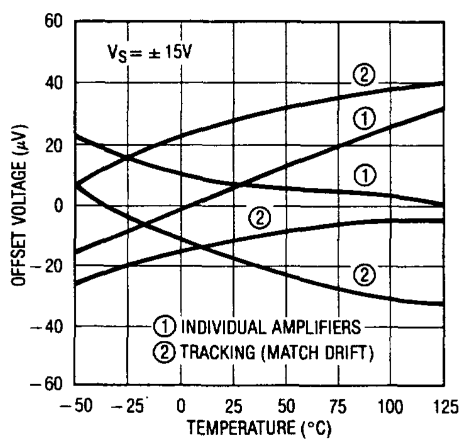
Input Bias Current Over Common-Mode Range



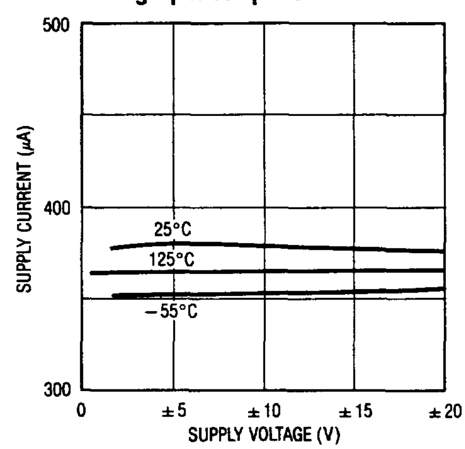
Warm-Up Drift



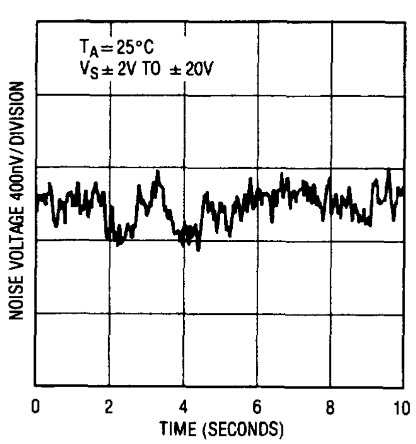
Offset Voltage Drift and Tracking with Temperature of Representative Units



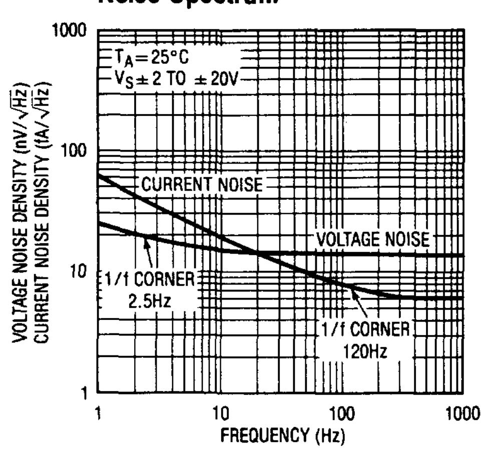
Supply Current vs Supply Voltage per Amplifier



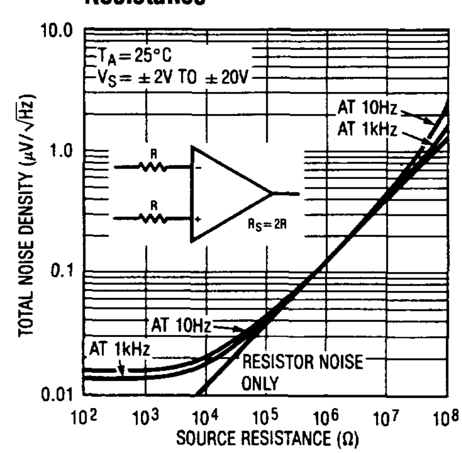
0.1Hz to 10Hz Noise



Noise Spectrum



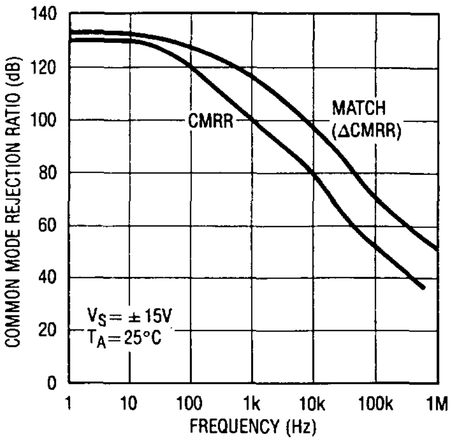
Total Noise vs Source Resistance



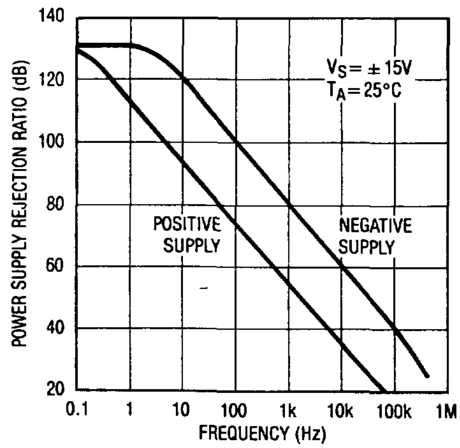
LINEAR TECHNOLOGY

TYPICAL PERFORMANCE CHARACTERISTICS

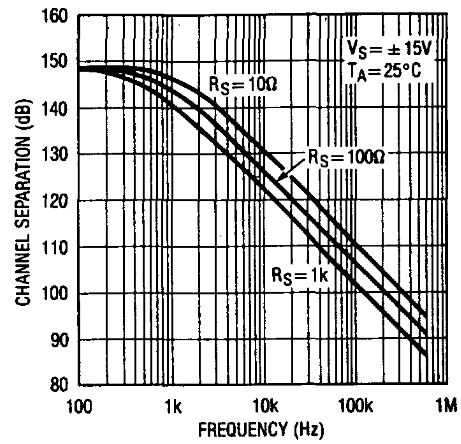
Common-Mode Rejection and CMRR Match vs Frequency



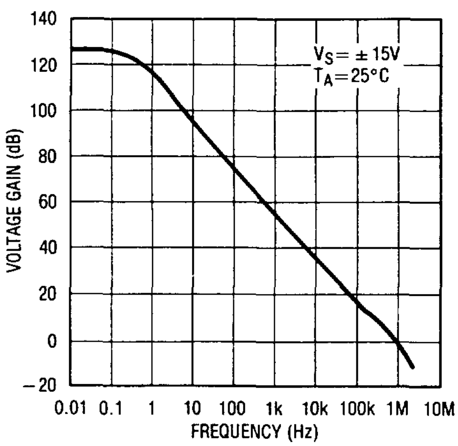
Power Supply Rejection vs Frequency



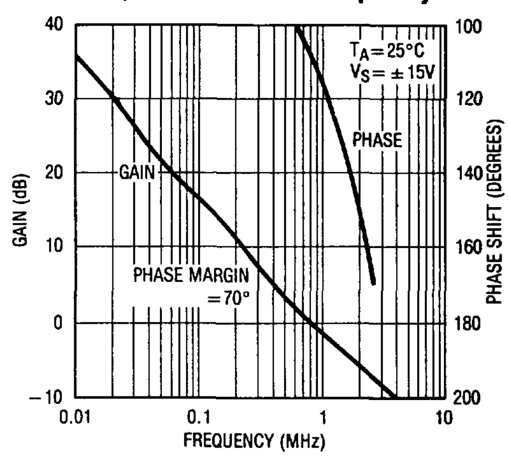
Channel Separation vs Frequency



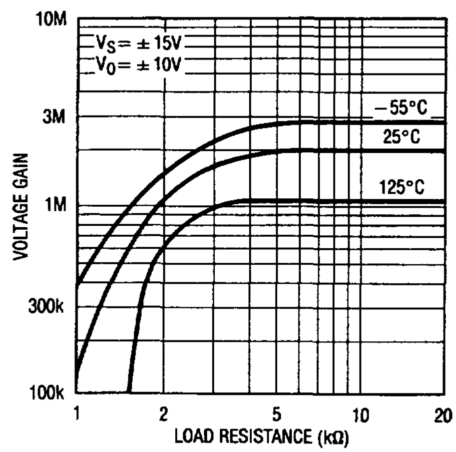
Voltage Gain vs Frequency



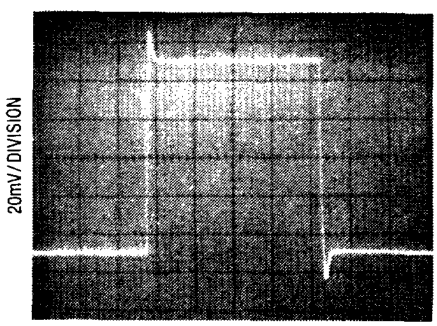
Gain, Phase Shift vs Frequency



Voltage Gain vs Load Resistance

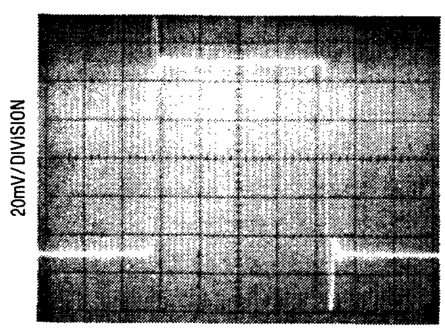


Small Signal Transient Response



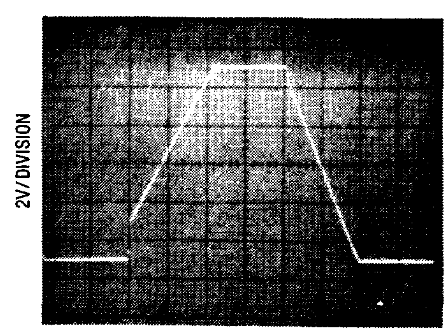
$A_V = +1$, $C_{LOAD} = 100pF$, 5μsec/DIV

Small Signal Transient Response



$A_V = +1$, $C_{LOAD} = 1000pF$, 5μsec/DIV

Large Signal Transient Response



$A_V = +1$, 20μsec/DIV

2

APPLICATIONS INFORMATION

The LT1024 may be inserted directly into OP-10, OP-207 or OP227 sockets with or without removal of external nulling components.

The LT1024 is specified over a wide range of power supply voltages from ±2V to ±18V. Operation with lower supplies is possible down to ±1.2V (two NiCad batteries).

Advantages of Matched Dual Op Amps

In many applications, the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references, and low drift active filters are some of the circuits requiring matching between two op amps.

The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the LT1024. This error cancellation principle holds for a considerable number of input-referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two non-inverting input currents ($I_B{}^+$). The difference between these two currents ($I_{OS}{}^+$) is the offset current of the instrumentation amplifier. Common-mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

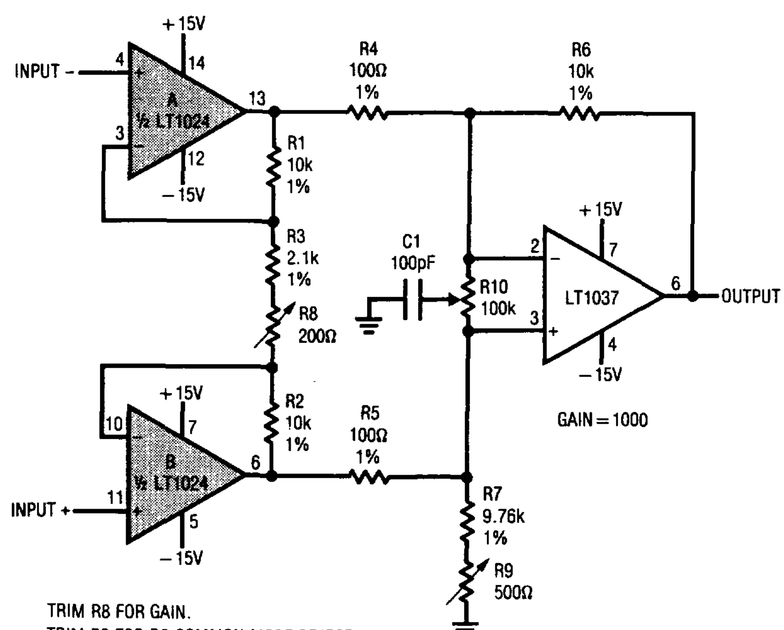
The concepts of common-mode and power supply rejection ratio match (ΔCMRR and ΔPSRR) are best demonstrated with a numerical example:

Assume $CMRR_A = +1.0\mu V/V$ or 120dB
and $CMRR_B = +0.5\mu V/V$ or 126dB,
then $\Delta CMRR = 0.5\mu V/V$ or 126dB
if $CMRR_B = -0.5\mu V/V$, which is still 126dB,
then $\Delta CMRR = 1.5\mu V/V$ or 116.5dB.

Typical performance of the instrumentation amplifier:
Input offset voltage = 25µV.
Input bias current = 30pA.
Input resistance = $10^{12}\Omega$.
Input offset current = 30pA.
Input noise = 0.7µVp-p.
Power bandwidth ($V_O = \pm 10V$) = 80kHz.

Clearly, the LT1024, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching dependent circuits.

Three Op Amp Instrumentation Amplifier



TRIM R8 FOR GAIN.
TRIM R9 FOR DC COMMON-MODE REJECTION.
TRIM R10 FOR AC COMMON-MODE REJECTION.

APPLICATIONS INFORMATION

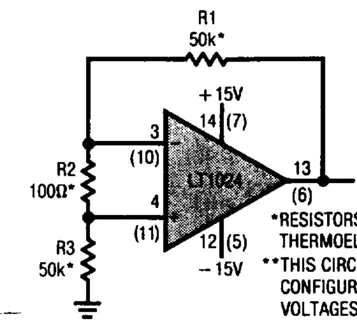
Achieving Picoampere/Microvolt Performance

In order to realize the picoampere/microvolt level accuracy of the LT1024, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations, the guard ring should be tied to ground, in non-inverting connections, to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width. Nanoampere level leakage into the offset trim terminals can affect offset voltage and drift with temperature.

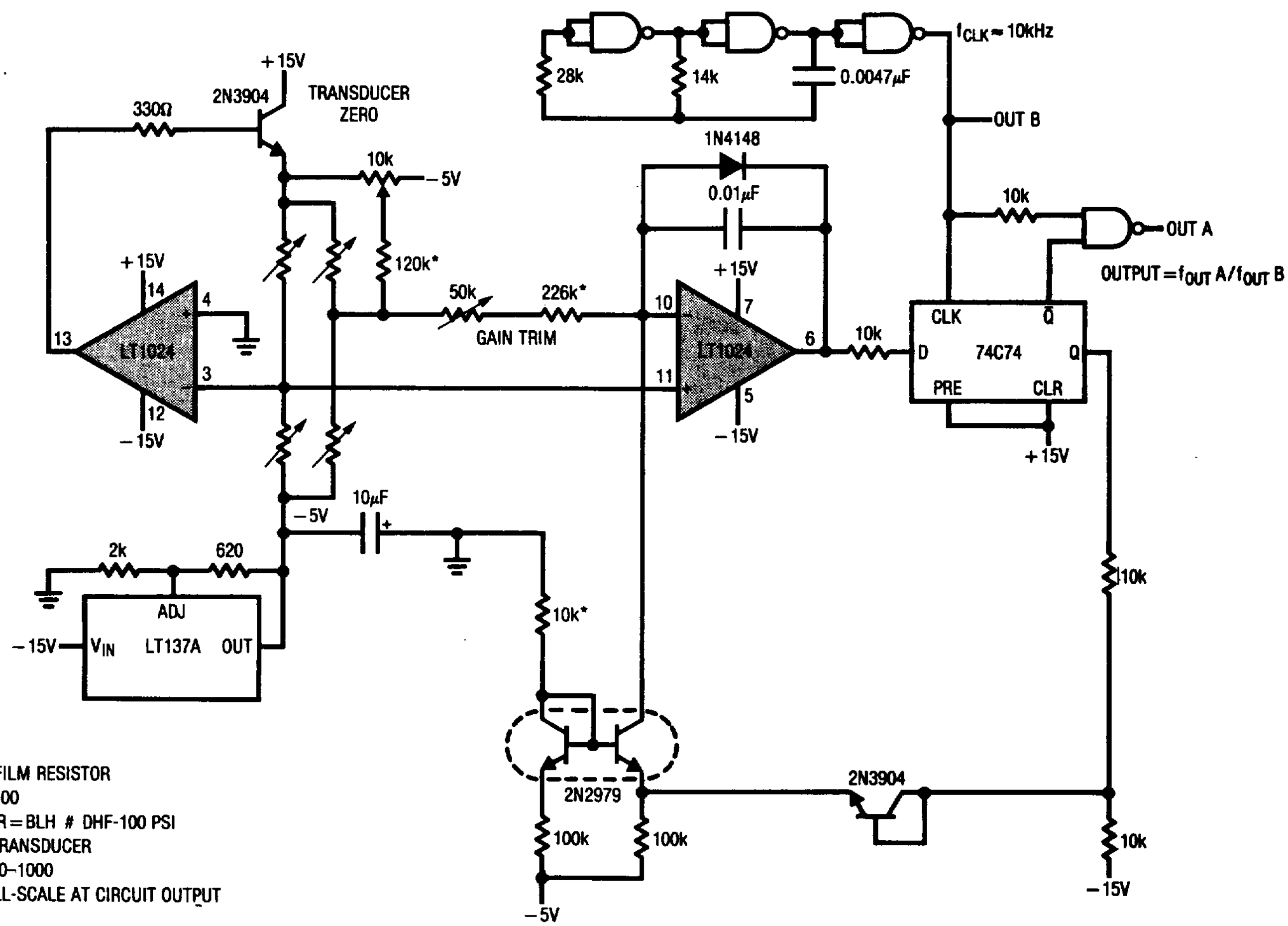
Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Test Circuit for Offset Voltage and its Drift with Temperature



*RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.
**THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION FOR THE LT1024, WITH SUPPLY VOLTAGES INCREASED TO ±20V, R1 = R3 = 20k, R2 = 200Ω, $A_V = 100$.
$V_O = 1000V_{OS}$

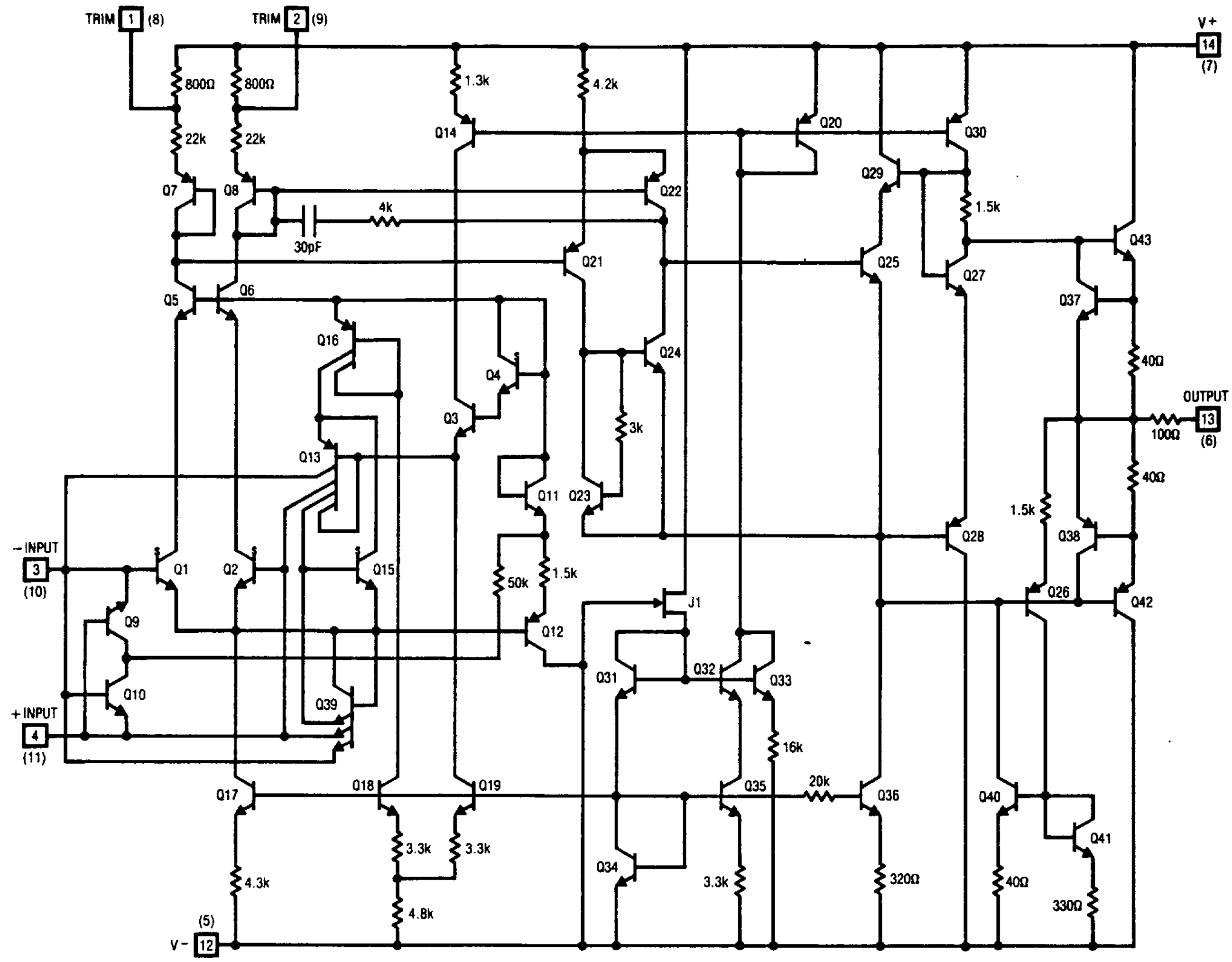
Direct Pressure Transducer to Digital Output Signal Conditioner



*1% METAL FILM RESISTOR
GATES = 74C00
TRANSDUCER = BLH # DHF-100 PSI PRESSURE TRANSDUCER
0–100 PSI = 0–1000 COUNTS FULL-SCALE AT CIRCUIT OUTPUT

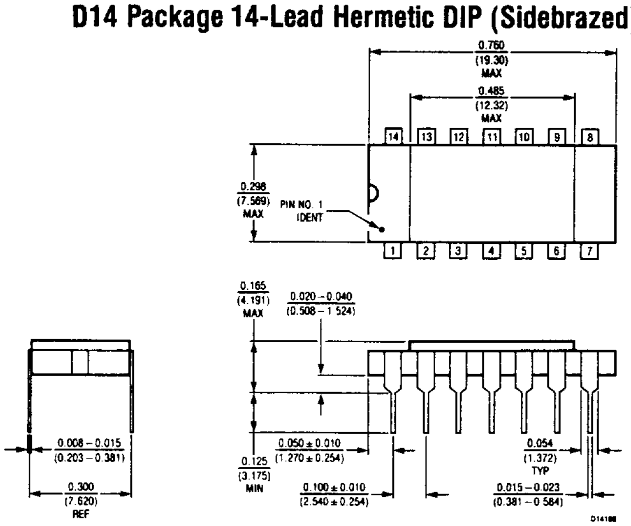
SCHEMATIC DIAGRAM

½ LT1024



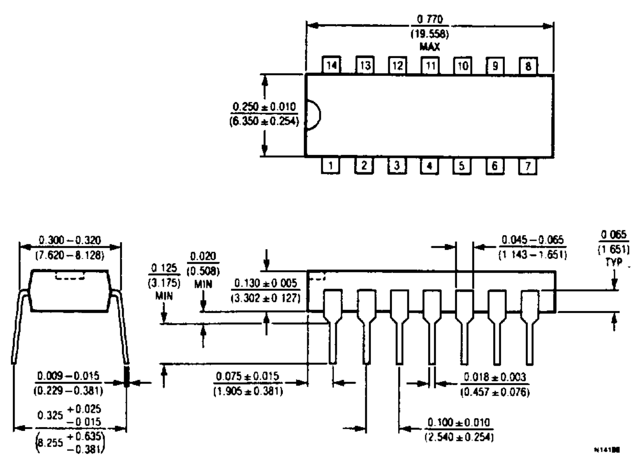
PACKAGE DESCRIPTION

D14 Package 14-Lead Hermetic DIP (Sidebrazed)



T_{JMAX}	θ_{JA}	θ_{JC}
150°C	100°C/W	60°C/W

N14 Package 14-Lead Plastic



T_{JMAX}	θ_{JA}	θ_{JC}
100°C	100°C/W	60°C/W

LINEAR TECHNOLOGY