3.3V µP Power Supply Monitor and Reset Circuit

General Description

The ASM1832 is a fully integrated microprocessor supervisor. It can halt and restart a “hung-up” microprocessor, restart a microprocessor after a power failure. It has a watchdog timer and external reset override. RESET and $\overline{\text{RESET}}$ outputs are push-pull.

A precision temperature-compensated reference and comparator circuits monitor the 3.3V, V_{CC} input voltage status. During power-up or when the V_{CC} power supply falls outside selectable tolerance limits, both RESET and $\overline{\text{RESET}}$ become active. When V_{CC} rises above the threshold voltage, the reset signals remain active for an additional 250ms minimum, allowing the power supply and system microprocessor to stabilize. The trip point tolerance signal, TOL, selects the trip level tolerance to be either 10% or 20%.

A debounced manual reset input, $\overline{\text{PBRST}}$, activates the reset outputs for a minimum period of 250ms. There is a watchdog timer to stop and restart a microprocessor that is “hung-up”. The watchdog timeouts periods are selectable: 150ms, 610ms, and 1200ms. If the $\overline{\text{ST}}$ input is not strobed LOW before the time-out period expires, a reset is generated.

Devices are available in 8-pin PDIP, 8-pin SO and compact 8-pin MicroSO packages.

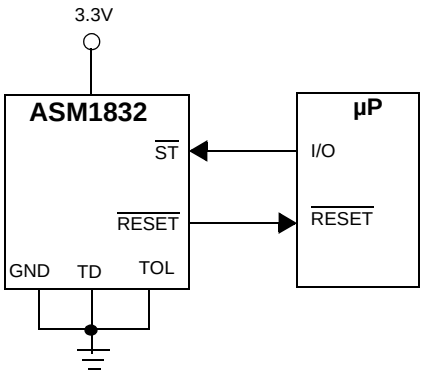
Key Features

- 3.3V supply monitor
- Push-pull output
- Selectable watchdog period
- Debounce manual push-button reset input
- Precision temperature-compensated voltage reference and comparator.
- Power-up, power-down and brown out detection
- 250ms minimum reset time
- Active LOW and HIGH reset signal
- Selectable trip point tolerance: 10% or 20%
- Low-cost 8-pin DIP/SO and 8-pin Micro SO packages
- Wide operating temperature -40°C to +85°C

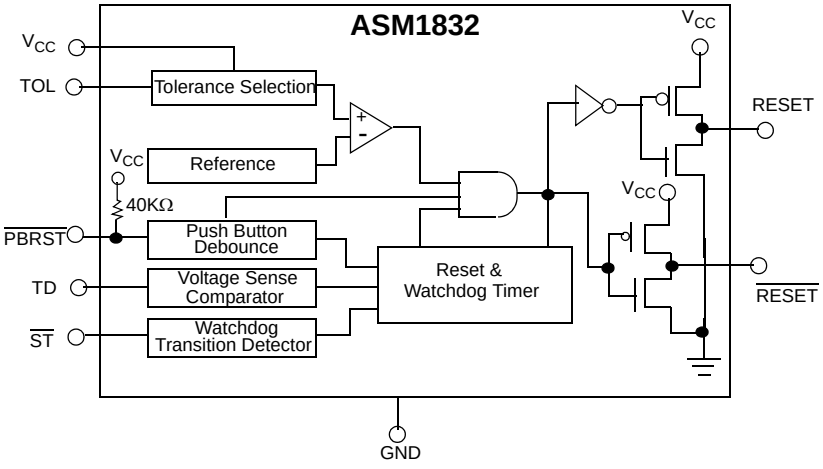
Applications

- Microprocessor systems
- Computers
- Controllers
- Portable instruments
- Automotive systems

Typical Operating Circuit



Block Diagram



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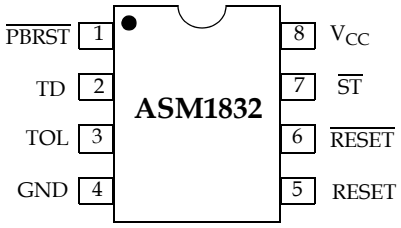
Pin Configuration



Pin Description

Pin # 8-Pin Package	Pin Name	Function
1	$\overline{\text{PBRST}}$	Debounced manual pushbutton reset input.
2	TD	Watchdog time delay selection. (t_{TD} = 150ms for TD = GND, t_{TD} = 610ms for TD=Open, and t_{TD} = 1200ms for TD = V_{CC}).
3	TOL	Selects 10% (TOL connected to GND) or 20% (TOL connected to V_{CC}) trip point tolerance.
4	GND	Ground.
5	RESET	Active HIGH reset output. RESET is active: 1. If V_{CC} falls below the reset voltage trip point. 2. If $\overline{\text{PBRST}}$ is LOW. 3. If $\overline{\text{ST}}$ is not strobed LOW before the timeout period set by TD expires. 4. During power-up.
6	$\overline{\text{RESET}}$	Active LOW reset output. (See RESET).
7	$\overline{\text{ST}}$	Strobe input.
8	V_{CC}	3.3V power.

Detailed Description

The ASM1832 monitors the microprocessor or microcontroller power supply and issues reset signals, both active HIGH and active LOW, that halt processor operation whenever the power supply voltage levels are outside a predetermined tolerance.

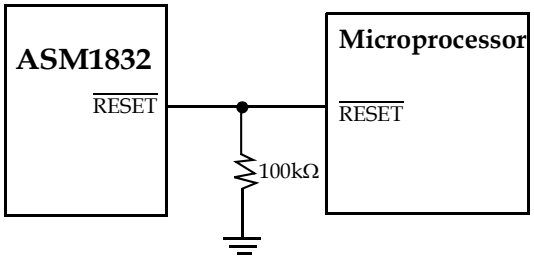
RESET and $\overline{\text{RESET}}$ outputs

RESET and $\overline{\text{RESET}}$ signals are active for a minimum of 250ms after the supply has returned to in-tolerance level. This allows the power supply and monitored processor to stabilize before instruction execution is allowed to begin.

Trip Point Tolerance Selection

The TOL input is used to determine the level V_{CC} can vary below 3.3V without asserting a reset. With TOL conected to V_{CC}, RESET and $\overline{\text{RESET}}$ become active whenever V_{CC} falls below 2.64V. RESET and $\overline{\text{RESET}}$ become active when the V_{CC} falls below 2.98V if TOL is connected to ground.

After V_{CC} has risen above the trip point set by TOL, RESET and $\overline{\text{RESET}}$ remain active for a minimum time period of 250ms. On power-down, once V_{CC} falls below the reset threshold $\overline{\text{RESET}}$ stays LOW and is guaranteed to be 0.4V or less until V_{CC} drops below 1.2V. The reset output on the ASM1832 uses a push-pull drive stage that can maintain a valid output below 1.2V. To sink current with V_{CC} below 1.2V, a resistor can be connected from the reset pin ($\overline{\text{RESET}}$) to Ground. This configuration will give a valid value on the reset output with V_{CC} approaching 0V. During both power up and down, the configuration will draw current when the $\overline{\text{RESET}}$ is in the high state. The value of 100KΩ should be adequate to maintain a valid condition. The active HIGH reset signal is valid down to a V_{CC} level of 1.2V also.



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Tolerance Select	Tolerance	TRIP Point Voltage (V)		
		Min	Nom	Max
TOL = V_{CC}	20%	2.47	2.55	2.64
TOL = GND	10%	2.80	2.88	2.97

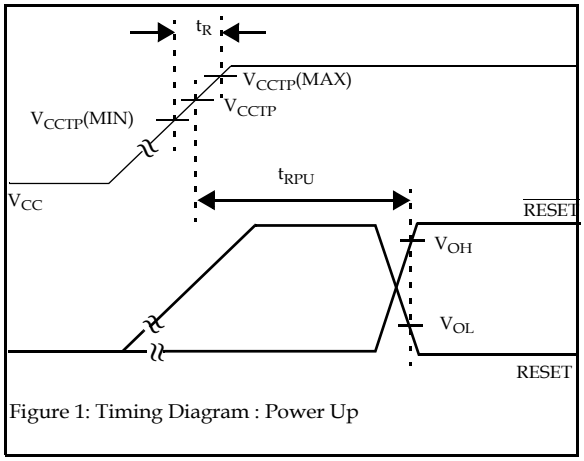


Figure 1: Timing Diagram : Power Up

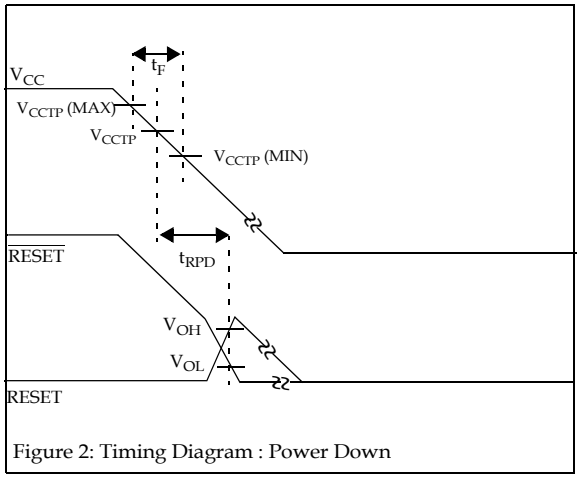


Figure 2: Timing Diagram : Power Down

Application Information

Manual Reset Operation

Push-button switch input, $\overline{\text{PBRST}}$, allows the user to override the internal trip point detection circuits and issue reset

signals. The pushbutton input is debounced and is pulled HIGH through an internal 40kΩ resistor.

When $\overline{PBRST}$ is held LOW for the minimum time t_{PB}, both resets become active and remain active for a minimum time period of 250ms after $\overline{PBRST}$ returns HIGH.

The debounced input is guaranteed to recognize pulses greater than 20ms. No external pull-up resistor is required, since $\overline{PBRST}$ is pulled HIGH by an internal 40kΩ resistor.

The $\overline{PBRST}$ can be driven from a TTL or CMOS logic line or shorted to ground with a mechanical switch.

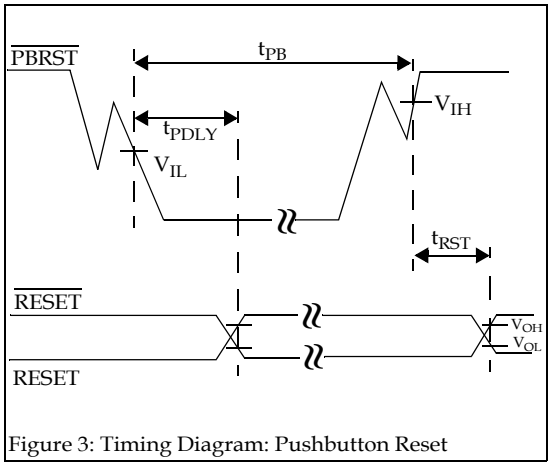


Figure 3: Timing Diagram: Pushbutton Reset

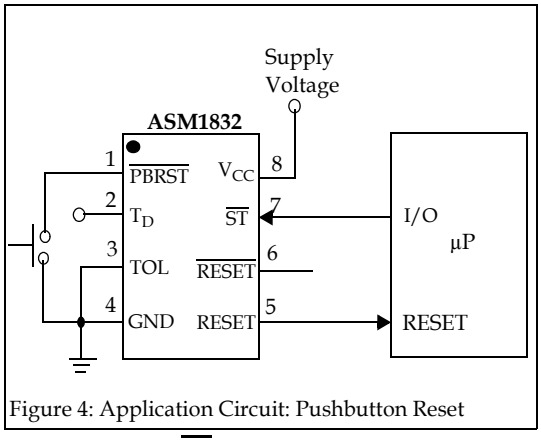
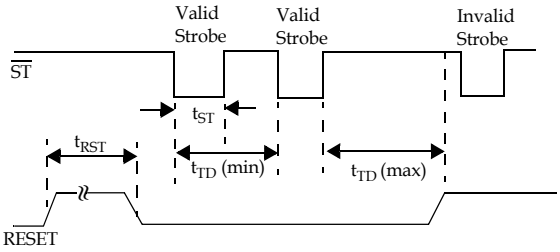


Figure 4: Application Circuit: Pushbutton Reset

Watchdog Timer and $\overline{ST}$ Input

A watchdog timer stops and restarts a microprocessor that is "hung-up". The µP must toggle the $\overline{ST}$ input within a set period (as selectable through TD input) to verify proper software execution. If the $\overline{ST}$ is not toggled low within the minimum timeout period, reset signals become active. On power-up after the supply voltage returns to an in-tolerance condition, the reset signal remains active for 250ms minimum, allowing the power supply and system microprocessor to stabilize.

$\overline{ST}$ Pulses as short as 20ns can be detected.



Note: $\overline{ST}$ is ignored whenever a reset is active

Figure 5: Timing Diagram: Strobe Input

Timeouts periods of approximately 150ms, 610ms or 1,200ms are selected through the TD pin.

TD Voltage level	Watchdog Time-out Period (ms)		
	Min	Nom	Max
GND	62.5	150	250
Floating	250	610	1000
V_{CC}	500	1200	2000

The watchdog timer can not be disabled. It must be strobed with a high-to-low transition to avoid watchdog timeout and reset.

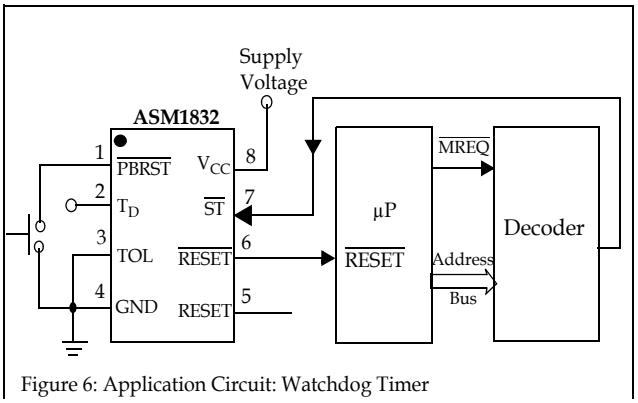


Figure 6: Application Circuit: Watchdog Timer

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Absolute Maximum Ratings

Parameter	Min	Max	Unit
Voltage on VCC	-0.5	7	V
Voltage on $\overline{ST}$, TD	-0.5	V_{CC} + 0.5	V
Voltage on $\overline{PBRST}$, RESET, $\overline{RESET}$	-0.5	V_{CC} + 0.5	V
Operating Temperature Range	-40	+85	°C
Soldering Temperature (for 10 sec)		+260	°C
Storage Temperature	-55	+125	°C
ESD rating HBM MM		 2 200	 KV V

Note:
1. Voltages are measured with respect to ground
2. These are stress ratings only and functional implication is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC Electrical Characteristics

Unless otherwise stated, 1.2 <= V_{CC}<=5.5V and over the operating temperature range of -40°C to +85°C. All voltages are referenced to ground.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		1.0		5.5	V
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	V_{IH}	V_{CC} >=2.7V	2		V_{CC} + 0.3	V
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	V_{IH}	V_{CC}<2.7V	V_{CC} - 0.4V			V
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}		-0.3		0.5	V
V_{CC} Trip Point (T_{OL} = GND)	V_{CCTP}		2.80	2.88	2.97	V
V_{CC} Trip Point (T_{OL} = V_{CC})	V_{CCTP}		2.47	2.55	2.64	V
Watchdog Timeout Period	t_{TD}	T_D = GND	62.5	150	250	ms

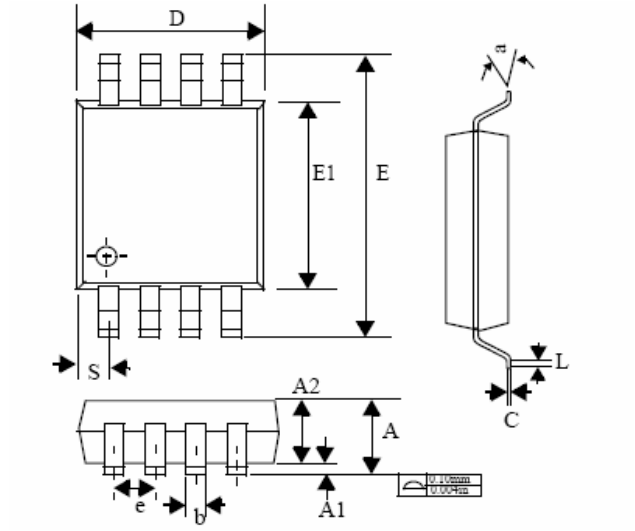
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Watchdog Timeout Period	t_{TD}	T_D = VCC	500	1200	2000	ms
Watchdog Timeout Period	t_{TD}	T_D Floating	250	610	1000	ms
Output Voltage	V_{OH}	I=-500µA, V_{CC} < 2.7V Note 1	V_{CC} - 0.3V	V_{CC} - 0.1V		V
Output Current	I_{OH}	Output = 2.4V, V_{CC} >=2.7V		350		µA
Output Current	I_{OL}	Output = 0.4V, V_{CC} >=2.7V	10			mA
Input Leakage	I_{IL}		-1.0		1.0	µA
RESET Low Level	V_{OL}	Note 1			0.4	V
Internal Pull-up Resistor		$\overline{PBRST}$ pin		40		kΩ
Operating Current	I_{CC1}	Outputs open, V_{CC} <= 3.6V and all inputs at V_{CC} or GND			20	µA
Input Capacitance	C_{IN}				5	pF
Output Capacitance	C_{OUT}				7	pF
$\overline{PBRST}$ Manual Reset Minimum Low Time	t_{PB}	$\overline{PBRST}$ = V_{IL}	20			ms
Reset Active Time	t_{RST}		250	610	1000	ms
$\overline{ST}$ Pulse Width	t_{ST}	Must not exceed t_{RD} minimum. Watchdog cannot be disabled.	20			ns
V_{CC} Fail Detect to $\overline{RESET}$ or RESET	t_{RPD}	Pulses < 2 µs at V_{CCTP} minimum will not cause reset		5	8	µs
V_{CC} Slew Rate	t_F		20			µs
$\overline{PBRST}$ Stable LOW to RESET and $\overline{RESET}$ Active	t_{PDLY}				20	ms
V_{CC} Detect to RESET or $\overline{RESET}$ inactive	t_{RPU}	t_{rise}=5µs	250	610	1000	ms
V_{CC} Slew Rate	t_R		0			ns

Notes

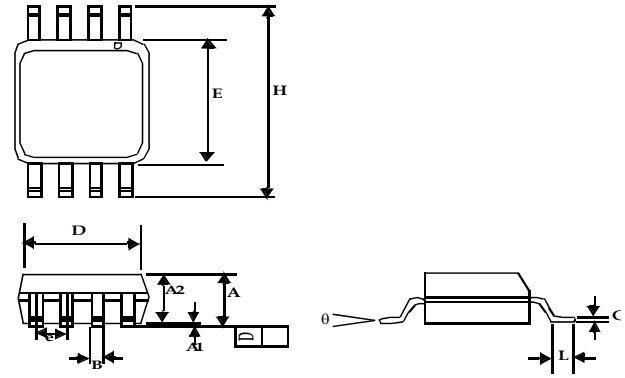
1. RESET remains within 0.5V of V_{CC} on power-down until V_{CC} falls below 2V. $\overline{RESET}$ remains within 0.5V of ground on power-down until V_{CC} falls below 2.0V.

Package Information

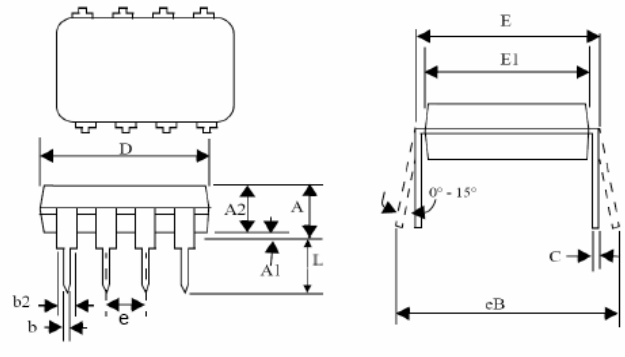
MicroSO (8-Pin)



SO (8-Pin)



Plastic DIP (8-Pin)



	Inches		Millimeteres	
	Min	Max	Min	Max
MicroSO (8-Pin)				
A	0.032	0.044	0.81	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.038	0.76	0.97
b	0.012 BSC		0.30 BSC	
C	0.004	0.008	0.10	0.20
D	0.114	0.122	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.184	0.200	4.67	5.08
E1	0.114	0.122	2.90	3.10
L	0.016	0.026	0.41	0.66
S	0.0206 BSC		0.52 BSC	
a	0°	6°	0°	6°
SO (8-Pin)				
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°
Plastic DIP (8-Pin)				
A	-	0.210	-	5.33
A1	0.015	-	0.38	-
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.36	0.56
b2	0.045	0.070	1.14	1.78
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	-	0.430	-	10.92
L	0.115	0.150	2.92	3.81

Ordering Information

Part Number	Package	Operating Temperature Range	Maximum Supply Current (µA)	Voltage Monitoring Application	Package Marking
TIN - LEAD DEVICES					
ASM1832	8-Pin PDIP	-40°C to 85°C	20	3.3 V	ASM1832
ASM1832S	8-SO	-40°C to 85°C	20	3.3 V	ASM1832S
ASM1832U	8-MicroSO	-40°C to 85°C	20	3.3 V	ASM1832
LEAD FREE DEVICES					
ASM1832F	8-Pin PDIP	-40°C to 85°C	20	3.3 V	ASM1832F
ASM1832SF	8-SO	-40°C to 85°C	20	3.3 V	ASM1832SF
ASM1832UF	8-MicroSO	-40°C to 85°C	20	3.3 V	ASM1832F

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