14 Bit, 800ksps Sampling

A/D Converter with Shutdown

FEATURES

- Sample Rate: 800ksps
- Power Dissipation: 150mW
- 81.5dB S/(N+D) and 93dB THD
- No Missing Codes
- No Pipeline Delay
- Nap and Sleep Shutdown Modes
- Operates with 2.5V Internal 15ppm/°C Reference or External Reference
- True Differential Inputs Reject Common Mode Noise
- 20MHz Full-Power Bandwidth Sampling
- Bipolar Input Range: ±2.5V
- 28-pin LCC and Flatpack packages

OPTIONS — MARKING

- **Package(s)**
  - 28-Pin Flat-pack — F
  - 28-Pin LCC — ECA
- **Operating Temperature Ranges**
  - Extended Temperature (-55°C to +125°C) — XT
  - Industrial Temperature (-40°C to +85°C) — IT
  - Military Processing (-55°C to +125°C) — MIL
  - Space Processing (-55°C to +125°C) — SPACE*

**As defined by individual customer Source Control Drawing (SCD)*

GENERAL DESCRIPTION

The AS1419 is a 1µs, 800ksps, 14-bit sampling A/D converter that draws only 150mW from ±5V supplies. This easy-to-use device includes a high dynamic range sample-and-hold and a precision reference. Two digitally selectable power shutdown modes provide flexibility for low power systems.

The AS1419 has a full-scale input range of ±2.5V. Outstanding AC performance includes 81.5dB S/(N + D) and 93dB THD with a 100kHz input; 80dB S/(N + D) and 86dB THD at the Nyquist input frequency of 400kHz.

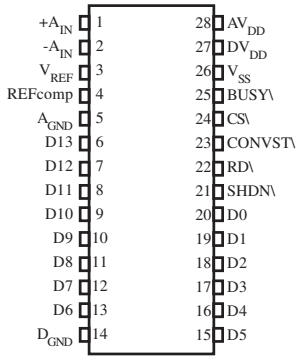
The unique differential input sample-and-hold can acquire single-ended or differential input signals up to its 20MHz bandwidth. The 60dB common mode rejection allows users to eliminate ground loops and common mode noise by measuring signals differentially from the source.

The ADC has a microprocessor compatible, 14-bit parallel output port. There is no pipeline delay in the conversion results. A separate convert start input and data ready signal (BUSY\) ease connections to FIFOs, DSPs and microprocessors.

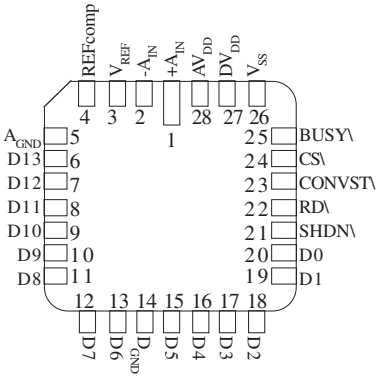
PIN ASSIGNMENT

(Top View)

28-Pin Flat Pack (F)



28-Pin LCC (ECA)



Typical applications are telecommunications, digital signal processing, multiplexed data acquisition systems, high speed data acquisitions, spectrum analysis, and imaging systems.

For more products and information please visit our web site at *www.austinsemiconductor.com*

ABSOLUTE MAXIMUM RATINGS*

$AV_{DD} = V_{DD} = DV_{DD}$ [1,2]

Supply Voltage (V_{DD}).....6V
Negative Supply Voltage (V_{SS}).....-6V
Total Supply Voltage (V_{DD} to V_{SS}).....12V
Analog Input Voltage[3].....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Digital Input Voltage[4].....(V_{SS} - 0.3V) to 10V
Digital Output Voltage.....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Power Dissipation.....500mW
Operating Temperature Range
Military.....-55°C to +125°C
Industrial.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses at or greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods will affect reliability.

CONVERTER CHARACTERISTICS (* denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = +25°C. With Internal Reference[5,6])

			AS1419			AS1419A			
PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		*	13			14			Bits
Integral Linearity Error[7]		*		±0.8	±2		±0.6	±1.25	LSB
Differential Linearity Error		*		±0.7	±1.5		±0.5	±1	LSB
Offset Error[8]		*		±5	±20		±5	±20	LSB
Full-Scale Error	Internal Reference			±10	±60		±10	±60	LSB
	External Reference = 2.5V			±5			±5		LSB
Full Scale Tempco	$I_{OUT(REF)}$ = 0			±15			±15		ppm/°C

ANALOG INPUT (* denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = +25°C.[5])

PARAMETER	CONDITIONS		SYM	MIN	TYP	MAX	UNITS
Analog Input Range[9]	4.75V ≤ V_{DD} ≤ 5.25V, -5.25V ≤ V_{SS} ≤ -4.75V	*	V_{IN}		±2.5		V
Analog Input Leakage Current	CS\ = HIGH	*	I_{IN}			±1	µA
Analog Input Capacitance	Between Conversions		C_{IN}		15		pF
	During Conversions		C_{IN}		5		pF
Sample-and-Hold Acquisition Time		*	t_{ACQ}		90	300	ns
Sample-and-Hold Aperture Delay Time			t_{AP}		-1.5		ns
Sample-and-Hold Aperture Delay Time Jitter			t_{jitter}		2		ps_{RMS}
Analog Input Common Mode Rejection Ratio	-2.5V < ($-A_{IN}$ = A_{IN}) < 2.5V		CMRR		60		dB

DYNAMIC ACCURACY (* denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = +25°C.)[5]

PARAMETER	CONDITIONS		SYM	MIN	TYP	MAX	-40	-55	UNITS
Signal-to(Noise + Distortion) Ratio	100kHz Input Signal	*	S/(N + D)	78	81.5		75	75	dB
	390 kHz Input Signal	*	S/(N + D)		80.0				dB
Total Harmonic Distortion	100kHz Input Signal, First 5 Harmonics	*	THD		-93	-86	-78	-75	dB
	390 kHz Input Signal, First 5 Harmonics	*	THD		-86				dB
Spurious Free Dynamic Range	100KHz Input Signal	*	SFDR		-95	-86	-80	-79	dB
Intermodulation Distortion	f_{IN1} = 29.37kHz, f_{IN2} = 32.446kHz		IMD		-86				dB
Full-Power Bandwidth					20				MHz
Full-Linear Bandwidth	S/(N + D) ≥ 77dB				1				MHz

INTERNAL REFERENCE CHARACTERISTICS [5]

PARAMETER	CONDITIONS	SYM	MIN	TYP	MAX	UNITS
Output Voltage	I_{OUT} = 0	V_{REF}	2.480	2.500	2.520	V
Output Tempco	I_{OUT} = 0	V_{REF}		±15		ppm/°C
Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V, -5.25V ≤ V_{SS} ≤ -4.75V	V_{REF}		0.05		LSB/V
Output Resistance	-0.1mA ≤ | I_{OUT} | ≤ 0.1mA	V_{REF}		2		kΩ
Output Voltage	I_{OUT} = 0	REFcomp		4.06		V

DIGITAL INPUTS AND DIGITAL OUTPUTS (* denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = +25°C.)[5]

PARAMETER	CONDITIONS		SYM	MIN	TYP	MAX	UNITS
High Level Input Voltage	V_{DD} = 5.25V	*	V_{IH}	2.4			V
Low Level Input Voltage	V_{DD} = 4.75V	*	V_{IL}			0.8	V
Digital Input Current	V_{IN} = 0V to V_{DD}	*	I_{IN}			±10	µA
Digital Input Capacitance			C_{IN}		5		pF
High Level Output Voltage	V_{DD} = 4.75V		V_{OH}				
	I_O = -10µA				4.5		V
	I_O = -200µA	*		4.0			V
Low Level Output Voltage	V_{DD} = 4.75V		V_{OL}				
	I_O = 160µA				0.05		V
	I_O = 1.6mA	*			0.10	0.4	V
High-Z Output Leakage D13 to D0	V_{OUT} = 0V to V_{DD}, CS\ High	*	I_{OZ}			±10	µA
High-Z Output Capacitance D13 to D0	CS\ High[9]	*	C_{OZ}			15	pF
Output Source Current	V_{OUT} = 0V		I_{SOURCE}		-10		mA
Output Sink Current	V_{OUT} = V_{DD}		I_{SINK}		10		mA

POWER REQUIREMENTS (* denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = +25°C.)[5]

PARAMETER	CONDITIONS		SYM	MIN	TYP	MAX	UNITS
Positive Supply Voltage[10]			V_{DD}	4.75		5.25	V
Negative Supply Voltage[10]			V_{SS}	4.75		-5.25	V
Positive Supply Current		*	I_{DD}		11	20	mA
	Nap Mode: SHDN\ = 0V, CS\ = 0V				1.5		mA
	Sleep Mode: SHDN\ = 0V, CS\ = 5V				250		µA
Negative Supply Current		*	I_{SS}		19	30	mA
	Nap Mode: SHDN\ = 0V, CS\ = 0V				100		mA
	Sleep Mode: SHDN\ = 0V, CS\ = 5V				1		µA
Power Dissipation		*	P_{DIS}		150	240	mW
	Nap Mode: SHDN\ = 0V, CS\ = 0V				7.5	12	mW
	Sleep Mode: SHDN\ = 0V, CS\ = 5V				1.2		mW

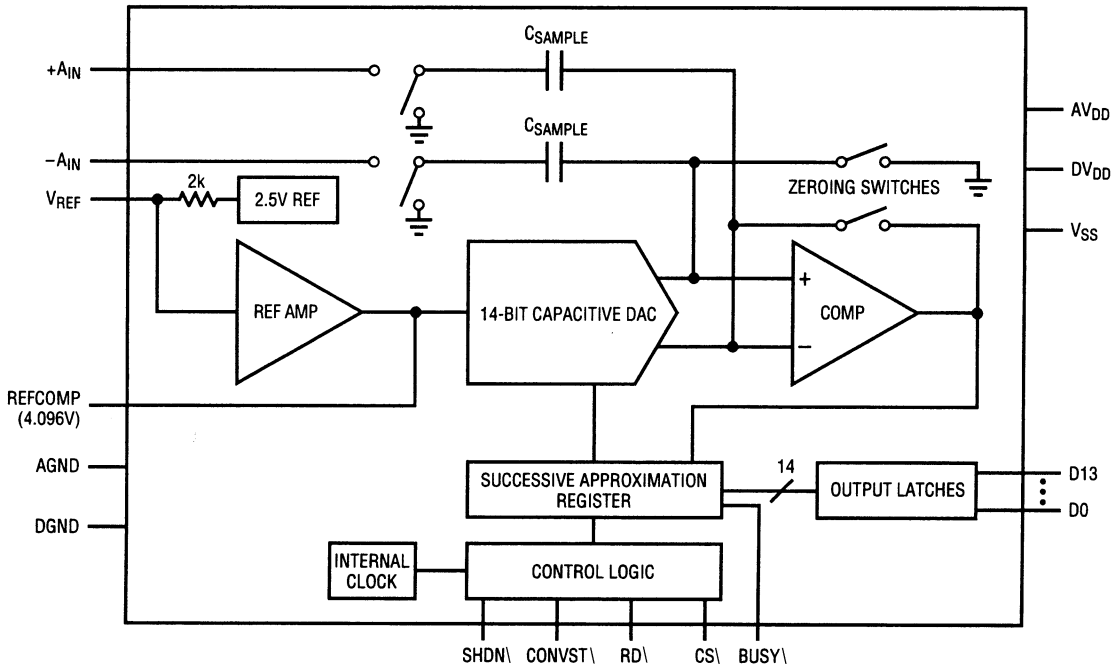
TIMING CHARACTERISTICS (* denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = +25°C.)[5]

PARAMETER	CONDITIONS		SYM	MIN	TYP	MAX	UNITS
Maximum Sampling Frequency		*	$f_{SAMPLE(MAX)}$	800			kHz
Conversion Time		*	t_{CONV}		950	1150	ns
Acquisition Time		*	t_{ACQ}		90	300	ns
Acquisition + Conversion Time		*	$t_{ACQ + CONV}$		1040	1250	ns
CS\ to RD\ Setup Time[9,10]		*	t_1	0			ns
CS\↓ to CONVST\↓ Setup Time[9,10]		*	t_2	40			ns
CS\↓ to SHDN\↓ Setup Time[9,10]			t_3	40			ns
SHDN\↑ to CONVST\↓ Wake-up Time[10]			t_4		400		ns
CONVST\ Low Time[10, 11]		*	t_5	40			ns
CONVST\ to BUSY\ Delay	C_L=25pF		t_6		20		ns
		*				50	ns
Data Ready Before BUSY\↑			t_7	20	50		ns
		*		15			ns
Delay Between Conversions[10]		*	t_8	40			ns
Wait Time RD\↓ After BUSY\↑[9]		*	t_9	-5			ns
Data Access Time After RD\↓	C_L=25pF		t_{10}		15	25	ns
		*				35	ns
	C_L=100pF				20	35	ns
		*				50	ns
Bus Relinquish Time			t_{11}		10	20	ns
	-40°C ≤ T_A < 85°C	*				30	ns
	-55°C ≤ T_A < 125°C	*				35	ns
RD\ Low Time		*	t_{12}	t_{10}			ns
CONVST\ High Time		*	t_{13}	40			ns

NOTES:

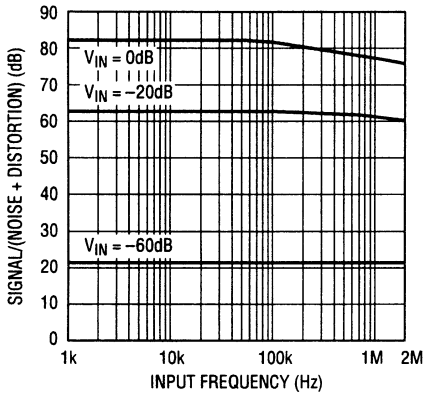
1. Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
2. All voltage values are with respect to ground with DGND and AGND wired together unless otherwise noted.
3. When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{DD} without latchup.
4. When these pin voltages are taken below V_{SS}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latchup. These pins are not clamped to V_{DD}.
5. $V_{DD} = 5V$, $V_{SS} = -5V$, $f_{SAMPLE} = 800kHz$, $t_r = t_f = 5ns$ unless otherwise specified.
6. Linearity, offset and full-scale specifications apply for a single ended $+A_{IN}$ input with $-A_{IN}$ grounded.
7. Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.
8. Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11.
9. Guaranteed by design, not subject to test.
10. Recommended operating conditions.
11. The falling edge of CONVST\ starts a conversion. If CONVST\ returns high at a critical point during the conversion it can create small errors. For best performance ensure that CONVST\ returns high either within 650ns after the start of the conversion or after BUSY\ rises.

FUNCTIONAL BLOCK DIAGRAM

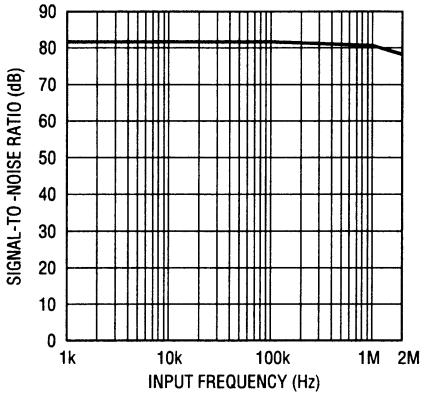


TYPICAL PERFORMANCE CHARACTERISTICS

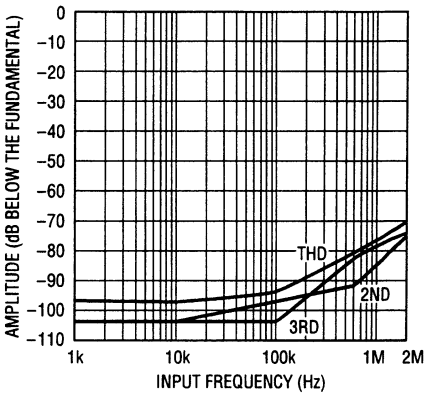
S/(N + D) vs Input Frequency and Amplitude



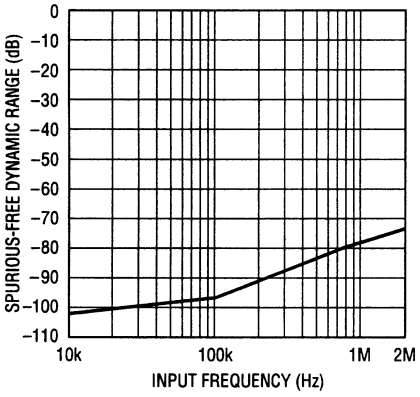
Signal-to-Noise Ratio vs Input Frequency



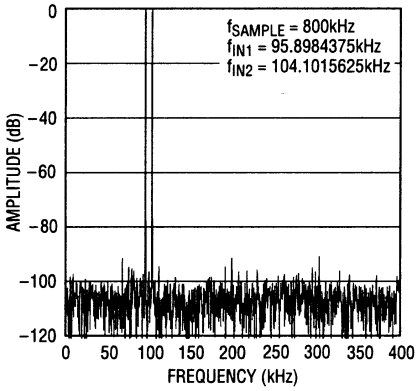
Distortion vs Input Frequency



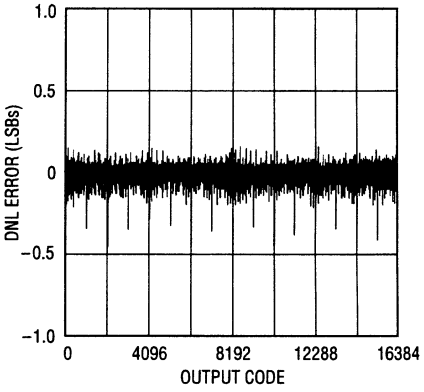
Spurious-Free Dynamic Range vs Input Frequency



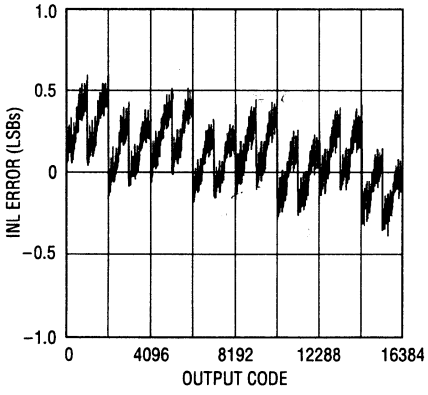
Intermodulation Distortion Plot



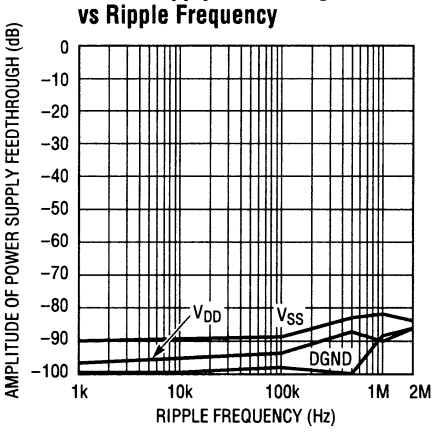
Differential Nonlinearity vs Output Code



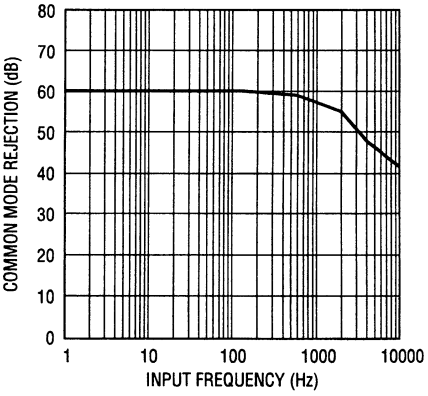
Integral Nonlinearity vs Output Code



Power Supply Feedthrough vs Ripple Frequency

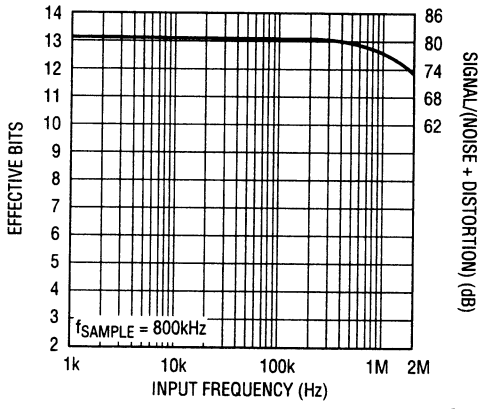


Input Common Mode Rejection vs Input Frequency



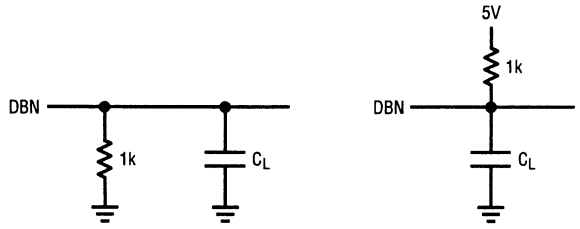
TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency



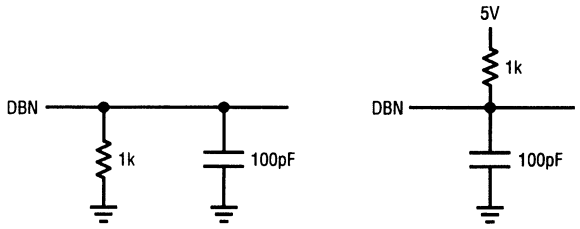
TEST CIRCUITS

Load Circuit for Access timings



(A) Hi-Z TO V_{OH} (B) Hi-Z TO V_O

Load Circuits for Output Float Delay



(A) V_{OH} TO Hi-Z (B) V_{OL} TO Hi-Z

PIN FUNCTIONS

+AIN (Pin 1): ±2.5V Positive Analog Input.

–AIN (Pin 2): ±2.5V Negative Analog Input.

VREF (Pin 3): 2.5V Reference Output. Bypass to AGND with 1µF.

REFCOMP (Pin 4): 4.06V Reference Output. Bypass to AGND with 10µF tantalum in parallel with 0.1µF or 10µF ceramic.

AGND (Pin 5): Analog Ground.

D13 to D6 (Pins 6 to 13): Three-State Data Outputs. The output format is 2's complement.

DGND (Pin 14): Digital Ground for Internal Logic. Tie to AGND.

D5 to D0 (Pins 15 to 20): Three-State Data Outputs. The output format is 2's complement.

SHDN\ (Pin 21): Power Shutdown Input. Low selects shutdown. Shutdown mode selected by CS\. CS\ = 0 for nap mode and CS\ = 1 for sleep mode.

RD\ (Pin 22): Read Input. This enables the output drivers when CS\ is low.

CONVST\ (Pin 23): Conversion Start Signal. This active low signal starts a conversion on its falling edge.

CS\ (Pin 24): Chip Select. The input must be low for the ADC to recognize CONVST\ and RD\ inputs. CS\ also sets the shutdown mode when SHDN\ goes low. CS\ and SHDN\ low select the quick wake-up nap mode. CS\ high and SHDN\ low select sleep mode.

BUSY\ (Pin 25): The BUSY\ output shows the converter status. It is low when a conversion is in progress. Data valid on the rising edge of BUSY\.

V_{SS} (Pin 26): – 5V Negative Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF or 10µF ceramic.

DV_{DD} (Pin 27): 5V Positive Supply. Short to Pin 28.

AV_{DD} (Pin 28): 5V Positive Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF or 10µF ceramic.

CONVERSION DETAILS

The AS1419 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 14-bit parallel output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs (please refer to Digital Interface section for the data format).

Conversion start is controlled by the CS\ and CONVST\ inputs. At the start of the conversion, the successive approximation register (SAR) is reset. Once a conversion cycle has begun, it cannot be restarted.

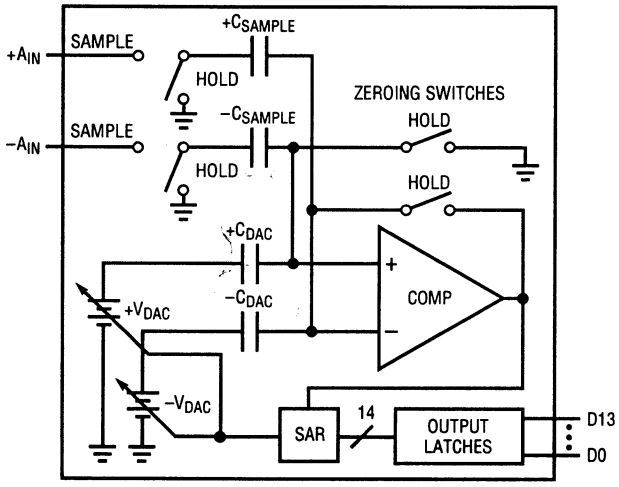


FIGURE 1: Simplified Block Diagram

During the conversion, the internal differential 14-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the $+A_{IN}$ and $-A_{IN}$ inputs are connected to the sample-and-hold capacitors (C_{SAMPLE}) during the acquire phase and the comparator offset is nulled by the zeroing switches. In this acquire phase, a minimum delay of 200ns will provide enough time for the sample-and-hold capacitors to acquire the analog signal. During the convert phase, the comparator zeroing switches open, putting the comparator into compare mode. The input switches the C_{SAMPLE} capacitors to ground, transferring the differential analog input charge onto the summing junction. This input charge is successively compared with the binary weighted charges supplied by the differential capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the differential DAC output balances the $+A_{IN}$ and $-A_{IN}$ input charges. The SAR contents (a 14-bit data word) which represents the difference of +AIN and –AIN are loaded into the 14-bit output latches.

DYNAMIC PERFORMANCE

The AS1419 has excellent high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2 shows a typical AS1419 FFT plot.

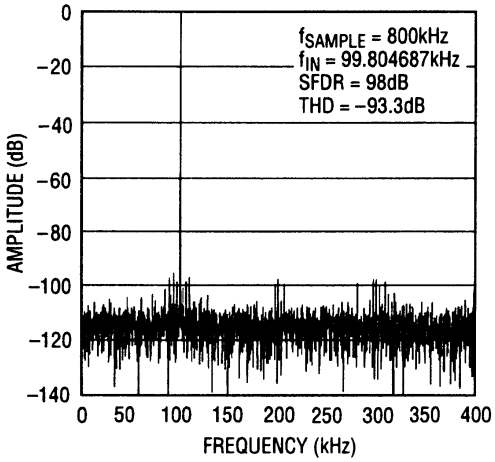


Figure 2a: AS1419 Nonaveraged, 4096 Point FFT, Input Frequency = 100kHz

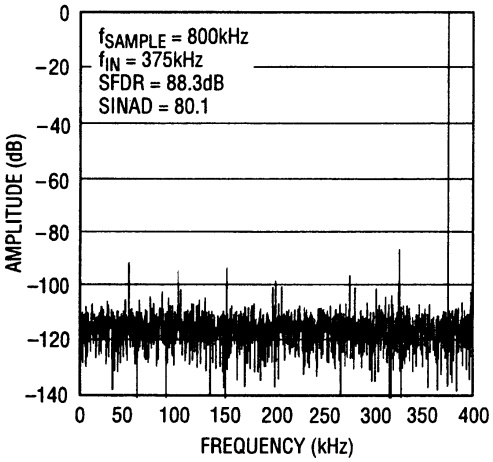


Figure 2b: AS1419 Nonaveraged, 4096 Point FFT, Input Frequency = 375kHz

Signal-to-Noise Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 2 shows a typical spectral content with a 800kHz sampling rate and a 100kHz input. The dynamic performance is excellent for input frequencies up to and beyond the Nyquist limit of 400kHz.

Effective Number of Bits

The effective number of bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) - 1.76]/6.02$$

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 800kHz, the AS1419 maintains near ideal ENOBs up to the Nyquist input frequency of 400kHz (refer to Figure 3).

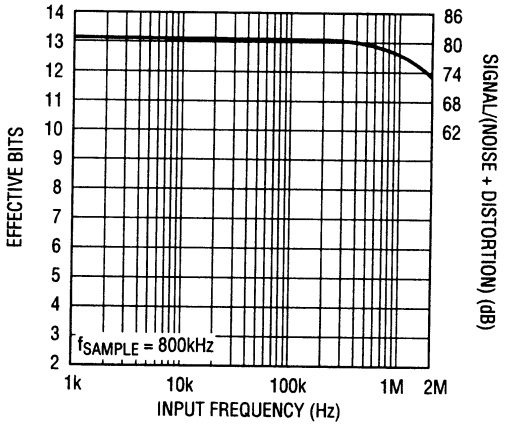


FIGURE 3: Effective Bits and Signal/ (Noise+Distortion) vs. Input Frequency

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20Log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots Vn^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. THD vs Input Frequency is shown in Figure 4. The AS1419 has good distortion performance up to the Nyquist frequency and beyond.

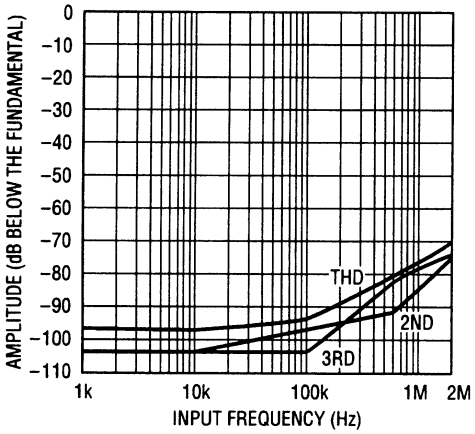


FIGURE 4: Distortion vs. Input Frequency

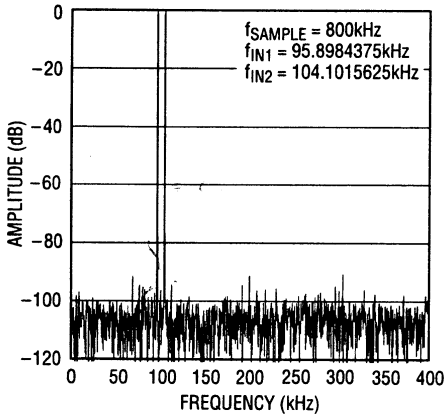


FIGURE 5: Intermodulation Distortion Plot

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ±nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD(fa+fb) = 20Log\frac{\text{Amplitude at } (fa+fb)}{\text{Amplitude at fa}}$$

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal.

The full-linear bandwidth is the input frequency at which the S/(N + D) has dropped to 77dB (12.5 effective bits). The AS1419 has been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist Frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

Driving the Analog Input

The differential analog inputs of the AS1419 are easy to drive. The inputs may be driven differentially or as a singleended input (i.e., the $-A_{IN}$ input is grounded). The $+A_{IN}$ and $-A_{IN}$ inputs are sampled at the same instant. Any unwanted signal that is common mode to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, then the AS1419 inputs can be driven directly. As source impedance increases so will acquisition time (see Figure 6). For minimum acquisition time with high source impedance, a buffer amplifier should be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 200ns for full throughput rate).

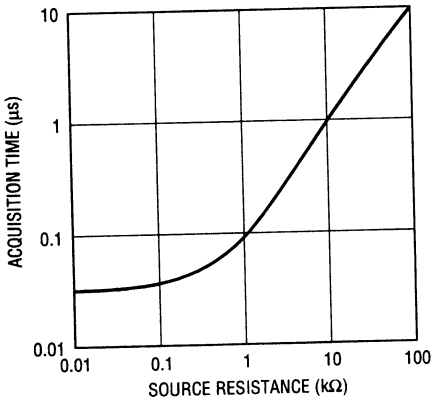


FIGURE 6: t_{ACQ} vs. Source Resistance

Input Filtering

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the AS1419 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 20MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For example, Figure 7 shows a 1000pF capacitor from $+A_{IN}$ to ground and a

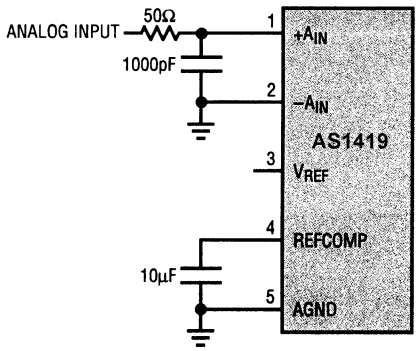


FIGURE 7: RC Input Filter

100Ω source resistor to limit the input bandwidth to 1.6MHz. The 1000pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling glitch sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can also generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Input Range

The ±2.5V input range of the AS1419 is optimized for low noise and low distortion. Most op amps also perform well over this same range, allowing direct coupling to the analog inputs and eliminating the need for special translation circuitry.

Some applications may require other input ranges. The AS1419 differential inputs and reference circuitry can accommodate other input ranges often with little or no additional circuitry. The following sections describe the reference and input circuitry and how they affect the input range.

Internal Reference

The AS1419 has an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.500V. It is connected internally to a reference amplifier and is available at V_{REF} (Pin 3) see Figure 8a. A 2k resistor is in series with the output so that it can be easily overdriven by an external reference or other circuitry, see Figure 8b. The reference amplifier gains the voltage at the V_{REF} pin by 1.625 to create the required internal reference voltage. This provides buffering between the V_{REF} pin and the high speed capacitive DAC. The reference amplifier compensation pin (REFCOMP, Pin 4) must be bypassed with a capacitor to ground. The reference amplifier is stable with capacitors of 1µF or greater. For the best noise performance, a 10µF ceramic or 10µF tantalum in parallel with a 0.1µF ceramic is recommended.

The V_{REF} pin can be driven with a DAC or other means shown in Figure 9. This is useful in applications where the peak input signal amplitude may vary. The input span of the ADC can then be adjusted to match the peak input signal, maximizing the signal-to-noise ratio. The filtering of the internal AS1419 reference amplifier will limit the bandwidth and settling time of this circuit. A settling time of 5ms should be allowed for after a reference adjustment.

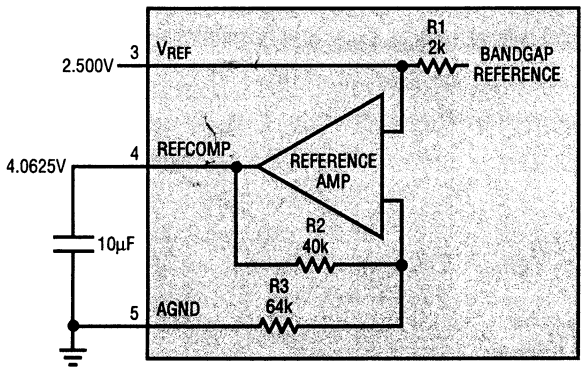


FIGURE 8a: AS1419 Reference Circuit

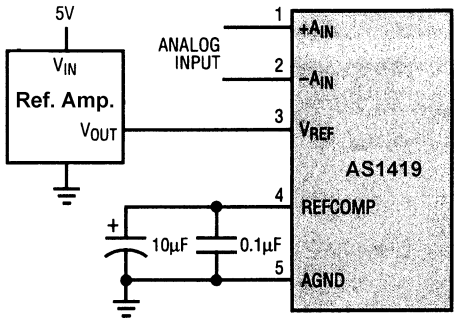


FIGURE 8b: Using an External Reference

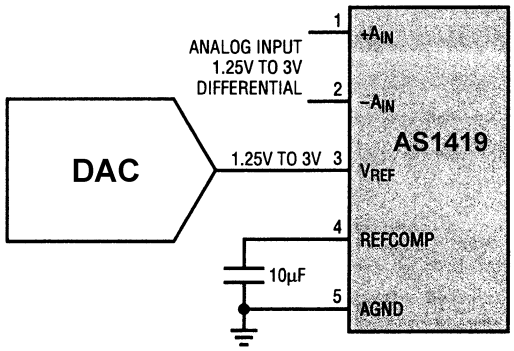


FIGURE 9: Driving V_{REF} with a DAC

Differential Inputs

The AS1419 has a unique differential sample-and-hold circuit that allows rail-to-rail inputs. The ADC will always convert the difference of $+A_{IN} - (-A_{IN})$ independent of the common mode voltage (see Figure 11a). The common mode rejection holds up to extremely high frequencies, see Figure 10a. The only requirement is that both inputs can not exceed the AV_{DD} or AV_{SS} power supply voltages. Integral nonlinearity errors (INL) and differential nonlinearity errors (DNL) are independent of the common mode voltage, however, the bipolar zero error (BZE) will vary. The change in BZE is typically less than 0.1% of the common mode voltage. Dynamic performance is also affected by the common mode voltage. THD will degrade as the inputs approach either power supply rail, from 86dB with a common mode of 0V to 76dB with a common mode of 2.5V or – 2.5V. Differential inputs allow greater flexibility for accepting different input ranges. Figure 10b shows a circuit that converts a 0V to 5V analog input signal with only an additional buffer that is not in the signal path.

Full-Scale and Offset Adjustment

Figure 11a shows the ideal input/output characteristics for the AS1419. The code transitions occur midway between successive integer LSB values (i.e., –FS + 0.5LSB, – FS + 1.5LSB, –FS + 2.5LSB,... FS – 1.5LSB, FS – 0.5LSB). The output is two's complement binary with 1LSB = FS – (– FS)/16384 = 5V/16384 = 305.2µV. In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 11b shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset applied to the –AIN input. For zero offset error, apply –152µV (i.e., – 0.5LSB) at $+A_{IN}$ and adjust the offset at the $-A_{IN}$ input until the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11. For full-scale adjustment, an input voltage of 2.499544V (FS/2 – 1.5LSBs) is applied to $+A_{IN}$ and R2 is adjusted until the output code flickers between 0111 1111 1111 10 and 0111 1111 1111 11.

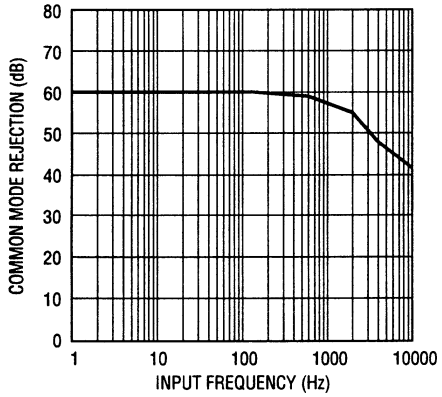


Figure 10a. CMRR vs Input Frequency

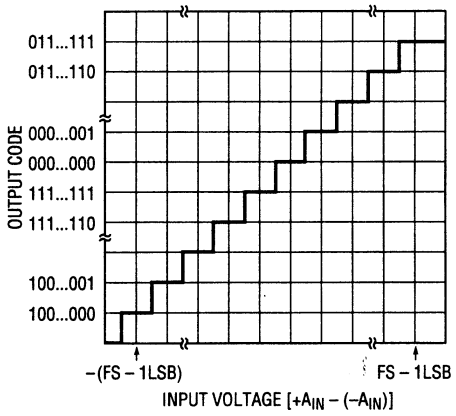


Figure 11a. AS1419 Transfer Characteristics

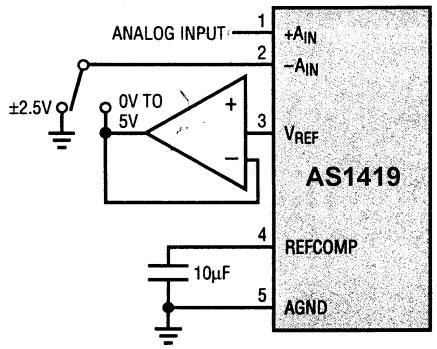


Figure 10b. Selectable 0V to 5V or ±2.5V Input Range

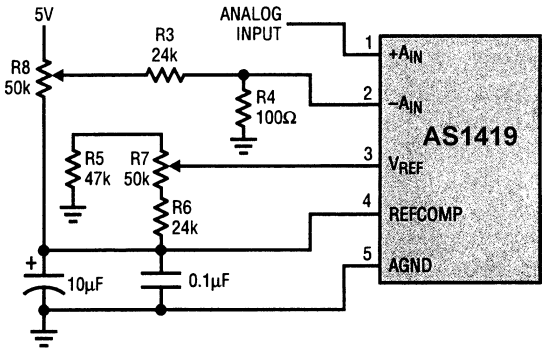


Figure 11b. Offset and Full-Scale Adjust Circuit

BOARD LAYOUT AND GROUNDING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the AS1419, a printed circuit board with ground plane is required. Layout should ensure that digital and analog signal lines are separated as much as possible. Particular care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.The analog input should be screened by AGND.

An analog ground plane separate from the logic system ground should be established under and around the ADC. Pin 5 (AGND), Pin 14 and Pin 19 (ADC's DGND) and all other analog grounds should be connected to this single analog ground point. The REFCOMP bypass capacitor and the DV_{DD} bypass capacitor should also be connected to this analog ground plane. No other digital grounds should be connected to this analog ground plane. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion or by using three-state buffers to isolate the ADC data bus. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The AS1419 has differential inputs to minimize noise coupling. Common mode noise on the $+A_{IN}$ and $-A_{IN}$ leads will be rejected by the input CMRR. The $-A_{IN}$ input can be used as a ground sense for the $+A_{IN}$ input; the AS1419 will hold and convert the difference voltage between $+A_{IN}$ and $-A_{IN}$. The leads to $+A_{IN}$ (Pin 1) and $-A_{IN}$ (Pin 2) should be kept as short as possible. In applications where this is not possible, the $+A_{IN}$ and $-A_{IN}$ traces should be run side by side to equalize coupling.

SUPPLY BYPASSING

High quality, low series resistance ceramic, 10µF bypass capacitors should be used at the V_{DD} and REFCOMP pins. Surface mount ceramic capacitors provide excellent bypassing in a small board space. Alternatively, 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors can be used. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

DIGITAL INTERFACE

The A/D converter is designed to interface with microprocessors as a memory mapped device. The CS\ and RD\ control inputs are common to all peripheral memory interfacing. A separate CONVST\ is used to initiate a conversion.

Internal Clock

The A/D converter has an internal clock that eliminates the need of synchronization between the external clock and the CS\ and RD\ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 0.95µs and a maximum conversion time over the full operating temperature range of 1.15µs. No external adjustments are required. The guaranteed maximum acquisition time is 300ns. In addition, a throughput time of 1.25µs and a minimum sampling rate of 800ksps are guaranteed.

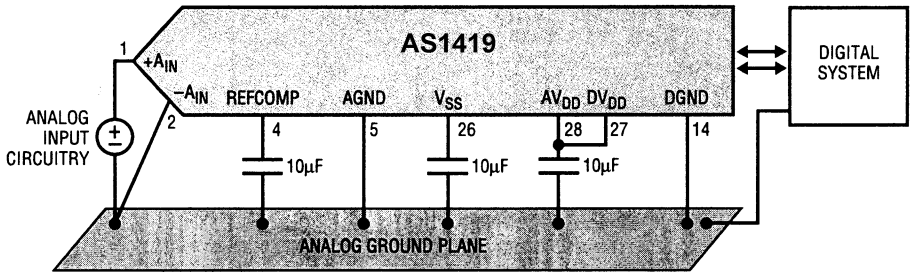


FIGURE 12: Power Supply Grounding Practice

Power Shutdown

The AS1419 provides two power shutdown modes, nap and sleep, to save power during inactive periods. The nap mode reduces the power by 95% and leaves only the digital logic and reference powered up. The wake-up time from nap to active is 400ns. In sleep mode, the reference is shut down and only a small current remains, about 250µA. Wake-up time from sleep mode is much slower since the reference circuit must power up and settle to 0.005% for full 14-bit accuracy. Sleep mode wake-up time is dependent on the value of the capacitor connected to the REFCOMP (Pin 4). The wake-up time is 10ms with the recommended 10µF capacitor. Shutdown is controlled by Pin 21 (SHDN\); the ADC is in shutdown when it is low. The shut-down mode is selected with Pin 20 (CS\); low selects nap.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: CONVST\, CS\ and RD\. A logic "0" applied to the CONVST\ pin will start a conversion after the ADC has been selected (i.e., CS\ is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the BUSY\ output. BUSY\ is low during a conversion.

Figures 16 through 20 show several different modes of operation. In modes 1a and 1b (Figures 16 and 17), CS\ and RD\ are both tied low. The falling edge of CONVST\ starts the conversion. The data outputs are always enabled and data can be latched with the BUSY\ rising edge. Mode 1a shows operation with a narrow logic low CONVST\ pulse. Mode 1b shows a narrow logic high CONVST\ pulse.

In mode 2 (Figure 18), CS\ is tied low. The falling edge of the CONVST\ signal again starts the conversion. Data outputs are in three-state until read by the MPU with the RD\ signal. Mode 2 can be used for operation with a shared MPU databus.

In slow memory and ROM modes (Figures 19 and 20), CS\ is tied low and CONVST\ and RD\ are tied together. The MPU starts the conversion and reads the output with the RD\ signal. Conversions are started by the MPU or DSP (no external sample clock).

In slow memory mode, the processor applies a logic low to RD\ (= CONVST\), starting the conversion. BUSY\ goes low, forcing the processor into a WAIT state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; BUSY\ goes high, releasing the processor and the processor takes RD\ (= CONVST\) back high and reads the new conversion data.

In ROM mode, the processor takes RD\ (= CONVST\) low, starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.

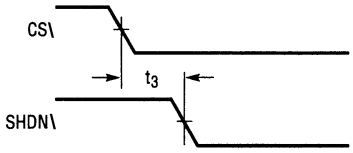


FIGURE 14a: CS\ to SHDN\ Timing

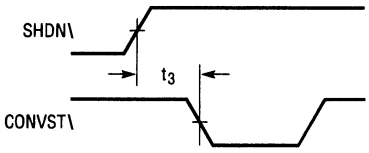


FIGURE 14a: SHDN\ to CONVST\ Wake-Up Timing

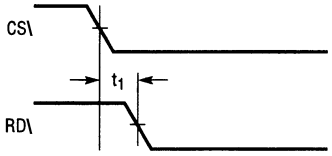


FIGURE 15: CS\ to CONVST\ Set-Up Timing

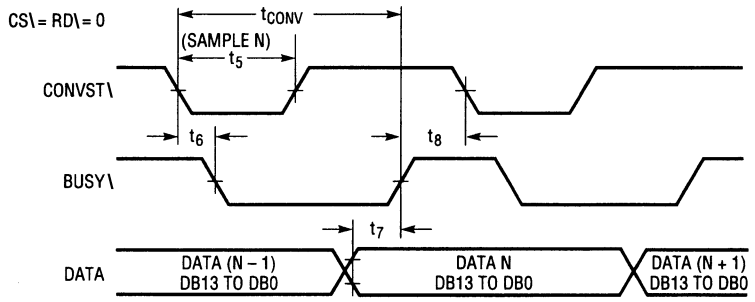


FIGURE 16: Mode 1a. CONVST\ Starts a Conversion. Data Outputs Always Enabled. (CONVST\ = ⎍⎍⎍)

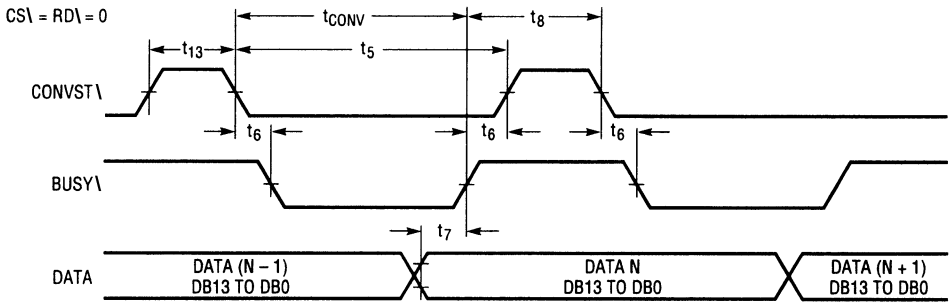


Figure 17. Mode 1b. CONVST\ Starts a Conversion. Data Outputs Always Enabled (CONVST\ = ⎍⎍⎍)

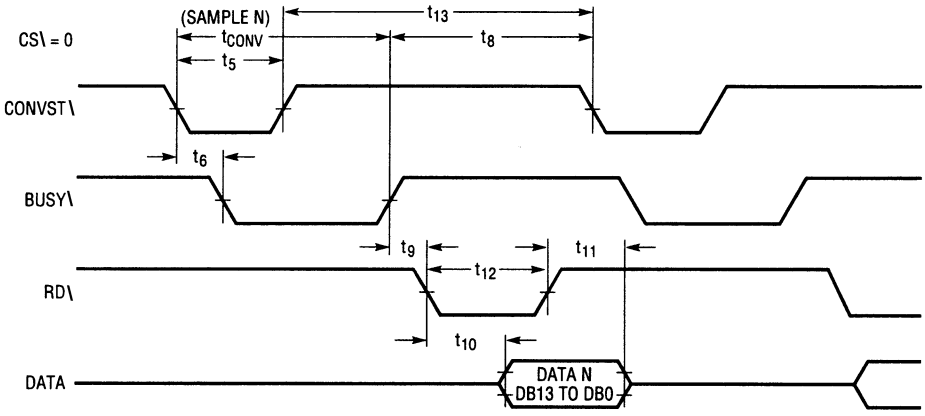


Figure 18. Mode 2. CONVST\ Starts a Conversion. Data is Read by RD

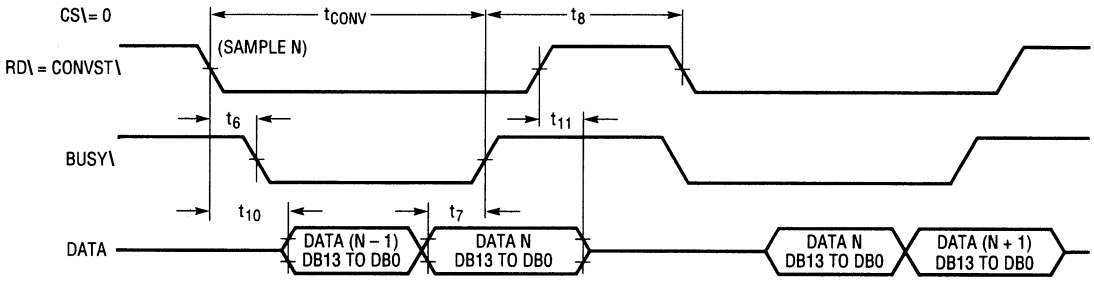


Figure 19. Slow Memory Mode Timing

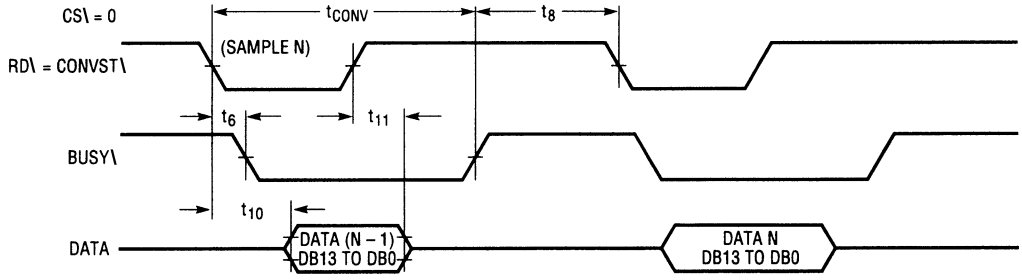
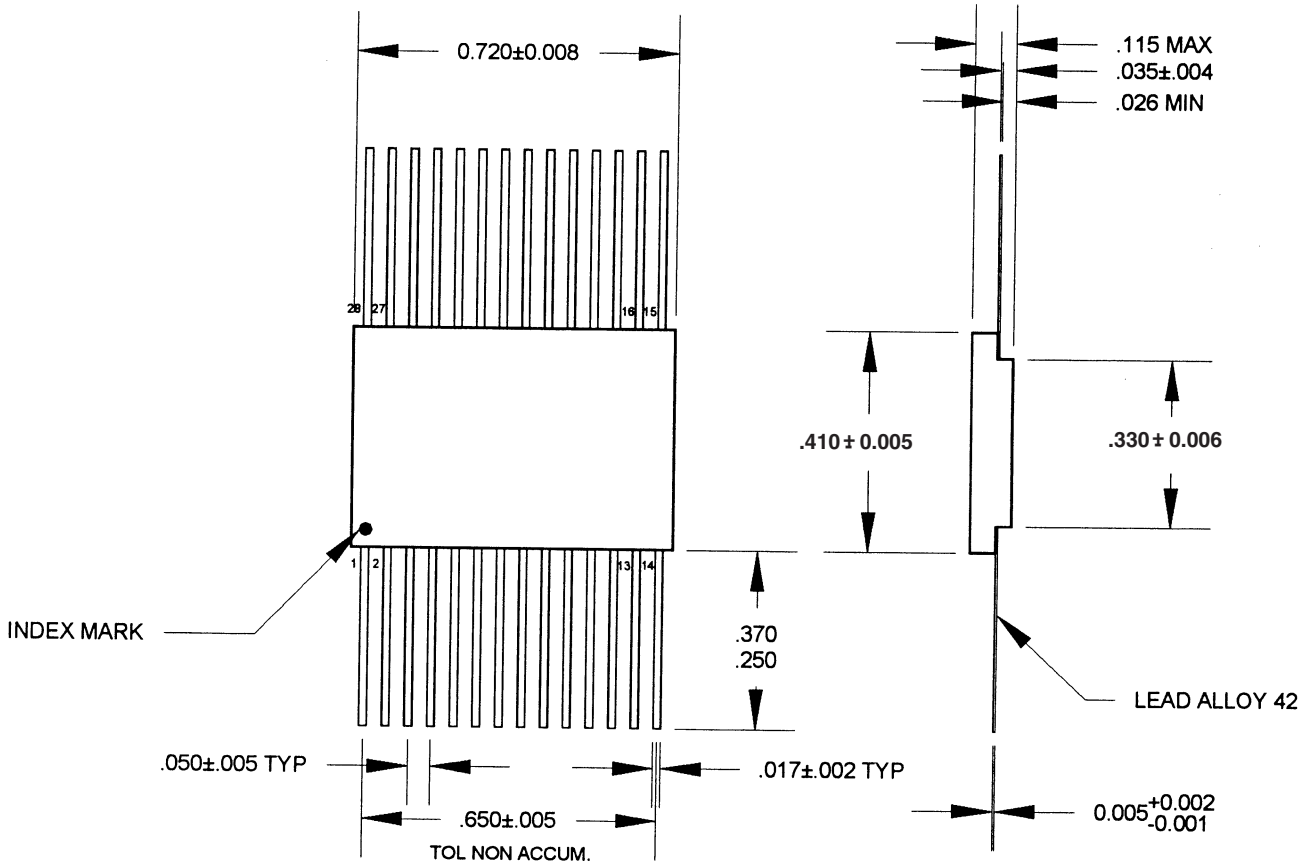


Figure 20. ROM Mode Timing

MECHANICAL DEFINITIONS*

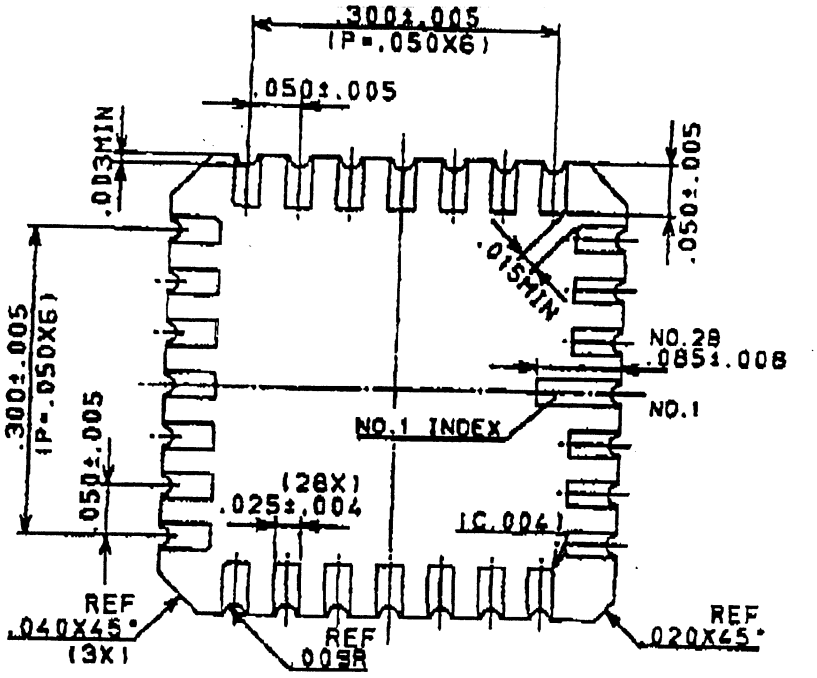
28-Pin Flat Pack
(Package Designator F)



**All measurements are in inches.*

MECHANICAL DEFINITIONS*

28-Pin LCC Package
(Package Designator ECA)



**All measurements are in inches.*

ORDERING INFORMATION

EXAMPLE: AS1419F-SPACE

Device Number	Package Type	Operating Temp.
AS1419	F	-*
AS1419A	F	-*

EXAMPLE: AS1419AECA-883C

Device Number	Package Type	Operating Temp.
AS1419	ECA	-*
AS1419A	ECA	-*

***AVAILABLE PROCESSES**

XT = Extended Temperature Range	-55°C to +125°C
IT = Industrial Temperature Range	-40°C to +85°C
MIL = Military Processing	-55°C to +125°C
SPACE = Space Processing**	-55°C to +125°C

**As defined by individual customer Source Control Drawing (SCD)*

DOCUMENT TITLE

14 Bit, 800ksps Sampling, A/D Converter with Shutdown

REVISION HISTORY

Rev #	History	Release Date	Status
1.0	Changed text on pg 2, Changed power requirement on pg 4 to 1.5	2/05	Release
1.3	Updated drawing Specifications	5/05	Release
1.4	Updated Timing Characteristics	7/08	Release
1.5	Added SCD note under Space Option Page 1 & 19	8/09	Release