

rev 1.0

## μP Supervisory Circuit

### **General Description**

The ASM161 and ASM162 are cost effective, low power supervisory circuits that monitor power supplies in microprocessor, microcontroller and digital systems. If the power supply drops below the reset threshold level, a reset is asserted and remains asserted for atleast 800ms after  $V_{CC}$  has risen above the reset threshold. An improved manual reset architecture gives the system designer additional flexibility.

The debounced manual reset input is negative edge triggered. The reset pulse period generated by a  $\overline{\text{MR}}$  transition is a minimum of 800 ms and a maximum of 2 sec duration. In addition, The  $\overline{\text{MR}}$  input signal is blocked for an additional 49µS minimum after the reset pulse ends. During the  $\overline{\text{MR}}$  disable period, the microcontroller is guaranteed a time period free of additional manual reset signals. During this period DRAM contents can be refreshed or other critical system tasks undertaken. Low power consumption makes the ASM161/162 ideal for use in portable and battery operated equipments. With 3V supplies power consumption is 8µW typically and 30µW maximum. The ASM161 has an open-drain, active-LOW RESET output and requires an external pull-up resistor. The ASM162 has an active HIGH RESET output.

The ASM161/162 are offered in compact 4-pin SOT-143 packages. No external components are required to trim threshold voltage for monitoring different supply voltages. With six different factory set, reset, threshold ranges from 2.63V to 4.63V, the ASM161/162 are suitable for monitoring 5V, 3.6V and 3.0V supplies. The ASM161/162 are available in temperature ranges 0° to 70°c and -40°c to +85°c.

Reset Threshold					
Part Suffix Voltage (V)					
L	4.63				
M	4.38				
J	4.00				
Т	3.08				
S	2.93				
R	2.63				

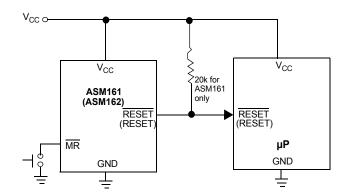
## **Key Features**

- · Edge triggered manual reset input
- single pulse output
- 49µS minimum MR disable period after reset
- CMOS/TTL logic or switch interface
- Debounced input
- Low supply current extends battery life
  - 6μA / 15μA typ/max at 5.5V
  - 4.5μA / 10μA typ/max at 3.6V
- Long reset period
  - 0.8 sec minimum, 2 sec maximum
- Two reset polarity options
  - ASM161: Active LOW, open-drain
  - ASM162: Active HIGH
- Pinout matches the AS811/812
- Small 4-Pin SOT-143 package
- Two temperature ranges: 0<sup>0</sup> to 70<sup>0</sup>c and -40<sup>0</sup>c to +85<sup>0</sup>c

### **Applications**

- PDAs
- Appliances
- · Computers and embedded controllers
- · Wireless communication systems
- Battery operated and intelligent instruments
- Automotive systems
- Safety systems

## **Typical Operating Circuit**

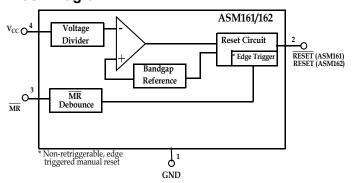


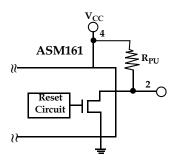
## October 2003



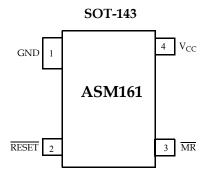
### rev 1.0

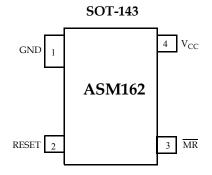
## **Block Diagram**





## **Pin Configuration**





RESET is open drain

## **Pin Description**

Pin	n #	Pin Name	Description
ASM161	ASM162	Pili Name	Description
1	1	GND	Ground.
2	-	RESET	Active-LOW, open-drain reset output. $\overline{\text{RESET}}$ remains LOW while $V_{CC}$ is below the reset threshold and for 800ms minimum after $V_{CC}$ rises above the reset threshold. An external pull-up resistor is needed.
-	2	RESET	Active HIGH reset output. RESET remains HIGH while $V_{CC}$ is below the reset threshold and for 800ms after $V_{CC}$ rises above the reset threshold.
3	3	MR	Manual reset input. A negative going edge transition on $\overline{\text{MR}}$ asserts reset. Reset remains asserted for one reset time-out period (800 ms min). This active-LOW input has an internal pull-up resistor. It can be driven from a TTL or CMOS logic line or shorted to ground with a switch. Leave open if unused.
4	4	V <sub>CC</sub>	Power supply input voltage.





#### rev 1.0

### **Detailed Descriptions**

The reset function ensures the microprocessor is properly reset and powers up into a known condition after a power failure.

#### **Reset Timing**

A reset is generated whenever the supply voltage is below the threshold level ( $V_{CC} < V_{TH}$ ). The reset duration is at least 800ms after  $V_{CC}$  has risen above the reset threshold and is guaranteed to be no more than 2 seconds. The rest signal remains active as long as the monitored supply voltage is below the internal threshold voltage.

The ASM161 has an open-drain, active LOW  $\overline{\text{RESET}}$  output (which is guaranteed to be in the correct state for  $V_{CC}$  down to 1.1 V). The ASM161 uses an external pull-up resistor. Output leakage current is under 1 $\mu$ A. A high resistance value can be used to minimize current drain.

The ASM162 generates an active-HIGH RESET output.

Part Number	Reset Polarity		
ASM161	LOW (use external pull-up resistor)		
ASM162	HIGH		

#### **Manual Reset**

The ASM161/162 have a unique manual reset circuit. A negative going edge transition on  $\overline{\text{MR}}$  initiates the reset. A manual reset generates a single reset pulse of fixed length. The output-reset pulse remains asserted for the Reset Active Time-Out Period  $t_{RP}$  and then clears. Once the reset pulse is completed, the  $\overline{\text{MR}}$  input remains disabled for at least 49µS but not more than 122µS. This period is specified as  $t_{MRD}$ .

During the  $\overline{\text{MR}}$  disabled period, the microcontroller is guaranteed a time period free of new manual reset signals. This period can be used to refresh critical DRAM contents or other system tasks.

The  $\overline{\text{MR}}$  pin must be taken HIGH and LOW again after the  $t_{\text{MRD}}$  period has been completed to initiate another reset pulse.

The manual reset input has an internal  $20k\Omega$  pull-up resistor.  $\overline{MR}$  can be left open if not used.

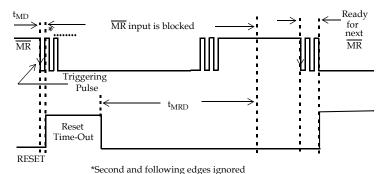


Figure 1: Manual Reset Timing

## **Application Information**

### **Glitch Resistance**

The ASM161/162 are relatively immune to short duration negative-going  $V_{CC}$  transients/glitches. A  $V_{CC}$  transient that goes 100mV below the reset threshold and lasts 20s or less will not typically cause a reset pulse.

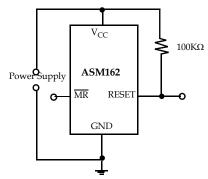


Figure 2: RESET valid with VCC under 1.1V

#### Valid Reset with VCC under 1.1V

To ensure that logic inputs connected to the ASM162 RESET pin are in a known state when  $V_{CC}$  is under 1.1V, a  $100k\Omega$  pull-down resistor at RESET is needed. The value is not critical.

This scheme does not work with the open-drain outputs of ASM161.



rev 1.0

## **Absolute Maximum Ratings**

Parameter	Min	Max	Unit
Pin Terminal Voltage with respect to Ground			
V <sub>cc</sub>	-0.3	6.0	V
RESET, RESET and MR	-0.3	V <sub>CC</sub> + 0.3	V
Input Current at V <sub>CC</sub> and MR		20	mA
Rate of Rise at V <sub>CC</sub>		100	V/µs
Power Dissipation (T <sub>A</sub> = 70°C)		320	mW
Operating Temperature Range	-40	85	°C
Storage Temperature Range	-65	160	°C
Lead Temperature (soldering, 10 sec)		300	°C

Note: These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability.



rev 1.0

### **Electrical Characteristics**

Unless otherwise noted,  $V_{CC}$  is over the full range and TA =  $0^{0}$  to  $70^{0}$ c for ASM161/162 X C and  $T_{A}$  =  $-40^{0}$ c to  $+85^{0}$ c for ASM161/162 X E devices. Typical values at  $T_{A}$  =  $25^{0}$ c,  $V_{CC}$  = 5V for L/M/J devices,  $V_{CC}$  = 3.3V for T/S devices and  $V_{CC}$  = 3V for R devices

Parameter	Symbol	Conditions		Min	Тур	Max	Unit	
Input Voltage (V <sub>CC</sub> ) Range	V <sub>CC</sub>	T <sub>A</sub> = 0°C to 70°C		1.1		5.5	V	
Supply Current	I <sub>CC</sub>	$T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C},$ $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	V <sub>CC</sub> < 5.5V, L/M/J		6	15	μA	
(Unloaded)	icc	$T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C},$ $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	V <sub>CC</sub> < 3.6V, R/S/T		4.5	10	μΑ	
		L Devices	T <sub>A</sub> = 25°C	4.56	4.63	4.70		
			Note 1	4.50		4.75		
		M devices	T <sub>A</sub> = 25°C	4.31	4.38	4.45		
			Note 1	4.25		4.50		
		J devices	T <sub>A</sub> = 25°C	3.93	4.00	4.06		
Reset Threshold	V		Note 1	Note 1 3.89	4.10	V		
Reset Tilleshold	V <sub>TH</sub>	T devices	T <sub>A</sub> = 25°C	3.04	3.08	3.11	V	
			Note 1	3.00		3.15		
		S devices	T <sub>A</sub> = 25°C	2.89	2.93	2.96		
			Note 1	2.85		3.00		
		R devices	T <sub>A</sub> = 25°C	2.59	2.63	2.66		
			Note 1	2.55		2.70		
Reset Threshold Temp Coefficient	T <sub>CVTH</sub>				30		ppm/ °C	
V <sub>CC</sub> to reset delay		$V_{CC} = V_{TH}$ to $(V_{TH} - 100 \text{mV})$			20		μS	
Reset Pulse Width	t <sub>RPW</sub>	T <sub>A</sub> = 0°C to 70°C		800	1400	2000		
		T <sub>A</sub> = -40°C to 85°C		560		2240	ms	
MR Minimum Pulse Width	t <sub>MR</sub>			10			μS	
MR Glitch Immunity					100		ns	
MR to RESET Propagation Delay	t <sub>MD</sub>				0.5		μs	

## October 2003



### rev 1.0

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
-	V <sub>IH</sub>	V <sub>CC</sub> > V <sub>TH</sub> (MAX), L/M/J devices	2.3			V
	V <sub>IL</sub>	VCC > VTH(IVIAX), E/IVI/O devices			0.8	V
MR Input Threshold	V <sub>IH</sub>		0.7V <sub>CC</sub>			V
	V <sub>IL</sub>	V <sub>CC</sub> > V <sub>TH</sub> (MAX), R/S/T devices			0.25V <sub>CC</sub>	V
MR Delay to MR Retrig-		T <sub>A</sub> = 0°C to 70°C	49	85	122	0
ger	t <sub>MRD</sub>	T <sub>A</sub> = -40°C to 85°C		85		μS
MR pull-up resistance			10	20	30	ΚΩ
	olt- V <sub>OL</sub>	V <sub>CC</sub> = V <sub>TH</sub> min., I <sub>SINK</sub> = 1.2mA, ASM161 R/S/T			0.3	
Low RESET output voltage (ASM161)		$V_{CC} = V_{TH} \text{ min., } I_{SINK} = 3.2\text{mA},$ ASM161 L/M/J			0.4	V
		$V_{CC} > 1.1$ , $I_{SINK} = 50 \mu A$			0.3	
RESET Output Leak- age Current (ASM161)	I <sub>LKG</sub>	$V_{DRAIN} \le 6.0V$ , $0^{\circ}C \le T_A \le 70^{\circ}C$			1	μΑ
Low RESET output voltage (ASM162)	V <sub>OL</sub>	$V_{CC} = V_{TH} \text{ min., } I_{SINK} = 1.2\text{mA},$ ASM162 R/S/T			0.3	V
	▼ OL	V <sub>CC</sub> = V <sub>TH</sub> min., I <sub>SINK</sub> = 3.2mA, ASM162 L/M/J			0.4	v
HIGH RESET Output Voltage (ASM162)	V <sub>OH</sub>	1.8 <v<sub>CC<v<sub>THmin., I<sub>SOURCE</sub> = 150 μA</v<sub></v<sub>	0.8V <sub>CC</sub>			V

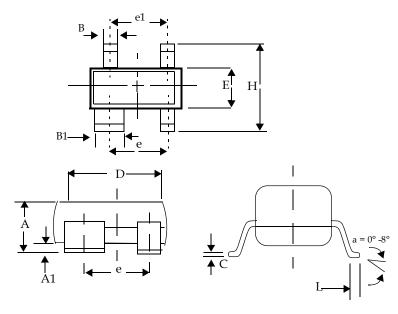
Notes: 1. Over operating temperature range.



### rev 1.0

# **Package Dimensions**

## Plastic SOT - 143 (4Pin)



Plastic SOT - 143 (4 pin)

	Incl	nes	Millimeters		
	Min	Max	Min	Max	
	Plastic	SOT-143	(4-Pin)		
Α	0.031	0.047	0.787	1.194	
A1	0.001	0.005	0.025	0.127	
В	0.014	0.022	0.356	0.559	
B1	0.030	0.038	0.762	0.965	
С	0.0034	0.006	0.086	0.152	
D	0.105	0.120	2.667	3.048	
Е	0.047	0.055	1.194	1.397	
е	0.070	0.080	1.778	2.032	
e1	0.071	0.079	1.803	2.007	
Н	0.082	0.098	2.083	2.489	
L	0.004	0.012	0.102	0.305	



rev 1.0 **Ordering Information** 

Part Number <sup>1</sup>	Reset Threshold (V)	Temperature Range (°C)	Pin-Package	Package Marking (XX Lot Code)
ASM161LCUS/T	4.63	0 TO 70	4-SOT-143	TAXX
ASM161MCUS/T	4.38	0 TO 70	4-SOT-143	TBXX
ASM161JCUS/T	4.00	0 TO 70	4-SOT-143	TCXX
ASM161TCUS/T	3.08	0 TO 70	4-SOT-143	TDXX
ASM161SCUS/T	2.93	0 TO 70	4-SOT-143	TEXX
ASM161RCUS/T	2.63	0 TO 70	4-SOT-143	TFXX
ASM162LCUS/T	4.63	0 TO 70	4-SOT-143	TGXX
ASM162MCUS/T	4.38	0 TO 70	4-SOT-143	THXX
ASM162JCUS/T	4.00	0 TO 70	4-SOT-143	TIXX
ASM162TCUS/T	3.08	0 TO 70	4-SOT-143	TJXX
ASM162SCUS/T	2.93	0 TO 70	4-SOT-143	TKXX
ASM162RCUS/T	2.63	0 TO 70	4-SOT-143	TLXX
ASM161LEUS/T	4.63	-40 TO 85	4-SOT-143	TMXX
ASM161MEUS/T	4.38	-40 TO 85	4-SOT-143	TNXX
ASM161JEUS/T	4.00	-40 TO 85	4-SOT-143	TOXX
ASM161TEUS/T	3.08	-40 TO 85	4-SOT-143	TPXX
ASM161SEUS/T	2.93	-40 TO 85	4-SOT-143	TQXX
ASM161REUS/T	2.63	-40 TO 85	4-SOT-143	TRXX
ASM162LEUS/T	4.63	-40 TO 85	4-SOT-143	TSXX
ASM162MEUS/T	4.38	-40 TO 85	4-SOT-143	TTXX
ASM162JEUS/T	4.00	-40 TO 85	4-SOT-143	TUXX
ASM162TEUS/T	3.08	-40 TO 85	4-SOT-143	TVXX
ASM162SEUS/T	2.93	-40 TO 85	4-SOT-143	TWXX
ASM162REUS/T	2.63	-40 TO 85	4-SOT-143	TXXX

Notes: 1. Tape and Reel packaging is indicated by the /T designation.





Alliance Semiconductor Corporation 2575, Augustine Drive, Santa Clara, CA 95054 Tel: 408 - 855 - 4900

Fax: 408 - 855 - 4999

www.alsc.com

Copyright © Alliance Semiconductor All Rights Reserved Part Number: ASM161 / ASM162 Document Version: 1.0

© Copyright 2003 Alliance Semiconductor Corporation. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warrantee to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems