Dual 12-Bit, High Bandwidth, Multiplying DAC with 4-Quadrant Resistors and Parallel Interface

AD5405

FEATURES

On chip 4-quadrant resistors allow flexible output ranges
10 MHz multiplying bandwidth
Fast parallel interface write cycle: 58 MSPS
2.5 V to 5.5 V supply operation
±10 V reference input
Extended temperature range: −40°C to 125°C
40-lead LFCSP package
Guaranteed monotonic
4-quadrant multiplication
Power-on reset
Readback function
.5 µA typical current consumption

APPLICATIONS

Portable battery-powered applications
Waveform generators
Analog processing
Instrumentation applications
Programmable amplifiers and attenuators
Digitally-controlled calibration
Programmable filters and oscillators
Composite video
Ultrasound
Gain, offset, and voltage trimming

GENERAL DESCRIPTION

The AD5405[1] is a dual CMOS, 12-bit, current output digital-to-analog converter (DAC).This device operates from a 2.5 V to 5.5 V power supply, making it suited to battery-powered and other applications.

The applied external reference input voltage (V_{REF}) determines the full-scale output current. An integrated feedback resistor (R_{FB}) provides temperature tracking and full-scale voltage output when combined with an external I-to-V precision amplifier. This device also contains all the 4-quadrant resistors necessary for bipolar operation and other configuration modes.

This DAC utilizes data readback, allowing the user to read the contents of the DAC register via the DB pins. On power-up, the internal register and latches are filled with zeros and the DAC outputs are at zero scale.

As a result of manufacture with a CMOS submicron process, the device offers excellent 4-quadrant multiplication characteristics, with large signal multiplying bandwidths of up to 10 MHz.

The AD5405 has a 6 mm × 6 mm, 40-lead LFCSP package.

[1] US Patent Number 5,689,257.

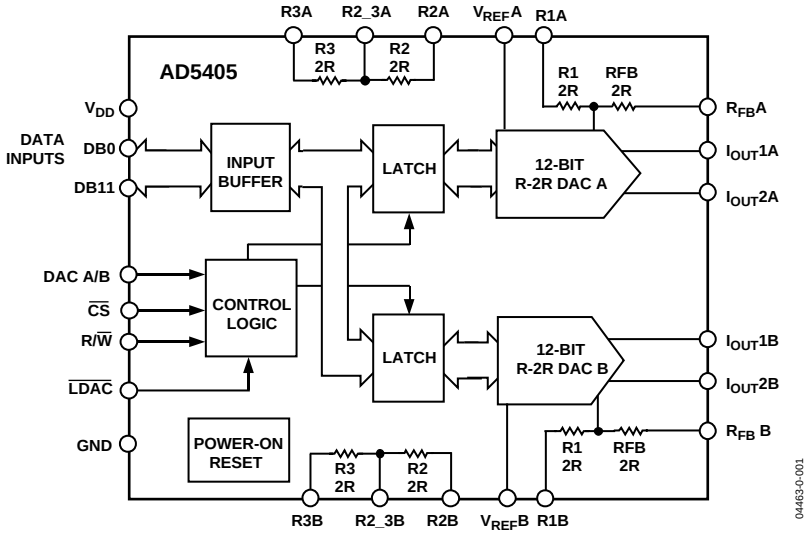

Figure 1. AD5405 Functional Block Diagram

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

REVISION HISTORY

7/04—Revision 0: Initial Version

SPECIFICATIONS[1]

V_{DD} = 2.5 V to 5.5 V, $V_{REF}A = V_{REF}B$ = 10 V, $I_{OUT}2$ = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. DC performance measured with OP1177, AC performance with AD9631, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions
STATIC PERFORMANCE					
Resolution			12	Bits	
Relative Accuracy			±1	LSB	
Differential Nonlinearity			−1/+2	LSB	Guaranteed monotonic
Gain Error			±25	mV	
Gain Error Temp Coefficient[2]		±5		ppm FSR/°C	
Bipolar Zero-Code Error			±25	mV	
Output Leakage Current			±1	nA	Data = 0x0000, T_A = 25°C, $I_{OUT}1$
			±10	nA	Data = $0x0000_H$, $I_{OUT}1$
REFERENCE INPUT					Typical resistor TC = −50 ppm/°C
Reference Input Range		±10		V	
$V_{REF}A$, $V_{REF}B$ Input Resistance	8	10	12	kΩ	DAC input resistance
$V_{REF}A$ to $V_{REF}B$ Input Resistance Mismatch		1.6	2.5	%	Typ = 25°C, Max = 125°C
R_1, R_{FB} Resistance	16	20	24	kΩ	
R_2, R_3 Resistance	16	20	24	kΩ	
R_2 to R_3 Resistance Mismatch		.06	.18	%	Typ = 25°C, Max = 125°C
DIGITAL INPUTS/OUTPUT					
Input High Voltage, V_{IH}	1.7			V	V_{DD} = 2.5 V to 5.5 V
Input Low Voltage, V_{IL}			0.8	V	V_{DD} = 2.7 V to 5.5 V
			0.7	V	V_{DD} = 2.5 V to 2.7 V
Input Leakage Current, I_{IL}			1	µA	
Input Capacitance			10	pF	
V_{DD} = 4.5 V to 5.5 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Output High Voltage, V_{OH}	V_{DD} − 1			V	I_{SOURCE} = 200 µA
V_{DD} = 2.5 V to 3.6 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Output High Voltage, V_{OH}	V_{DD} −0.5			V	I_{SOURCE} = 200 µA
DYNAMIC PERFORMANCE					
Reference Multiplying BW		10		MHz	V_{REF} = 5 V pk-pk, DAC loaded all 1s
Output Voltage Settling Time		80	120	ns	Measured to ±1 mV of FS. R_{LOAD} = 100 Ω, C_{LOAD} =15 pF. DAC latch alternately loaded with 0s and 1s.
Digital Delay		20	40	ns	
Digital-to-Analog Glitch Impulse		3		nV-s	1 LSB change around major carry, V_{REF} = 0 V
Multiplying Feedthrough Error			−75	dB	DAC latch loaded with all 0s. Reference = 10 kHz
Output Capacitance			2	pF	DAC latches loaded with all 0s
			4	pF	DAC latches loaded with all 1s
Digital Feedthrough		5		nV-s	Feedthrough to DAC output with $\overline{CS}$ high and alternate loading of all 0s and all 1s
Total Harmonic Distortion		−75		dB	V_{REF} = 5 V p-p, all 1s loaded, f = 1 kHz
		−75		dB	V_{REF} = 5 V, sine wave generated from digital code
Output Noise Spectral Density		25		nV/√Hz	@ 1 kHz

Parameter	Min	Typ	Max	Unit	Conditions
SFDR Performance (Wideband)					
Clock = 10 MHz					
500 kHz f_{OUT}		55		dB	
100 kHz f_{OUT}		63		dB	
50 kHz f_{OUT}		65		dB	
Clock = 25 MHz					
500 kHz f_{OUT}		50		dB	
100 kHz f_{OUT}		60		dB	
50 kHz f_{OUT}		62		dB	
SFDR Performance (Narrow Band)					
Clock = 10 MHz					
500 kHz f_{OUT}		73		dB	
100 kHz f_{OUT}		80		dB	
50k Hz f_{OUT}		87		dB	
Clock = 25 MHz					
500 kHz f_{OUT}		70		dB	
100 kHz f_{OUT}		75		dB	
50k Hz f_{OUT}		80		dB	
Intermodulation Distortion					
Clock = 10 MHz					
f_1 = 400 kHz, f_2 = 500 kHz		65		dB	
f_1 = 40 kHz, f_2 = 50 kHz		72		dB	
Clock = 25 MHz					
f_1 = 400 kHz, f_2 = 500 kHz		51		dB	
f_1 = 40 kHz, f_2 = 50 kHz		65		dB	
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I_{DD}			10	µA	Logic inputs = 0 V or V_{DD}
Power Supply Sensitivity			0.001	%/%	ΔV_{DD} = ±5%

[1] Temperature range for Y version is –40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

TIMING CHARACTERISTICS

V_{DD} = 2.5 V to 5.5 V, V_{REF} = 5 V, $I_{OUT}2$ = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
Write Mode			
t_1	0	ns min	R/$\overline{W}$ to $\overline{CS}$ setup time
t_2	0	ns min	R/$\overline{W}$ to $\overline{CS}$ hold time
t_3	10	ns min	$\overline{CS}$ low time
t_4	10	ns min	Address setup time
t_5	0	ns min	Address hold time
t_6	6	ns min	Data setup time
t_7	0	ns min	Data hold time
t_8	5	ns min	R/$\overline{W}$ high to $\overline{CS}$ low
t_9	7	ns min	$\overline{CS}$ min high time
Data Readback Mode			
t_{10}	0	ns typ	Address setup time
t_{11}	0	ns typ	Address hold time
t_{12}	5	ns typ	Data access time
	35	ns max	
t_{13}	5	ns typ	Bus relinquish time
	10	ns max	

[1] See Figure 2. Temperature range for Y version is −40°C to +125°C. Guaranteed by design and characterization, not subject to production test.
[2] All input signals are specified with tr = tf = 5ns (10% to 90% of VDD) and timed from a voltage level of (V_{IL} + V_{IH})/2. Digital output timing measured with load circuit in Figure 3.

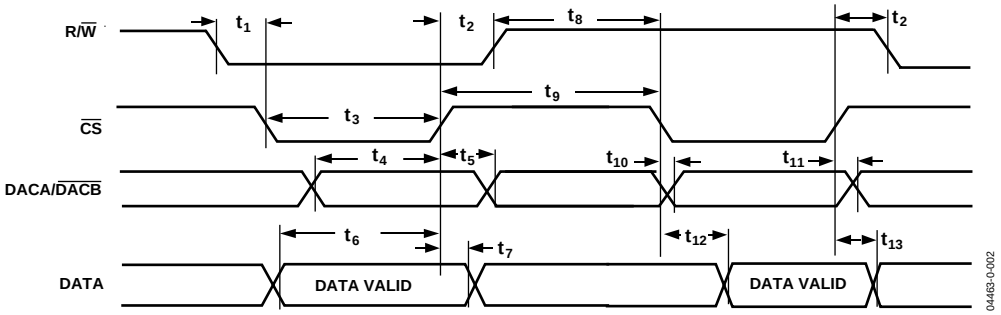

Figure 2. Timing Diagram

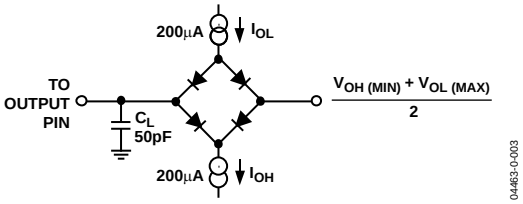

Figure 3. Load Circuit for Data Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
$V_{REF}A$, $V_{REF}B$, $R_{FB}A$, $R_{FB}B$ to GND	−12 V to +12 V
$I_{OUT}1$, $I_{OUT}2$ to GND	−0.3 V to +7 V
Logic Inputs and Output[1]	−0.3V to V_{DD} + 0.3 V
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
40-lead LFCSP, θ_{JA} Thermal Impedance	30°C/W
Lead Temperature, Soldering (10 sec.)	300°C
IR Reflow, Peak Temperature (< 20 sec.)	235°C

[1] Over voltages at DBx, $\overline{LDAC}$, $\overline{CS}$, and $\overline{W}$/R are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

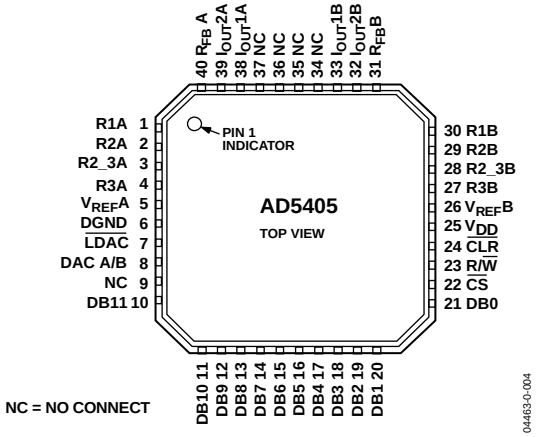

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1 to 4	R1A to R3A	DAC A 4-Quadrant Resistors. Allow a number of configuration modes, including bipolar operation with minimum of external components.
5, 26	$V_{REF}A$, $V_{REF}B$	DAC Reference Voltage Input Terminals.
6	DGND	Digital Ground Pin.
7	$\overline{LDAC}$	Load DAC Input. Allows asynchronous or synchronous updates to the DAC output. The DAC is asynchronously updated when this signal goes low. Alternatively, if this line is held permanently low, an automatic or synchronous update mode is selected whereby the DAC is updated on the rising edge of $\overline{CS}$.
8	DAC A/B	Selects DAC A or B. Low selects DAC A, while high selects DAC B.
9, 34, 35, 36, 37	NC	Not internally connected.
10 to 21	DB11 to DB0	Parallel Data Bits 11 through 0.
22	$\overline{CS}$	Chip Select Input. Active low. Used in conjunction with R/$\overline{W}$ to load parallel data to the input latch or to read data from the DAC register. Edge sensitive; when pulled high, the DAC data is latched.
23	R/$\overline{W}$	Read/Write. When low, used in conjunction with $\overline{CS}$ to load parallel data. When high, used in conjunction with $\overline{CS}$ to read back contents of DAC register.
24	$\overline{CLR}$	Active Low Control Input. Clears DAC output and input and DAC registers.
25	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of 2.5 V to 5.5 V.
26 to 30	R3B to R1B	DAC B 4-Quadrant Resistors. Allow a number of configuration modes, including bipolar operation with a minimum of external components.
32	$I_{OUT}2B$	DAC A Analog Ground. This pin typically should be tied to the analog ground of the system, but may be biased to achieve single-supply operation.
33	$I_{OUT}1B$	DAC B Current Outputs.
38	$I_{OUT}1A$	DAC A Current Outputs.
39	$I_{OUT}2A$	DAC A Analog Ground. This pin typically should be tied to the analog ground of the system, but may be biased to achieve single-supply operation.
31, 40	$R_{FB}B$, $R_{FB}A$	External Amplifier Output.

TYPICAL PERFORMANCE CHARACTERISTICS

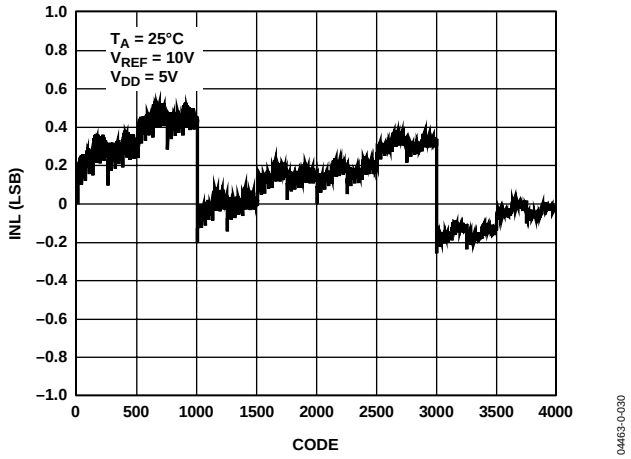

Figure 5. INL vs. Code (12-Bit DAC)

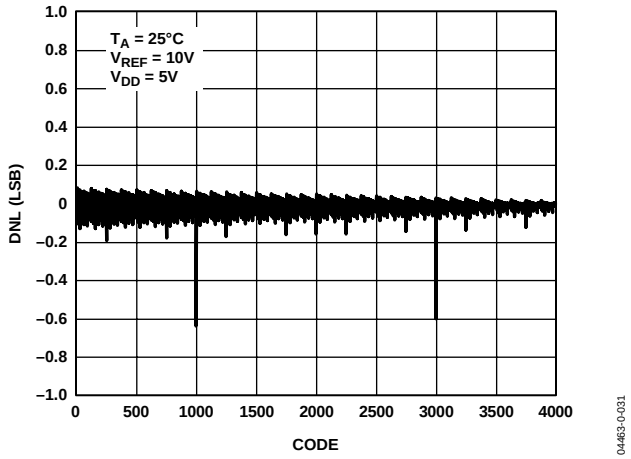

Figure 6. DNL vs. Code (12-Bit DAC)

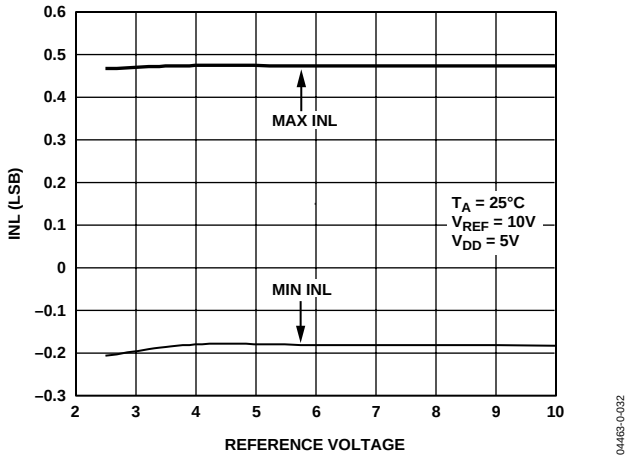

Figure 7. INL vs. Reference Voltage

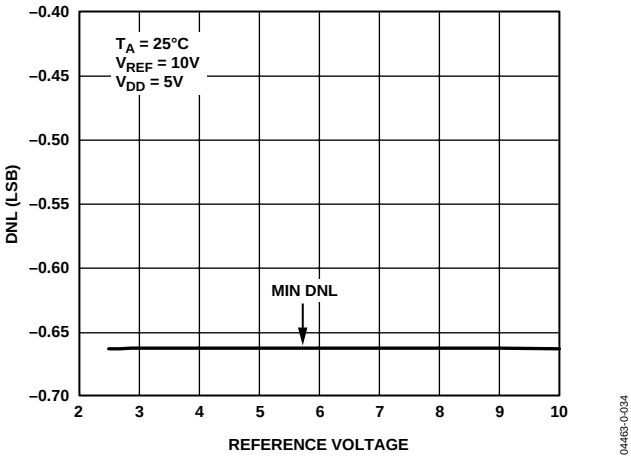

Figure 8. DNL vs. Reference Voltage

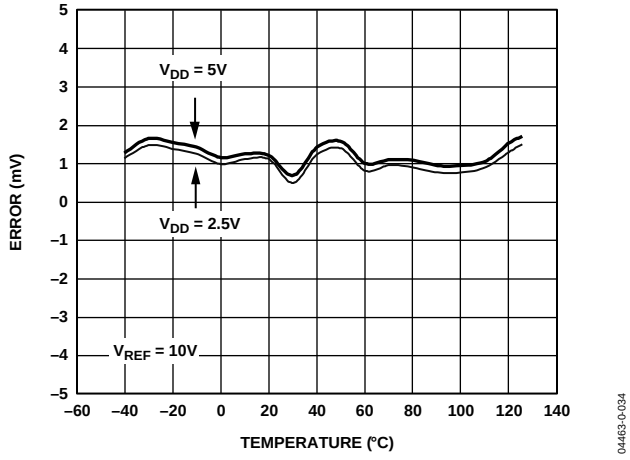

Figure 9. Gain Error vs. Temperature

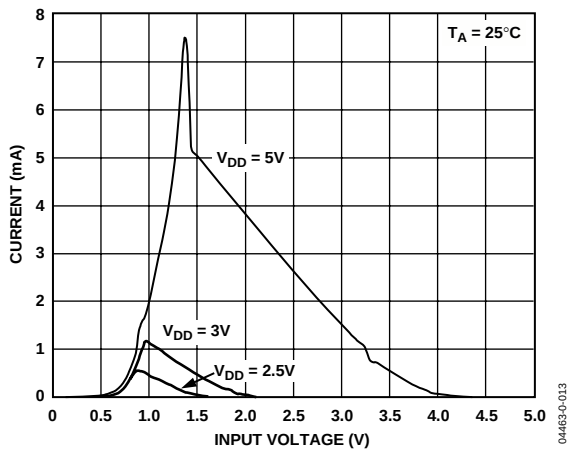

Figure 10. Supply Current vs. Logic Input Voltage

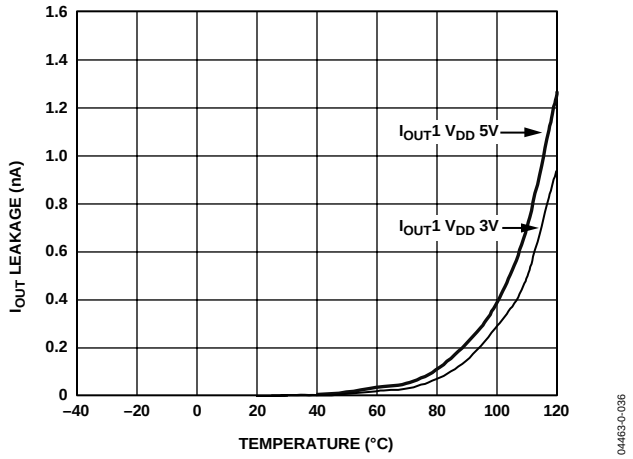

Figure 11. I_{OUT}1 Leakage Current vs. Temperature

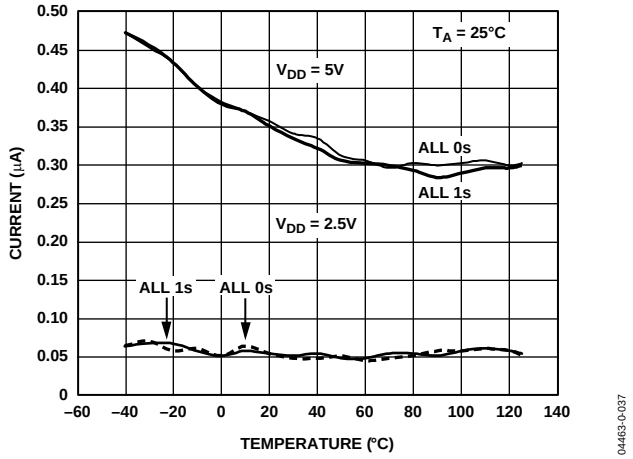

Figure 12. Supply Current vs. Temperature

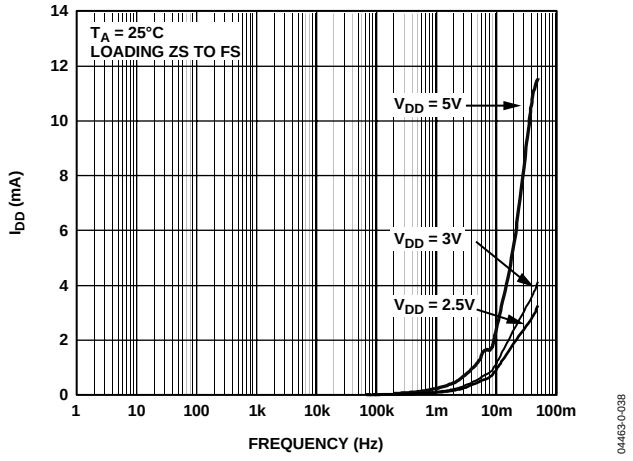

Figure 13. Supply Current vs. Update Rate

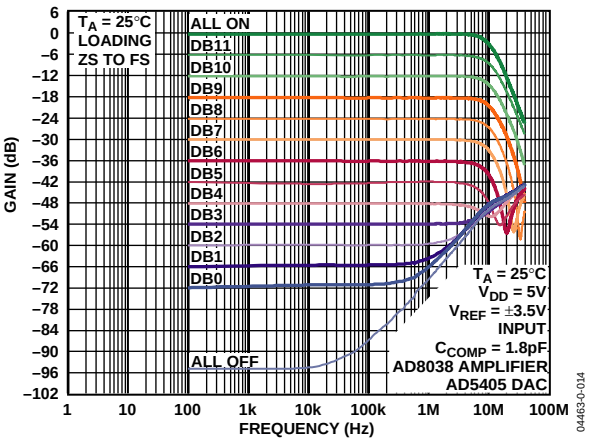

Figure 14. Reference Multiplying Bandwidth vs. Frequency and Code

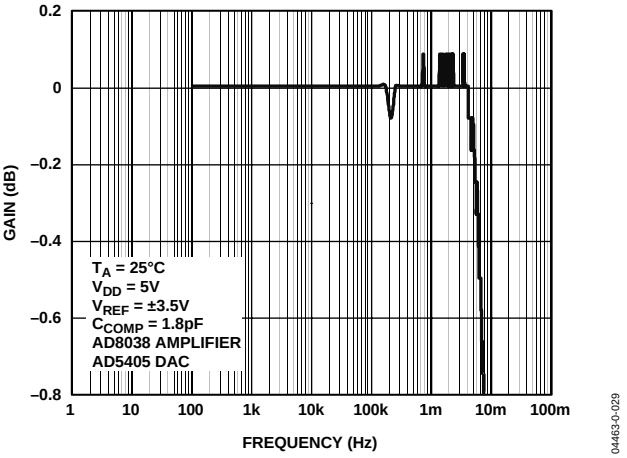

Figure 15. Reference Multiplying Bandwidth–All 1s Loaded

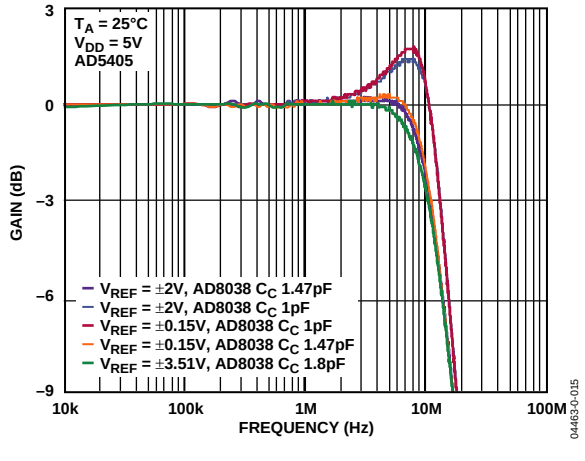

Figure 16. Reference Multiplying Bandwidth vs. Frequency and Compensation Capacitor

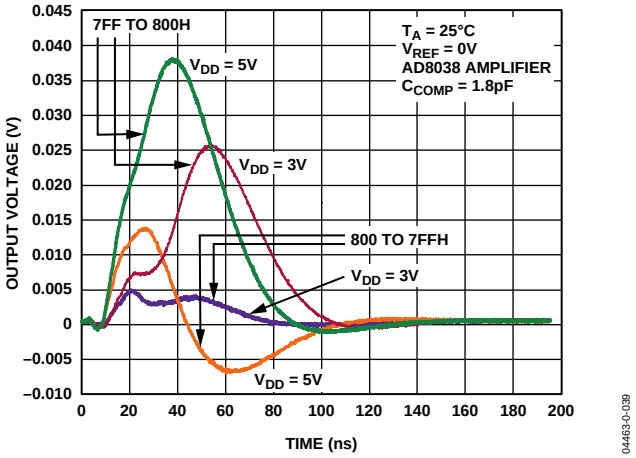

Figure 17. Midscale Transition, V_{REF} = 0 V

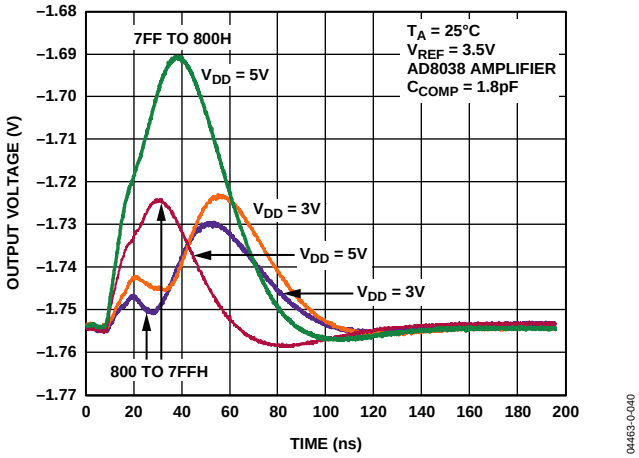

Figure 18. Midscale Transition, V_{REF} = 3.5 V

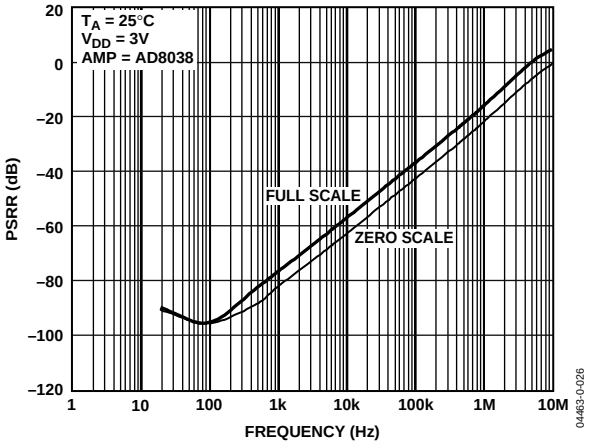

Figure 19. Power Supply Rejection vs. Frequency

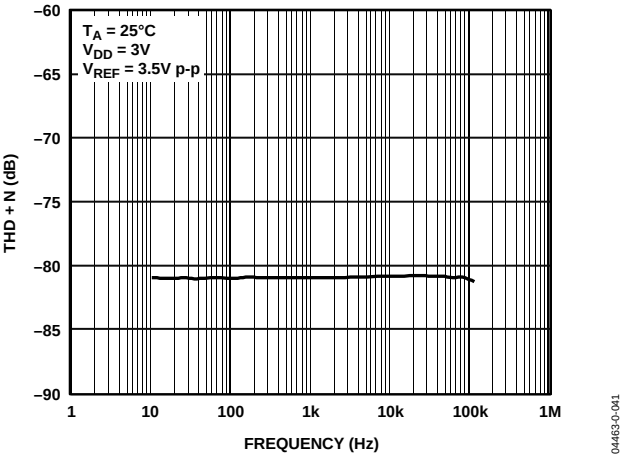

Figure 20. THD and Noise vs. Frequency

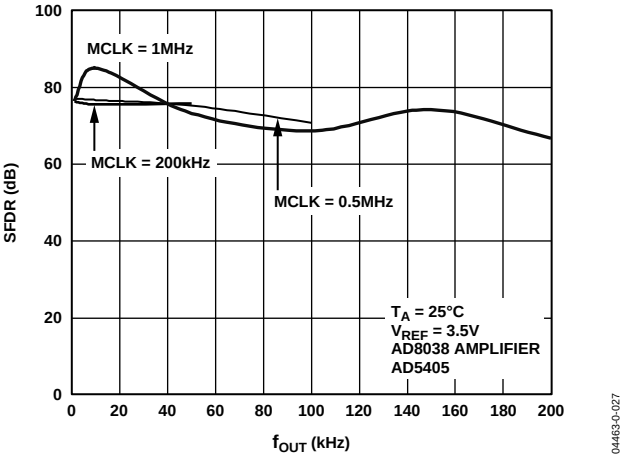

Figure 21. Wideband SFDR vs. f_{OUT} Frequency

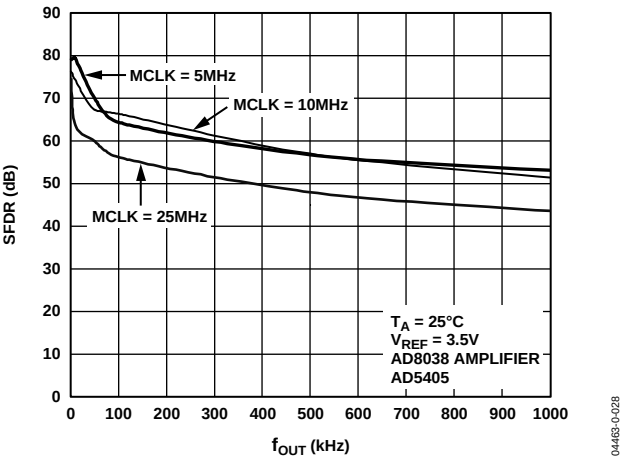

Figure 22. Wideband SFDR vs. f_{OUT} Frequency

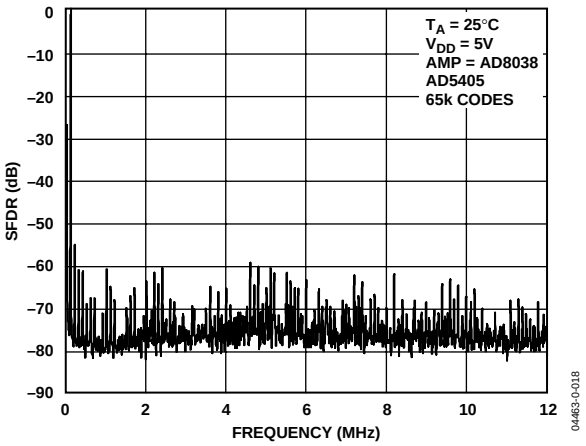

Figure 23. Wideband SFDR, f_{OUT} = 100 kHz, Clock = 25 MHz

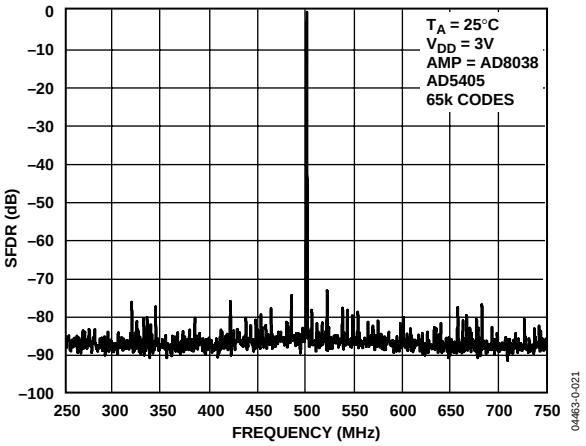

Figure 26. Narrow-Band Spectral Response, f_{OUT} = 500 kHz, Clock = 25 MHz

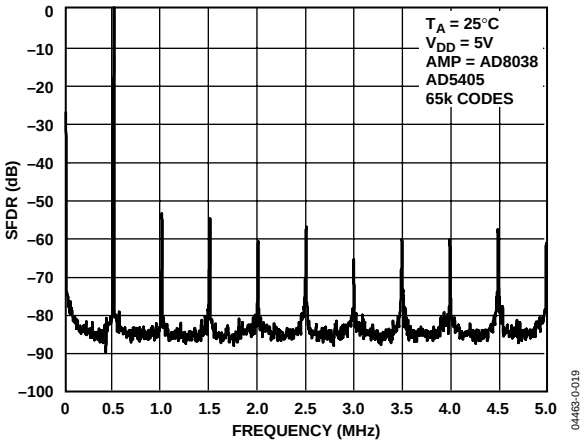

Figure 24. Wideband SFDR, f_{OUT} =500 kHz, Clock = 10 MHz

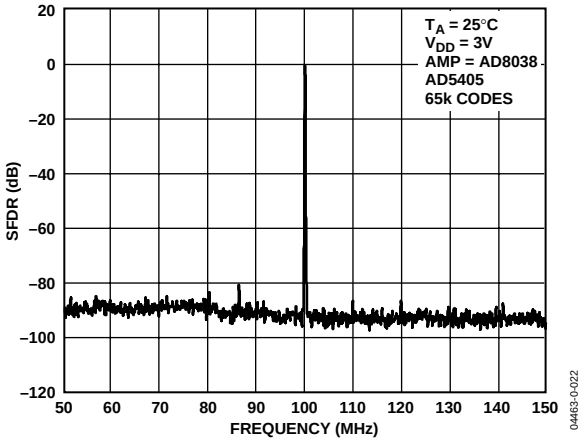

Figure 27. Narrow-Band SFDR, f_{OUT} = 100 kHz, Clock = 25 MHz

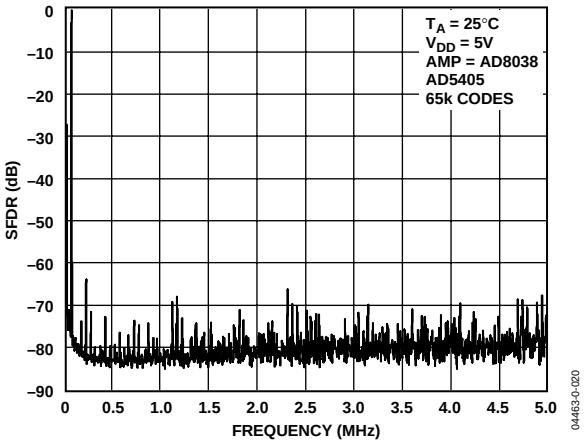

Figure 25. Wideband SFDR, f_{OUT} = 50 kHz, Clock = 10 MHz

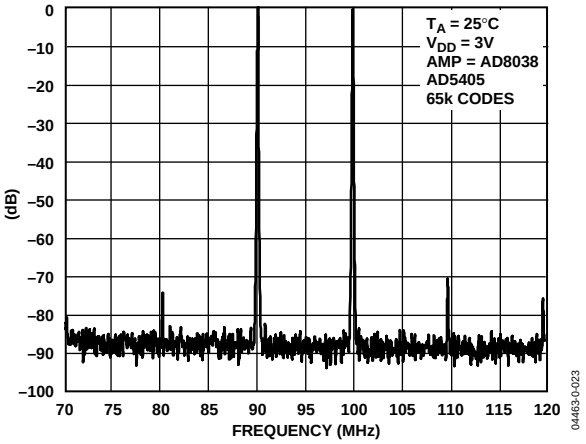

Figure 28. Narrow-Band IMD, f_{OUT} = 90 kHz, 100 kHz, Clock = 10 MHz

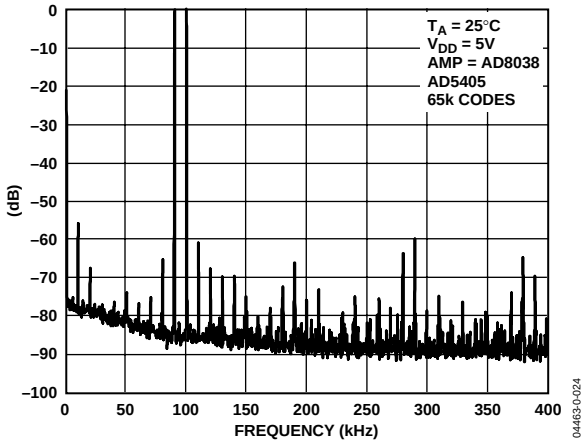

Figure 29. Wideband IMD, f_{OUT} = 90 kHz, 100 kHz, Clock = 25 MHz

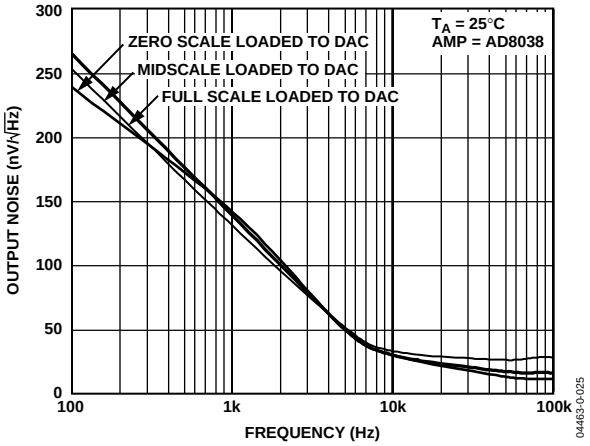

Figure 30. Output Noise Spectral Density

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

Gain Error
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For this DAC, ideal maximum output is V_{REF} − 1 LSB. Gain error of the DACs is adjustable to zero with external resistance.

Output Leakage Current
Output leakage current is current that flows in the DAC ladder switches when these are turned off. For the $I_{OUT}1$ terminal, it can be measured by loading all 0s to the DAC and measuring the $I_{OUT}1$ current. Minimum current flows in the $I_{OUT}2$ line when the DAC is loaded with all 1s.

Output Capacitance
Capacitance from $I_{OUT}1$ or $I_{OUT}2$ to AGND.

Output Current Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change. For this device, it is specified with a 100 Ω resistor to ground.

Digital to Analog Glitch lmpulse
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is typically specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device' s digital inputs is capacitively coupled through the device to show up as noise on the I_{OUT} pins and subsequently into the following circuitry. This noise is digital feedthrough.

Multiplying Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC $I_{OUT}1$ terminal, when all 0s are loaded to the DAC.

Digital Crosstalk
This is the glitch impulse transferred to the outputs of one DAC in response to a full-scale code change (all 0s to all 1s, and vice versa) in the input register of the other DAC. It is expressed in nV-s.

Analog Crosstalk
This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s, and vice versa), while keeping LDAC high. Then pulse LDAC low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-s.

Channel to Channel Isolation
This refers to the proportion of input signal from one DAC's reference input which appears at the output of the other DAC, and is expressed in dBs.

Total Harmonic Distortion (THD)
The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower-order harmonics are included, such as the second to the fifth.

$$THD = 20 \log \frac{\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2\right)}}{V_1}$$

Intermodulation Distortion
The DAC is driven by two combined sine wave references of frequencies fa and fb. Distortion products are produced at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3,... Intermodulation terms are those for which m or n is not equal to zero. The second-order terms include (fa + fb) and (fa − fb) and the third-order terms are (2fa + fb), (2fa − fb), (f + 2fa + 2fb) and (fa − 2fb). IMD is defined as

$$IMD = 20 \log \frac{\left(rms\ sum\ of\ the\ sum\ and\ diff\ distortion\ products\right)}{rms\ amplitude\ of\ the\ fundamental}$$

Compliance Voltage Range
The maximum range of (output) terminal voltage for which the device provides the specified characteristics.

GENERAL DESCRIPTION

DAC SECTION

The AD5405 is a 12-bit, dual-channel, current-output DAC consisting of a standard inverting R-2R ladder configuration. Figure 31 shows a simplified diagram for a single channel of the AD5405. The feedback resistor R_{FB} has a value of 2R. The value of R is typically 10 kΩ (minimum 8 kΩ and maximum 12 kΩ). If $I_{OUT}1A$ and $I_{OUT}2A$ are kept at the same potential, a constant current flows in each ladder leg, regardless of digital input code. Thus, the input resistance presented at V_{REF} is always constant.

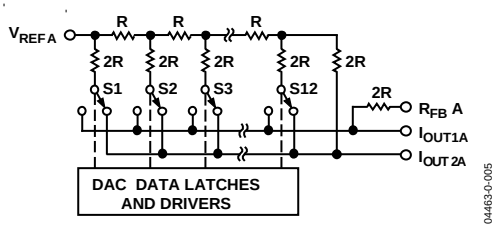

Figure 31. Simplified Ladder Configuration

Access is provided to the V_{REF}, R_{FB}, $I_{OUT}1$, and $I_{OUT}2$ terminals of each DAC, making the device extremely versatile and allowing it to be configured in several different operating modes, such as for unipolar output, bipolar output, or single-supply mode.

CIRCUIT OPERATION

Unipolar Mode

Using a single op amp, this DAC can easily be configured to provide 2-quadrant multiplying operation or a unipolar output voltage swing, as shown in Figure 32.

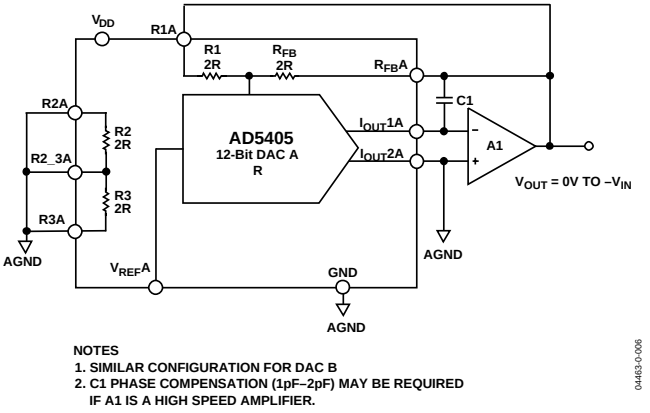

Figure 32. Unipolar Operation

When an output amplifier is connected in unipolar mode, the output voltage is given by

$$V_{OUT} = -D/2^n \times V_{REF}$$

where D is the fractional representation of the digital word loaded to the DAC, and n is the resolution of the DAC.

$$D = 0 \text{ to } 4095$$

With a fixed 10 V reference, the circuit shown in Figure 32 gives a unipolar 0 V to −10 V output voltage swing. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication.

Table 5 shows the relationship between digital code and expected output voltage for unipolar operation.

Table 5. Unipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$-V_{REF}$ (4095/4096)
1000 0000	$-V_{REF}$ (2048/4096) = $-V_{REF}/2$
0000 0001	$-V_{REF}$ (1/4096)
0000 0000	$-V_{REF}$ (0/4096) = 0

Bipolar Operation

In some applications, it may be necessary to generate full 4-quadrant multiplying operation or a bipolar output swing. This can be easily accomplished by using another external amplifier, as shown in Figure 33.

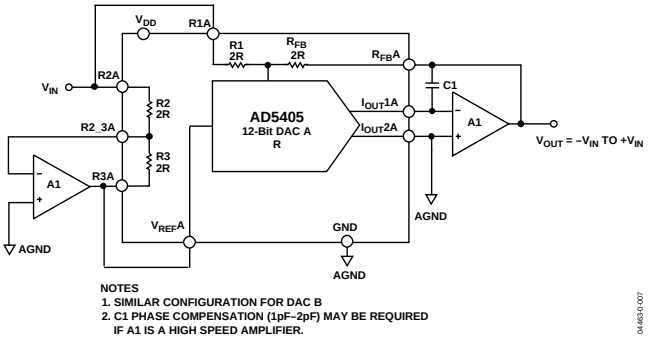

Figure 33. Bipolar Operation (4-Quadrant Multiplication)

When in bipolar mode, the output voltage is given by

$$V_{OUT} = V_{REF} \times D/2^{n-1} \times V_{REF}$$

where D is the fractional representation of the digital word loaded to the DAC, in the range of 0 to 4095, and n is the number of bits. When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication.

Table 6 shows the relationship between the digital code and the expected output voltage for bipolar operation.

Table 6. Bipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$+V_{REF}$ (2047/2048)
1000 0000	0
0000 0001	$-V_{REF}$ (2047/2048)
0000 0000	$-V_{REF}$ (2048/2048)

Stability

In the I-to-V configuration, the I_{OUT} of the DAC and the inverting node of the op amp must be connected as close as possible, and proper PCB layout techniques must be employed. Because every code change corresponds to a step function, gain peaking may occur if the op amp has limited GBP and there is excessive parasitic capacitance at the inverting node. This parasitic capacitance introduces a pole into the open loop response which can cause ringing or instability in the closed-loop applications circuit.

An optional compensation capacitor, C1, can be added in parallel with R_{FB} for stability, as shown in Figure 32 and Figure 33. Too small a value of C1 can produce ringing at the output, while too large a value can adversely affect the settling time. C1 should be found empirically, but 1 pF to 2 pF is generally adequate for the compensation.

SINGLE-SUPPLY APPLICATIONS

Voltage Switching Mode of Operation

Figure 34 shows these DACs operating in the voltage switching mode. The reference voltage, V_{IN}, is applied to the $I_{OUT}1$ pin, $I_{OUT}2$ is connected to AGND, and the output voltage is available at the V_{REF} terminal. In this configuration, a positive reference voltage results in a positive output voltage, making single-supply operation possible. The output from the DAC is voltage at a constant impedance (the DAC ladder resistance). Thus an op amp is necessary to buffer the output voltage. The reference input no longer sees a constant input impedance, but one that varies with code. So, the voltage input should be driven from a low impedance source.

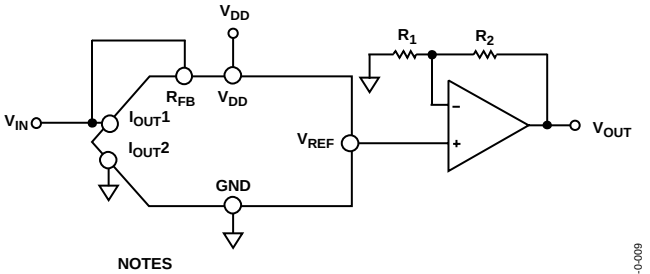

Figure 34. Single-Supply Voltage Switching Mode

Note that V_{IN} is limited to low voltages because the switches in the DAC ladder no longer have the same source-drain drive voltage. As a result, their on resistance differs and degrades the integral linearity of the DAC. Also, V_{IN} must not go negative by more than 0.3 V or an internal diode turns on, exceeding the max ratings of the device. In this type of application, the full range of multiplying capability of the DAC is lost.

POSITIVE OUTPUT VOLTAGE

Note that the output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages. In order to achieve a positive voltage output, an applied negative reference to the input of the DAC is preferred over the output inversion through an inverting amplifier because of the resistor's tolerance errors. To generate a negative reference, the reference can be level shifted by an op amp such that the V_{OUT} and GND pins of the reference become the virtual ground and −2.5 V respectively, as shown in Figure 35.

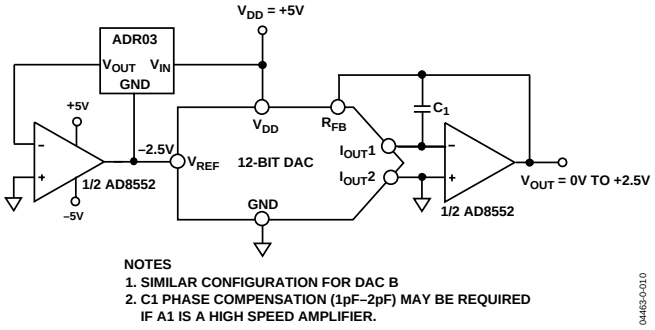

Figure 35. Positive Voltage Output with Minimum Components

ADDING GAIN

In applications where the output voltage is required to be greater than V_{IN}, gain can be added with an additional external amplifier or it can also be achieved in a single stage. Consider the effect of temperature coefficients of the thin film resistors of the DAC. Simply placing a resistor in series with the R_{FB} resistor causes mismatches in the temperature coefficients resulting in larger gain temperature coefficient errors. Instead, the circuit of Figure 36 is a recommended method of increasing the gain of the circuit. R_1, R_2, and R_3 should all have similar temperature coefficients, but they need not match the temperature coefficients of the DAC. This approach is recommended in circuits where gains of > 1 are required.

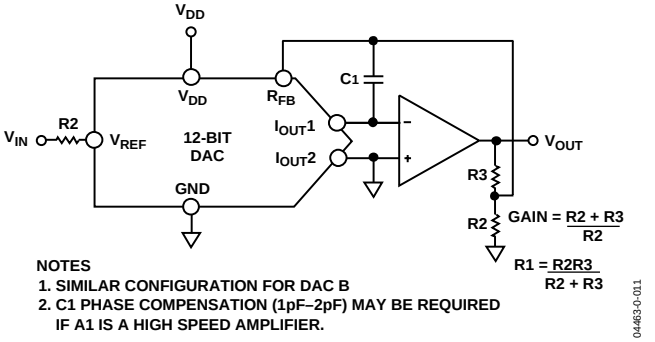

Figure 36. Increasing Gain of Current Output DAC

USED AS A DIVIDER OR PROGRAMMABLE GAIN ELEMENT

Used as a divider or programmable gain element, current-steering DACs are very flexible and lend themselves to many different applications. If this type of DAC is connected as the feedback element of an op amp, and R_{FB} is used as the input resistor, as shown in Figure 37, then the output voltage is inversely proportional to the digital input fraction D.

For $D = 1-2^n$ the output voltage is

$$V_{OUT} = -V_{IN}/D = -V_{IN}/\left(1-2^{-n}\right)$$

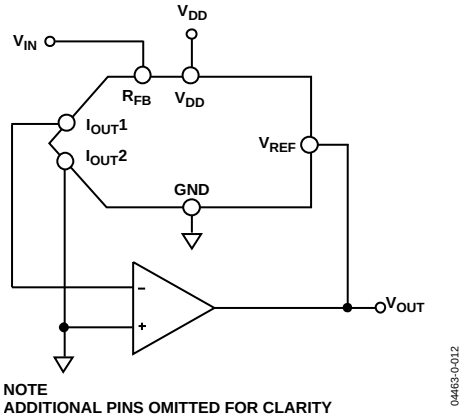

Figure 37. Current-Steering DAC Used as a Divider or Programmable Gain Element

As D is reduced, the output voltage increases. For small values of the digital fraction D, it is important to ensure that the amplifier does not saturate and also that the required accuracy is met. For example, an 8-bit DAC driven with the binary code 0 × 10 (00010000), that is, 16 decimal, in the circuit of Figure 37 should cause the output voltage to be 16 × V_{IN}. However, if the DAC has a linearity specification of ±0.5 LSB, then D can, in fact, have the weight anywhere in the range 15.5/256 to 16.5/256 so that the possible output voltage is in the range 15.5 V_{IN} to 16.5 V_{IN}—an error of 3% even though the DAC itself has a maximum error of 0.2%.

DAC leakage current is also a potential error source in divider circuits. The leakage current must be counterbalanced by an opposite current supplied from the op amp through the DAC. Because only a fraction D of the current into the V_{REF} terminal is routed to the $I_{OUT}1$ terminal, the output voltage has to change as follows:

Output Error Voltage Due to DAC Leakage = (*Leakage* × *R*)/*D*

where R is the DAC resistance at the V_{REF} terminal.

For a DAC leakage current of 10 nA, R = 10 kΩ and a gain (that is, 1/D) of 16, the error voltage is 1.6 mV.

REFERENCE SELECTION

When selecting a reference for use with the AD5405 series of current output DACs, pay attention to the reference output voltage temperature coefficient specification. This parameter not only affects the full-scale error, but can also affect the linearity (INL and DNL) performance. The reference temperature coefficient should be consistent with the system accuracy specifications. For example, an 8-bit system required to hold its overall specification to within 1 LSB over the temperature range 0°C to 50°C dictates that the maximum system drift with temperature should be less than 78 ppm/°C. A 12-bit system with the same temperature range to overall specification within 2 LSBs requires a maximum drift of 10 ppm/°C. By choosing a precision reference with low output temperature coefficient, this error source can be minimized. Table 7 lists some references available from Analog Devices that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. The input offset voltage of an op amp is multiplied by the variable gain (due to the code-dependent output resistance of the DAC) of the circuit. A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed upon the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, could cause the DAC to be nonmonotonic.

The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing in the feedback resistor R_{FB}. Most op amps have input bias currents low enough to prevent any significant errors in 12-bit applications.

Common-mode rejection of the op amp is important in voltage-switching circuits, because it produces a code-dependent error at the voltage output of the circuit. Most op amps have adequate common-mode rejection for use at 12-bit resolution.

Provided the DAC switches are driven from true wide band, low impedance sources (V_{IN} and AGND) they settle quickly. Consequently, the slew rate and settling time of a voltage-switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time in this configuration, minimize capacitance at the V_{REF} node (voltage output node in this application) of the DAC. This is done by using low input capacitance buffer amplifiers and careful board design.

Most single-supply circuits include ground as part of the analog signal range, which in turn requires an amplifier that can handle rail-to-rail signals. Analog Devices offers a large range of single-supply amplifiers, as listed in Table 8.

Table 7. Suitable ADI Precision References Recommended for Use with AD5405 DACs

Reference	Output Voltage	Initial Tolerance	Temperature Drift	0.1 Hz to 10 Hz noise	Package
ADR01	10 V	0.1%	3 ppm/°C	20 µV p-p	SC70, TSOT, SOIC
ADR02	5 V	0.1%	3 ppm/°C	10 µV p-p	SC70, TSOT, SOIC
ADR03	2.5 V	0.2%	3 ppm/°C	10 µV p-p	SC70, TSOT, SOIC
ADR425	5 V	0.04%	3 ppm/°C	3.4 µV p-p	MSOP, SOIC

Table 8. Precision ADI Op Amps Suitable for Use with AD5405 DACs

Part No.	Max Supply Voltage V	V_{OS} (max) µV	I_B (max) nA	GBP MHz	Slew Rate V/µs
OP97	±20	25	0.1	0.9	0.2
OP1177	±18	60	2	1.3	0.7
AD8551	+6	5	0.05	1.5	0.4

Table 9. High Speed ADI Op Amps Suitable for Use with AD5405 DACs

Part No.	Max Supply Voltage V	V_{OS} (max) µV	I_B (max) nA	BW @ A_{CL} MHz	Slew Rate V/µs
AD8065	±12	1500	0.01	145	180
AD8021	±12	1000	1000	200	100
AD8038	±5	3000	0.75	350	425

PARALLEL INTERFACE

Data is loaded to the AD5405 in the format of a 12-bit parallel word. Control lines $\overline{CS}$ and R/$\overline{W}$ allow data to be written to or read from the DAC register. A write event takes place when $\overline{CS}$ and R/$\overline{W}$ are brought low, data available on the data lines fills the shift register, and the rising edge of $\overline{CS}$ latches the data and transfers the latched data word to the DAC register. The DAC latches are not transparent, thus a write sequence must consist of a falling and rising edge on $\overline{CS}$ to ensure data is loaded to the DAC register and its analog equivalent reflected on the DAC output. A read event takes place when R/$\overline{W}$ is held high and $\overline{CS}$ is brought low. Data is loaded from the DAC register back to the input register and out onto the data line where it can be read back to the controller for verification or diagnostic purposes. The input and DAC registers of these devices are not transparent, so a falling and rising edge of $\overline{CS}$ is required to load each data-word.

MICROPROCESSOR INTERFACING

The AD5405 can be interfaced to a variety of 16-bit microcontrollers or DSP processors. Figure 38 shows the AD5405 DAC interfaced to a generic 16-bit microcontroller/DSP processor. Microprocessor interfacing to this family of DAC is via a data bus that uses a standard protocol compatible with microcontrollers and DSP processors. The address decoder selects DAC A or DAC B and also to loads parallel data to the input latch or to read data from the DAC using an AND gate.

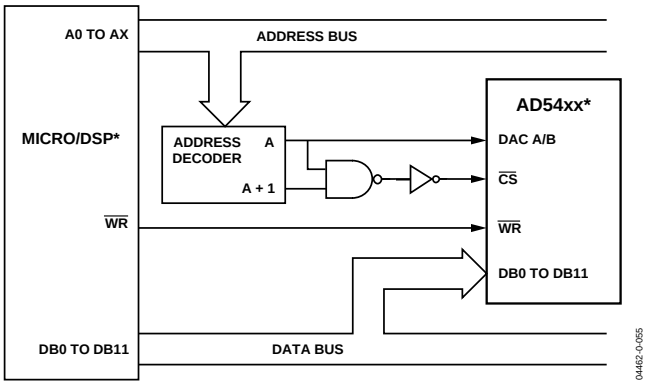

Figure 38. AD54xx to Parallel Interface

PCB LAYOUT AND POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5405 is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the DAC is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

These DACs should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as close to the package as possible, ideally right up against the device. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane while signal traces are placed on the soldered side.

It is good practice to employ compact, minimum lead length PCB layout design. Leads to the input should be as short as possible to minimize IR drops and stray inductance.

The PCB metal traces between V_{REF} and R_{FB} should also be matched to minimize gain error. To maximize high frequency performance, the I-to-V amplifier should be located as close to the device as possible.

EVALUATION BOARD FOR THE DACS

The evaluation board consists of a DAC and a current-to-voltage amplifier, the AD8065. Included on the evaluation board is a 10 V reference, the ADR01. An external reference may also be applied via an SMB input.

The evaluation kit consists of a CD-ROM with self-installing PC software to control the DAC. The software simply allows the user to write a code to the device.

POWER SUPPLIES FOR THE EVALUATION BOARD

The board requires ±12 V and 5 V supplies. The 12 V V_{DD} and V_{SS} are used to power the output amplifier, while the 5 V is used to power the DAC (V_{DD1}) and transceivers (V_{CC}).

Both supplies are decoupled to their respective ground plane with 10 µF tantalum and 0.1 µF ceramic capacitors.

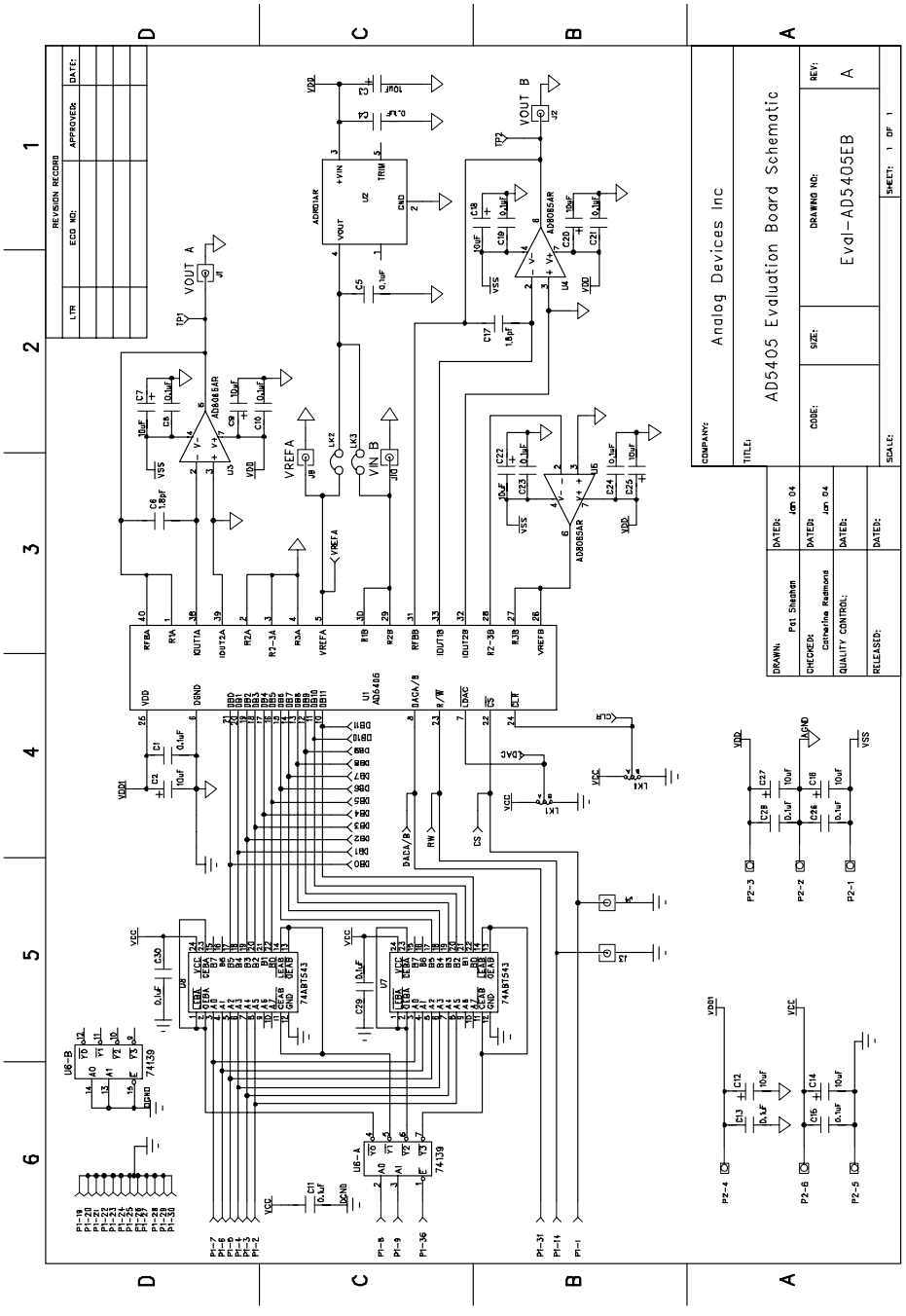

Figure 39. Schematic of AD5405 Evaluation Board

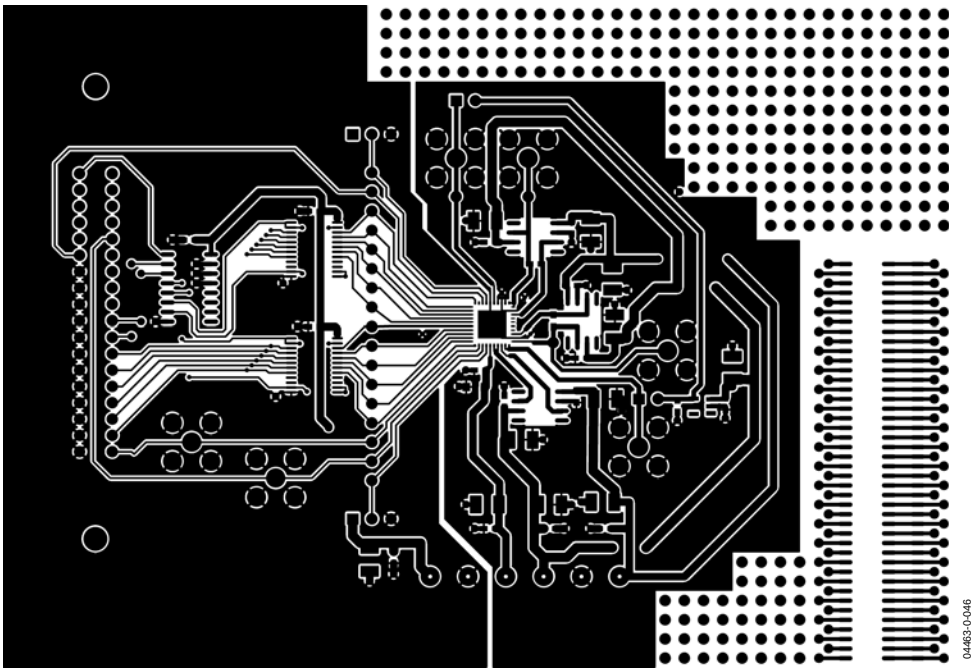

Figure 40. Component-Side Artwork

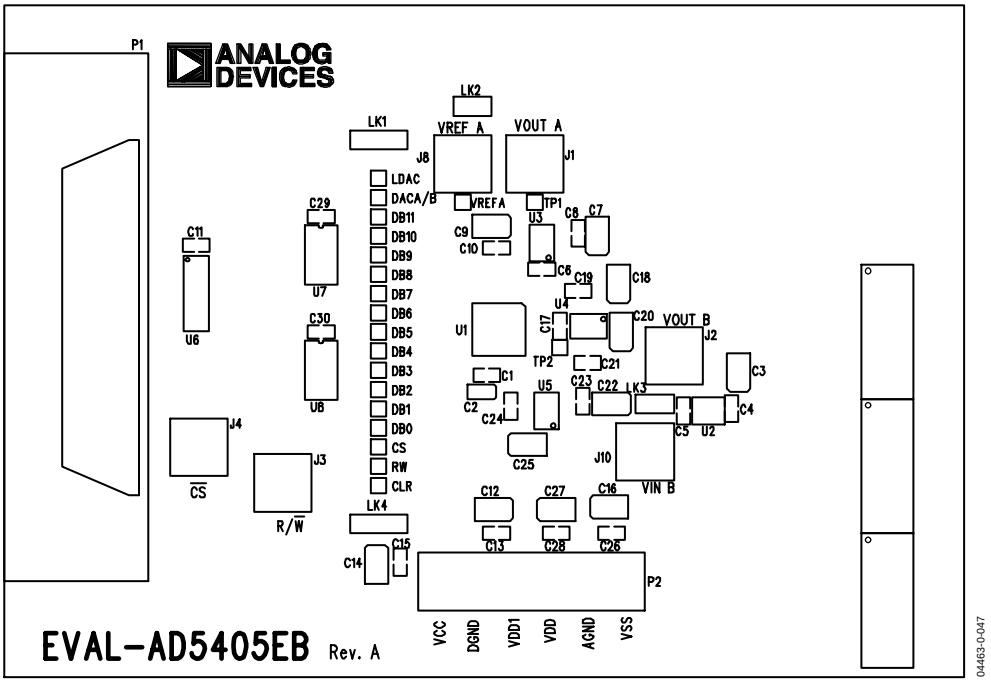

Figure 41. Silkscreen—Component-Side View (Top Layer)

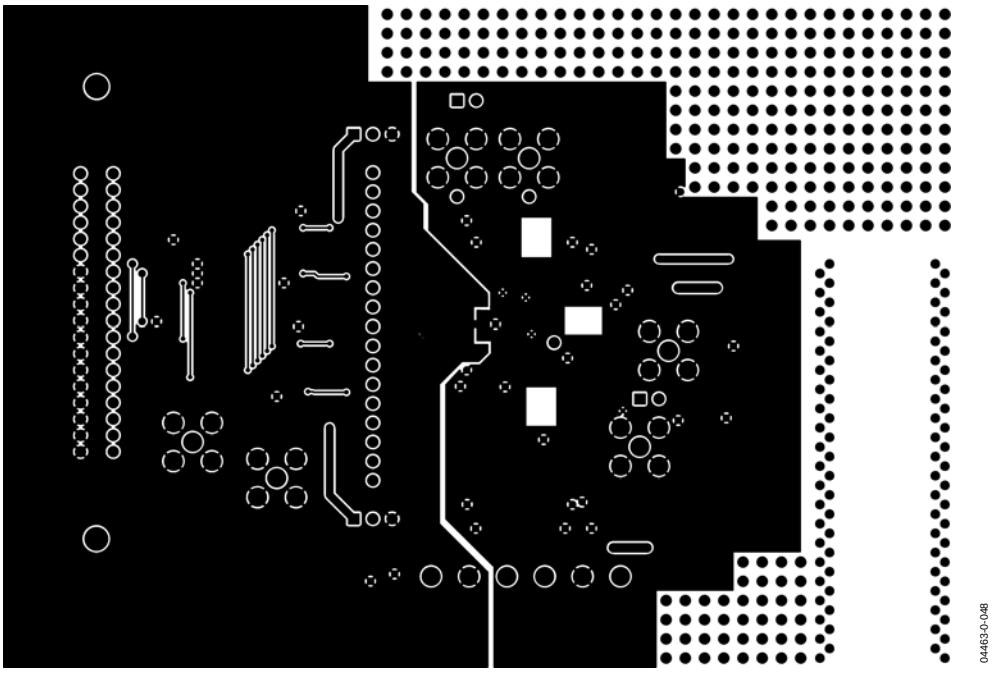

Figure 42. Solder-Side Artwork

OVERVIEW OF AD54xx DEVICES

Table 10.

Part No.	Resolution	No. DACs	INL(LSB)	Interface	Package	Features
AD5424	8	1	±0.25	Parallel	RU-16, CP-20	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5426	8	1	±0.25	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5428	8	2	±0.25	Parallel	RU-20	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5429	8	2	±0.25	Serial	RU-10	10 MHz BW, 50 MHz Serial
AD5450	8	1	±0.25	Serial	RJ-8	10 MHz BW, 50 MHz Serial
AD5432	10	1	±0.5	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5433	10	1	±0.5	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5439	10	2	±0.5	Serial	RU-16	10 MHz BW, 50 MHz Serial
AD5440	10	2	±0.5	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5451	10	1	±0.25	Serial	RJ-8	10 MHz BW, 50 MHz Serial
AD5443	12	1	±1	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5444	12	1	±0.5	Serial	RM-8	10 MHz BW, 50 MHz Serial
AD5415	12	2	±1	Serial	RU-24	10 MHz BW, 58 MHz Serial
AD5445	12	2	±1	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5447	12	2	±1	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5449	12	2	±1	Serial	RU-16	10 MHz BW, 50 MHz Serial
AD5452	12	1	±0.5	Serial	RJ-8, RM-8	10 MHz BW, 50 MHz Serial
AD5446	14	1	±1	Serial	RM-8	10 MHz BW, 50 MHz Serial
AD5453	14	1	±2	Serial	UJ-8, RM-8	10 MHz BW, 50 MHz Serial
AD5553	14	1	±1	Serial	RM-8	4 MHz BW, 50 MHz Serial Clock
AD5556	14	1	±1	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ Pulse Width
AD5555	14	2	±1	Serial	RM-8	4 MHz BW, 50 MHz Serial Clock
AD5557	14	2	±1	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ Pulse Width
AD5543	16	1	±2	Serial	RM-8	4 MHz BW, 50 MHz Serial Clock
AD5546	16	1	±2	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ Pulse Width
AD5545	16	2	±2	Serial	RU-16	4 MHz BW, 50 MHz Serial Clock
AD5547	16	2	±2	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ Pulse Width

OUTLINE DIMENSIONS

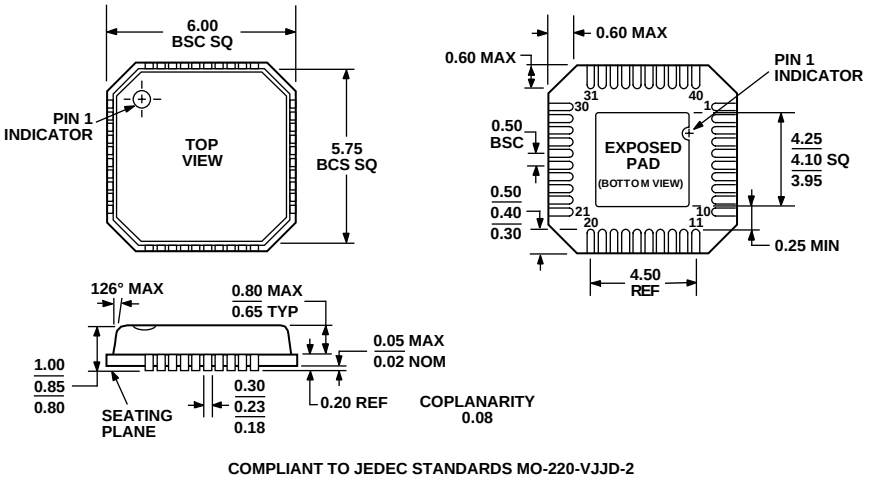

Figure 43. 40 Lead LFCSP
(CP-40)
Dimensions shown in inches and (mm)

ORDERING GUIDE

Model	Resolution	INL (LSBs)	Temperature Range	Package Description	Package Option
AD5405YCP	12	±1	−40°C to +125°C	LFCSP	CP-40
AD5405YCP–REEL	12	±1	−40°C to +125°C	LFCSP	CP-40
AD5405YCP–REEL7	12	±1	−40°C to +125°C	LFCSP	CP-40
EVAL-AD5405EB				Evaluation Kit	

NOTES

D04463–0–7/04(0)