

Quad Line Receiver

AVAILABLE AS MILITARY SPECIFICATIONS

- Military Equivalent Screening - 883 1.2.2

GENERAL DESCRIPTION

The AS10515F16MIL is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the AS10515F16MIL with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 9) to prevent upsetting the current source bias network.

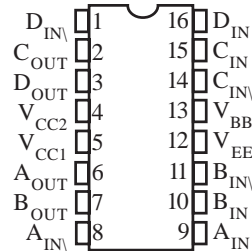
- $P_D = 150\text{mW Max/Pkg}$ (No Load)
- $t_{pd} = 2.0\text{ns typ}$
- $t_r, t_f = 2.0\text{ns type}$ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	FLATS	BURN-IN (CONDITION C)
V_{CC1}	5	GND
A_{OUT}	6	$51\ \Omega$ to V_{TT}
B_{OUT}	7	$51\ \Omega$ to V_{TT}
$A_{IN}\backslash$	8	V_{BB}
A_{IN}	9	GND
B_{IN}	10	GND
$B_{IN}\backslash$	11	V_{BB}
V_{EE}	12	V_{EE}
V_{BB}	13	V_{BB}
$C_{IN}\backslash$	14	V_{BB}
C_{IN}	15	GND
D_{IN}	16	GND
$D_{IN}\backslash$	1	V_{BB}
C_{OUT}	2	$51\ \Omega$ to V_{TT}
D_{OUT}	3	$51\ \Omega$ to V_{TT}
V_{CC2}	4	GND

PIN ASSIGNMENT (Top View)

16-Pin FlatPack (F)



BURN-IN CONDITIONS:

$V_{TT} = -2.0\text{V MAX} / -2.2\text{V MIN}$

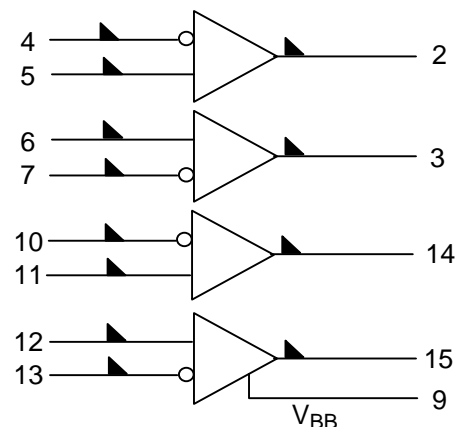
$V_{EE} = -5.7\text{V MAX} / -5.2\text{V MIN}$

V_{BB} = All pins designated for V_{BB} must be tied together, no external voltage applied.

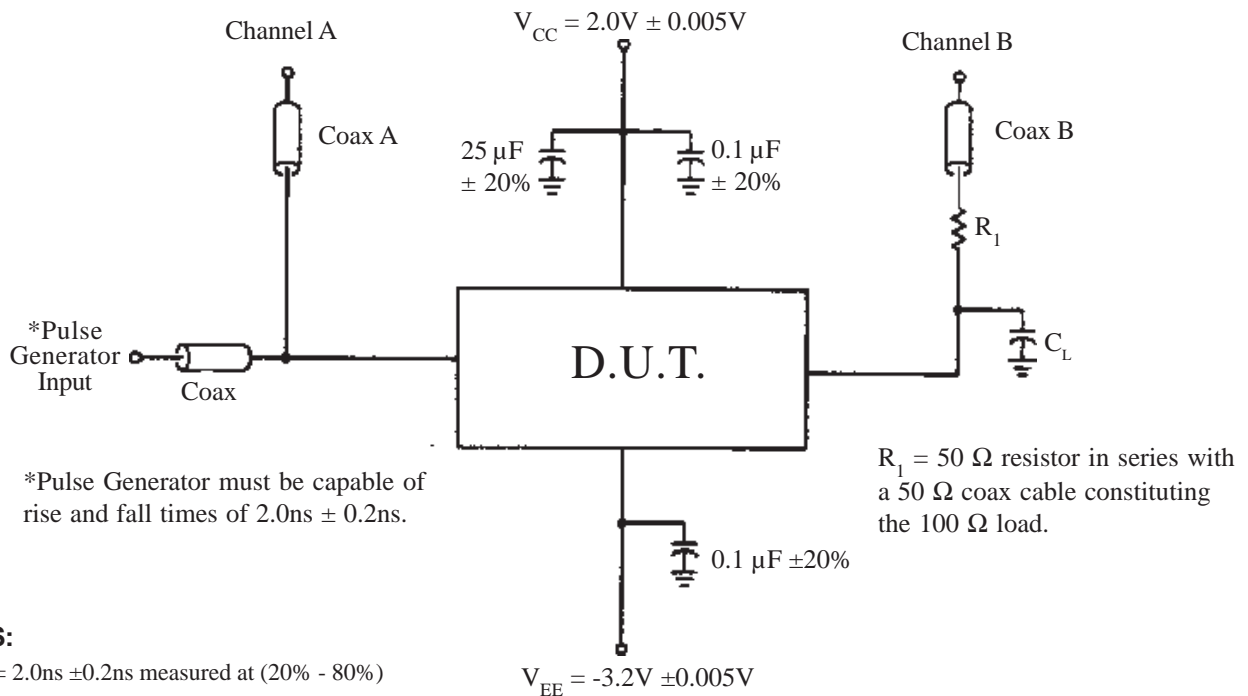
NOTES

1. V_{BB} to be used to supply bias to the AS10515F16MIL only and bypassed (when used) with $0.01\ \mu\text{F}$ to $0.1\ \mu\text{F}$ capacitor.
2. When the input pin with the bubble goes positive, the output goes negative.

LOGIC DIAGRAM



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NOTES:

1. $t_r = t_f = 2.0ns \pm 0.2ns$ measured at (20% - 80%)
2. $P_w \geq 20ns$
3. $P_{RF} = 1.0$ MHz
4. $R_1 = 50 \Omega$ resistor in series with 50Ω coax constituting the 100Ω load.
5. Unused outputs should be loaded 100Ω to ground.
6. 2:1 divider may be used.

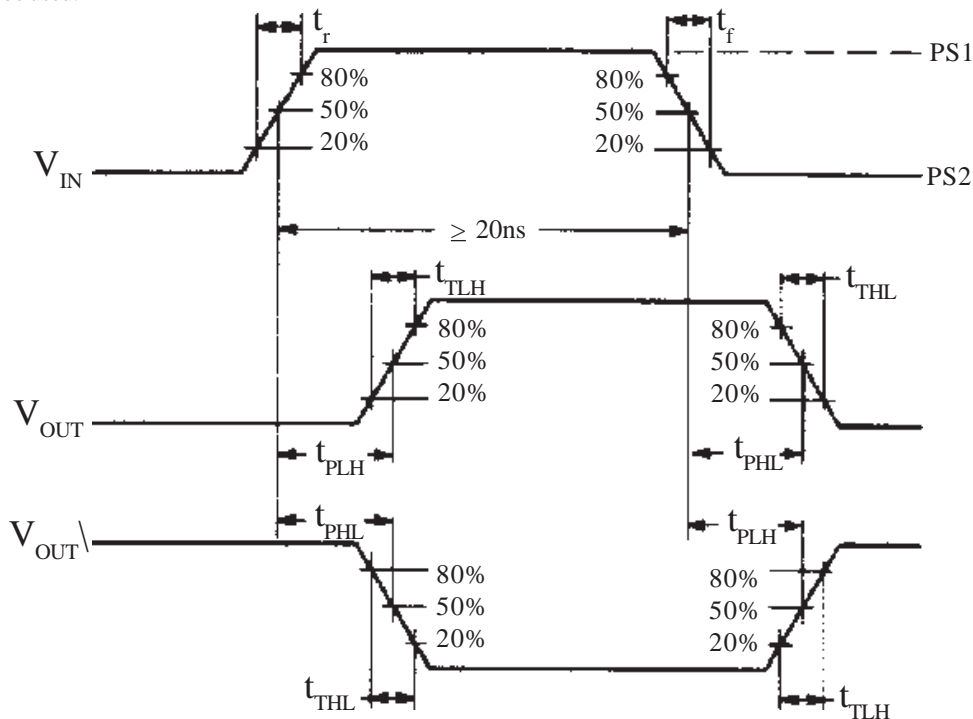


Figure 1. Switching Test Circuit and Waveforms

QUIESCENT LIMIT TABLE*

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	PS1	PS2	VEEL	V _{EE}	V _{CB}	
T _A = 25°C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-3.2	-5.2	-5.2	
T _A = 125°C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-3.2	-5.2	-5.2	
T _A = -55°C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-3.2	-5.2	-5.2	

SYMBOL	PARAMETER	LIMITS						UNITS	TEST VOLTAGE APPLIED TO PINS BELOW:							
		+25°C		+125°C		-55°C			Pinouts referenced are for F package, check Pin Assignments V _{CC} = 0V, Output Load = 100 Ω to -2.0V							
		Subgroup 1	Subgroup 2	Subgroup 1	Subgroup 2	Subgroup 3	Subgroup 3		V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	V _{EE}	V _{CC}	***	P.U.T.
V _{OH}	High Output Voltage	-0.93	-0.78	-0.825	-0.63	-1.08	-0.88	V	5, 6, 11, 12	4, 7, 10, 13			8	1, 16	4-7 11-13	2, 3, 14, 15
V _{OL}	Low Output Voltage	-1.85	-1.62	-1.82	-1.545	-1.92	-1.655	V	4, 7, 10, 13	5, 6, 11, 12			8	1, 16	4-7 11-13	2, 3, 14, 15
V _{OH1}	High Output Voltage	-0.95	-0.78	-0.845	-0.63	-1.10	-0.88	V			5, 6, 11, 12	4, 7, 10, 13	8	1, 16	4-7 11-13	2, 3, 14, 15
V _{OL1}	Low Output Voltage	-1.85	-1.60	-1.82	-1.525	-1.92	-1.635	V			4, 7, 10, 13	5, 6, 11, 12	8	1, 16	4-7 11-13	2, 3, 14, 15
**V _{BB}	Reference Voltage	-1.35	-1.23	-1.24	-1.12	-1.44	-1.32	V					8	1, 16	5, 6 11, 12	9
I _{EE}	Power Supply Current		-26		-29		-29	mA					8	1, 16	5, 6 11, 12	8
I _{IH}	Input Current High		95		165		165	μA	4-7 10-13				8	1, 16		4-7 10-13
I _{CBO}	Input Leakage Current		-1.0		-1.0		-1.5	μA					8	1, 16	4-7 10-13	4-7 10-13

** Connected to pin 9.
 *** Measure voltage on pin 9 while it is connected to other pins.

QUIESCENT LIMIT TABLE*

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Test Temperature	Test Voltage Values (Volts)									
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	P _{S1}	P _{S2}	V _{EEL}	V _{EE}	V _{CB}	V _{CB}
T _A = 25°C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-3.2	-5.2	-5.2	-5.2
T _A = 125°C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-3.2	-5.2	-5.2	-5.2
T _A = -55°C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-3.2	-5.2	-5.2	-5.2

SYMBOL	PARAMETER	LIMITS						UNITS	TEST VOLTAGE APPLIED TO PINS BELOW:				
		+25°C		+125°C		-55°C			Pinouts referenced are for F package, check Pin Assignments V _{CC} = 2.0V, Output Load = 100 Ω to GND				
		Subgroup 9	Subgroup 10	Subgroup 9	Subgroup 10	Subgroup 11	Subgroup 11		V _{IN}	V _{OUT}	V _{CC}	V _{EEL}	P.U.T.
t _{TLH}	Rise Time	MIN 1.1	MAX 3.3	MIN 1.0	MAX 4.4	MIN 1.0	MAX 3.9	ns	4, 7, 11, 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t _{THL}	Fall Time	MIN 1.1	MAX 3.3	MIN 1.0	MAX 4.4	MIN 1.0	MAX 3.9	ns	4, 7, 11, 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t _{PHL}	Propagation Delay High to Low	MIN 1.0	MAX 2.9	MIN 1.0	MAX 4.0	MIN 1.0	MAX 3.5	ns	4, 7, 11, 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t _{PLH}	Propagation Delay Low to High	MIN 1.0	MAX 2.90	MIN 1.0	MAX 4.0	MIN 1.0	MAX 3.5	ns	4, 7, 11, 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15