1.6V Nanopower Comparators with/without Internal References

FEATURES

- ♦ Second-source for MAX9117-MAX9120
- ♦ Guaranteed to Operate Down to +1.6V
- ♦ Ultra-Low Supply Current
  - 350nA - TSM9119/TSM9120
  - 600nA - TSM9117/TSM9118
- ♦ Internal 1.252V ±1.75% Reference
- ♦ Input Voltage Range Extends 200mV Outside-the-Rails
- ♦ No Phase Reversal for Overdriven Inputs
- ♦ Push-pull and Open-Drain Output Versions Available
- ♦ Crowbar-Current-Free Switching
- ♦ Internal Hysteresis for Clean Switching
- ♦ 5-pin SC70 and 8-pin SOIC Packaging

APPLICATIONS

2-Cell Battery Monitoring/Management
Medical Instruments
Threshold Detectors/Discriminators
Sensing at Ground or Supply Line
Ultra-Low-Power Systems
Mobile Communications
Telemetry and Remote Systems

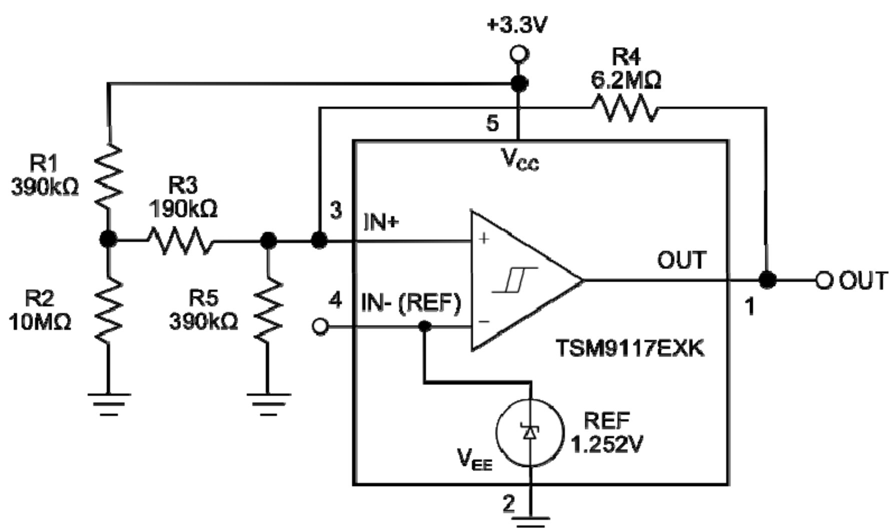
DESCRIPTION

The TSM9117–TSM9120 family of nanopower comparators is electrically and form-factor identical to the MAX9117-MAX9120 family of analog comparators. Ideally suited for all 2-cell battery-management/monitoring applications, these 5-pin SC70 analog comparators guarantee +1.6V operation, draw very little supply current, and have robust input stages that can tolerate input voltages beyond the power supply. The TSM9117 and the TSM9118 draw 600nA of supply current and include an on-board 1.252V ±1.75% reference. The comparator-only TSM9119 and the TSM9120 draw a supply current of 350nA.

The TSM9117 and TSM9119's push-push output drivers were designed to drive 5mA loads from one supply rail to the other supply rail. The TSM9118 and the TSM9120's open-drain output stages make it easy to incorporate these comparators into systems that operate on different supply voltages.

TYPICAL APPLICATION CIRCUIT

Nanopower 2.9V V_{CC} Threshold Detector



PART	INTERNAL REFERENCE	OUTPUT TYPE	SUPPLY CURRENT (nA)
TSM9117	Yes	Push-Pull	600
TSM9118	Yes	Open-Drain	600
TSM9119	No	Push-Pull	350
TSM9120	No	Open-Drain	350

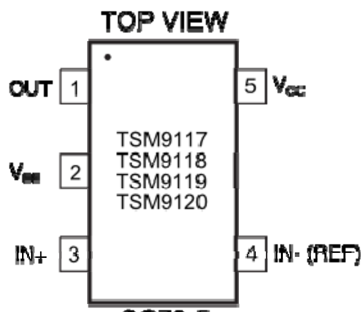
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) .... +6V
Voltage Inputs (IN+, IN-, REF) .... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Output Voltage
TSM9117/9119 .... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
TSM9118/9120 ....(V_{EE} - 0.3V) to +6V
Current Into Input Pins .... ±20mA
Output Current .... ±50mA
Output Short-Circuit Duration 10s

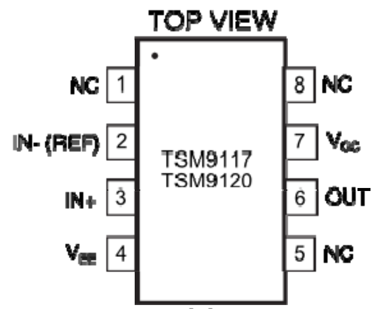
Continuous Power Dissipation (T_A = +70°C)
5-Pin SC70 (Derate 2.5mW/°C above +70°C) 200mW
8-Pin SOIC (Derate 5.88mW/°C above +70°C) 471mW
Operating Temperature Range .... -40°C to +85°C
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°

Electrical and thermal stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

PACKAGE/ORDERING INFORMATION



SC70-5
XK Package
IN- (REF) Pin 4 - TSM9117/TSM9118 only



SO-8
SA Package
IN- (REF) Pin 2 - TSM9117 only

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY	ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM9117EXK+T	TAA	Tape & Reel	3000	TSM9117ESA+	TS9117E	Tube	97
TSM9118EXK+T	TAB	Tape & Reel	3000	TSM9117ESA+T		Tape & Reel	2500
TSM9119EXK+T	TAC	Tape & Reel	3000	TSM9120ESA+	TS9120E	Tube	97
TSM9120EXK+T	TAD	Tape & Reel	3000	TSM9120ESA+T		Tape & Reel	2500

Lead-free Program: Touchstone Semiconductor supplies only lead-free packaging.

Consult Touchstone Semiconductor for products specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS: TSM9117 & TSM9118

V_{CC} = +5V, V_{EE} = 0V, V_{IN+} = V_{REF}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. See Note 1.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Inferred from the PSRR test	T_A = +25°C	1.6		5.5	V
			T_A = T_{MIN} to T_{MAX}	1.8		5.5	
Supply Current	I_{CC}	V_{CC} = 1.6V	T_A = +25°C		0.6	1	μA
		V_{CC} = 5V	T_A = +25°C		0.68	1.30	
			T_A = T_{MIN} to T_{MAX}			1.60	
IN+ Voltage Range	V_{IN+}	Inferred from the output swing test		V_{EE} - 0.2		V_{CC} + 0.2	V
Input Offset Voltage	V_{OS}	(Note 2)	T_A = +25°C		1	5	mV
			T_A = T_{MIN} to T_{MAX}			10	
Input-Referred Hysteresis	V_{HB}	(Note 3)			4		mV
Input Bias Current	I_B	T_A = +25°C			0.15	1	nA
		T_A = T_{MIN} to T_{MAX}				2	
Power-Supply Rejection Ratio	PSRR	V_{CC} = 1.6V to 5.5V, T_A = +25°C			0.1	1	mV/V
		V_{CC} = 1.8V to 5.5V, T_A = T_{MIN} to T_{MAX}				1	mV/V
Output-Voltage Swing High	V_{CC} - V_{OH}	TSM9117, V_{CC} = 5V, I_{SOURCE} = 5mA	T_A = +25°C		190	400	mV
			T_A = T_{MIN} to T_{MAX}			500	
		TSM9117, I_{SOURCE} = 1mA	V_{CC} = 1.6V, T_A = +25°C		100	200	
			V_{CC} = 1.8V, T_A = T_{MIN} to T_{MAX}			300	
Output-Voltage Swing Low	V_{OL}	V_{CC} = 5V, I_{SINK} = 5mA	T_A = +25°C		190	400	mV
			T_A = T_{MIN} to T_{MAX}			500	
		I_{SINK} = 1mA	V_{CC} = 1.6V, T_A = +25°C		100	200	
			V_{CC} = 1.8V, T_A = T_{MIN} to T_{MAX}			300	
Output Leakage Current	I_{LEAK}	TSM9118 only, V_O = 5.5V			0.002	1	μA
Output Short-Circuit Current	I_{SC}	Sourcing, V_O = V_{EE}	V_{CC} = 5V		35		mA
			V_{CC} = 1.6V		3		
		Sinking, V_O = V_{CC}	V_{CC} = 5V		35		
			V_{CC} = 1.6V		3		
High-to-Low Propagation Delay (Note 4)	t_{PD-}	V_{CC} = 1.6V			16		μs
		V_{CC} = 5V			14		
Low-to-High Propagation Delay (Note 4)	t_{PD+}	TSM9117 only	V_{CC} = 1.6V		15		μs
			V_{CC} = 5V		40		
		TSM9118 only	V_{CC} = 1.6V, R_{PULLUP} = 100kΩ		16		
			V_{CC} = 5V, R_{PULLUP} = 100kΩ		45		
Rise Time	t_{RISE}	TSM9117 only, C_L = 15pF			1.6		μs
Fall Time	t_{FALL}	C_L = 15pF			0.2		μs
Power-Up Time	t_{ON}				1.2		ms
Reference Voltage	V_{REF}	T_A = +25°C		1.230	1.252	1.274	V
		T_A = T_{MIN} to T_{MAX}		1.196		1.308	
Reference Voltage Temperature Coefficient	TCV_{REF}				100		ppm/°C
Reference Output Voltage Noise	e_n	BW = 10Hz to 100kHz			1.1		mV_{RMS}
		BW = 10Hz to 100kHz, C_{REF} = 1nF			0.2		
Reference Line Regulation	$\Delta V_{REF}/ \Delta V_{CC}$	V_{CC} = 1.6V to 5.5V			0.25		mV/V
Reference Load Regulation	$\Delta V_{REF}/ \Delta I_{OUT}$	ΔI_{OUT} = 10nA			±1		mV/nA

ELECTRICAL CHARACTERISTICS: TSM9119 & TSM9120

V_{CC} = +5V, V_{EE} = 0V, V_{CM} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. See Note 1.

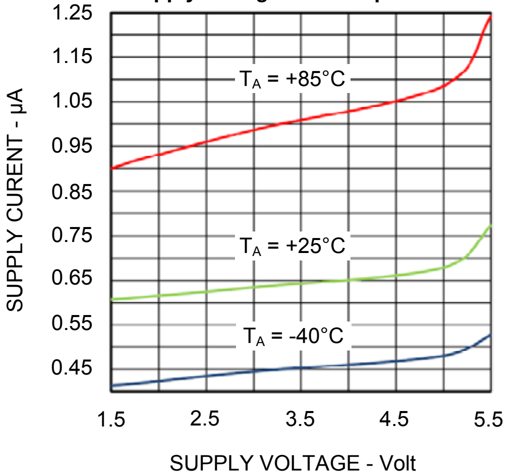
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Inferred from the PSRR test	T_A = +25°C	1.6		5.5	V
			$T_A = T_{MIN}$ to T_{MAX}	1.8		5.5	
Supply Current	I_{CC}	V_{CC} = 1.6V	T_A = +25°C		0.35	0.80	µA
		V_{CC} = 5V	T_A = +25°C		0.45	0.80	
			$T_A = T_{MIN}$ to T_{MAX}			1.20	
Input Common-Mode Voltage Range	V_{CM}	Inferred from the CMRR test		V_{EE} - 0.2		V_{CC} + 0.2	V
Input Offset Voltage	V_{OS}	-0.2V ≤ V_{CM} ≤ (V_{CC}+0.2V) (Note 2)	T_A = +25°C		1	5	mV
			$T_A = T_{MIN}$ to T_{MAX}			10	
Input-Referred Hysteresis	V_{HB}	-0.2V ≤ V_{CM} ≤ (V_{CC}+0.2V) (Note 3)			4		mV
Input Bias Current	I_B	T_A = +25°C			0.15	1	nA
		$T_A = T_{MIN}$ to T_{MAX}				2	
Input Offset Current	I_{OS}				75		pA
Power-Supply Rejection Ratio	PSRR	V_{CC} = 1.6V to 5.5V, T_A = +25°C			0.1	1	mV/V
		V_{CC} = 1.8V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}				1	mV/V
Common-Mode Rejection Ratio	CMRR	(V_{EE} - 0.2V) ≤ V_{CM} ≤ (V_{CC} + 0.2V)			0.5	3	mV/V
Output-Voltage Swing High	V_{CC} - V_{OH}	TSM9119 only, V_{CC} = 5V, I_{SOURCE} = 5mA	T_A = +25°C		190	400	mV
			$T_A = T_{MIN}$ to T_{MAX}			500	
		TSM9119 only, I_{SOURCE} = 1mA	V_{CC} = 1.6V, T_A = +25°C		100	200	
			V_{CC} = 1.8V, $T_A = T_{MIN}$ to T_{MAX}			300	
Output-Voltage Swing Low	V_{OL}	V_{CC} = 5V, I_{SINK} = 5mA	T_A = +25°C		190	400	mV
			$T_A = T_{MIN}$ to T_{MAX}			500	
		I_{SINK} = 1mA	V_{CC} = 1.6V, T_A = +25°C		100	200	
			V_{CC} = 1.8V, $T_A = T_{MIN}$ to T_{MAX}			300	
Output Leakage Current	I_{LEAK}	TSM9120 only, V_O = 5.5V			0.001	1	µA
Output Short-Circuit Current	I_{SC}	Sourcing, $V_O = V_{EE}$	V_{CC} = 5V		35		mA
			V_{CC} = 1.6V		3		
		Sinking, $V_O = V_{CC}$	V_{CC} = 5V		35		
			V_{CC} = 1.6V		3		
High-to-Low Propagation Delay (Note 4)	t_{PD-}	V_{CC} = 1.6V			16		µs
		V_{CC} = 5V			14		
Low-to-High Propagation Delay (Note 4)	t_{PD+}	TSM9119 only	V_{CC} = 1.6V		15		µs
			V_{CC} = 5V		40		
		TSM9120 only	V_{CC} = 1.6V, R_{PULLUP} = 100kΩ		16		
			V_{CC} = 5V, R_{PULLUP} = 100kΩ		45		
Rise Time	t_{RISE}	TSM9119 only, C_L = 15pF			1.6		µs
Fall Time	t_{FALL}	C_L = 15pF			0.2		µs
Power-Up Time	t_{ON}				1.2		ms

Note 1: All specifications are 100% tested at T_A = +25°C. Specification limits over temperature ($T_A = T_{MIN}$ to T_{MAX}) are guaranteed by design, not production tested.
Note 2: V_{OS} is defined as the center of the hysteresis band at the input.
Note 3: The hysteresis-related trip points are defined by the edges of the hysteresis band, measured with respect to the center of the hysteresis band (i.e., V_{OS}) (See Figure 2).
Note 4: Specified with an input overdrive ($V_{OVERDRIVE}$) of 100mV, and load capacitance of C_L = 15pF. $V_{OVERDRIVE}$ is defined above and beyond the offset voltage and hysteresis of the comparator input. For the TSM9117/TSM9118, reference voltage error should also be added.

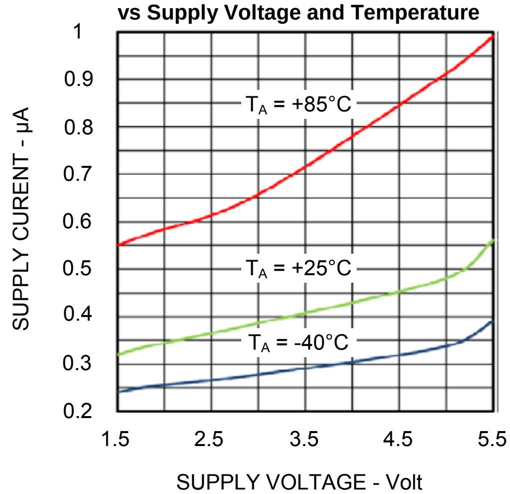
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = +5V; V_{EE} = 0V; C_L = 15pF; $V_{OVERDRIVE}$ = 100mV; T_A = +25°C, unless otherwise noted.

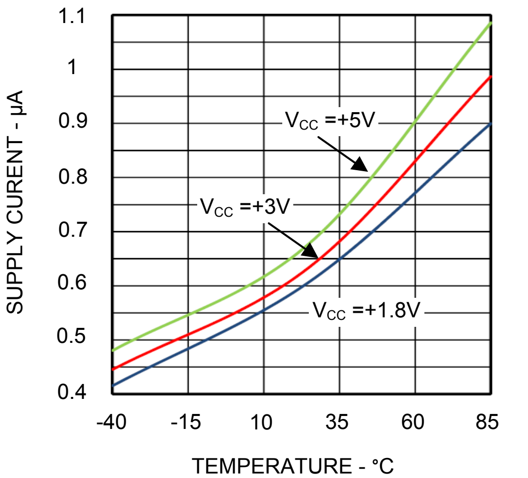
TSM9117/9118 Supply Current vs Supply Voltage and Temperature



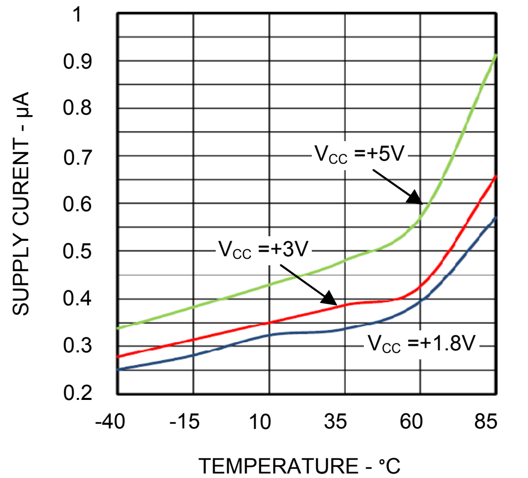
TSM9119/9120 Supply Current vs Supply Voltage and Temperature



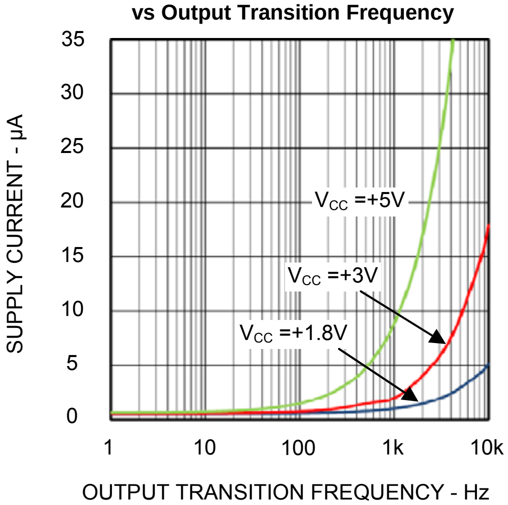
TSM9117/9118 Supply Current vs Temperature



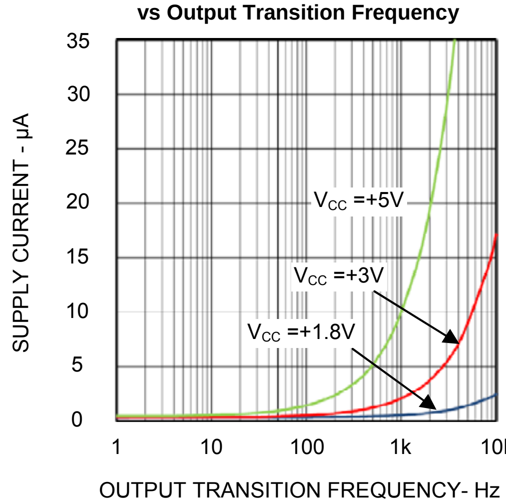
TSM9119/9120 Supply Current vs Temperature



TSM9117/9118 Supply Current vs Output Transition Frequency



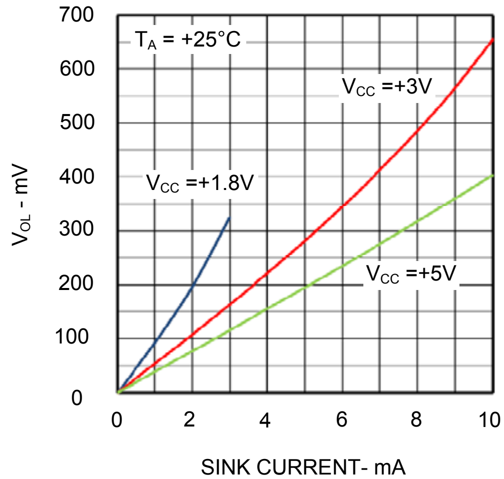
TSM9119/9120 Supply Current vs Output Transition Frequency



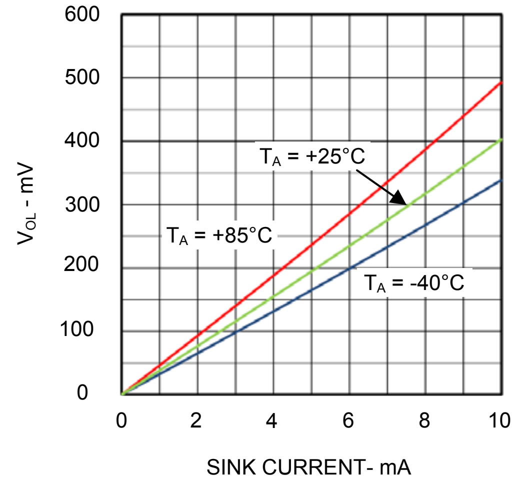
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = +5V; V_{EE} = 0V; C_L = 15pF; $V_{OVERDRIVE}$ = 100mV; T_A = +25°C, unless otherwise noted.

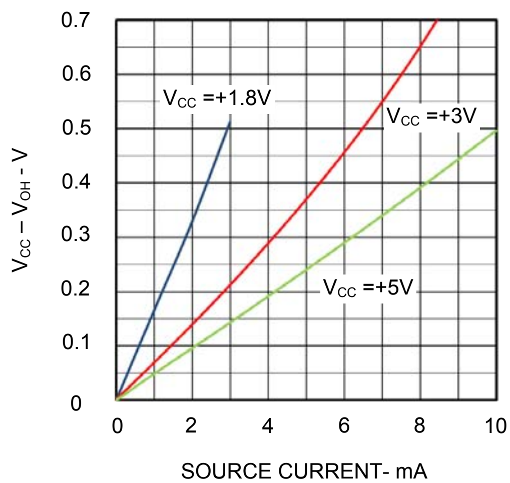
Output Voltage Low vs. Sink Current



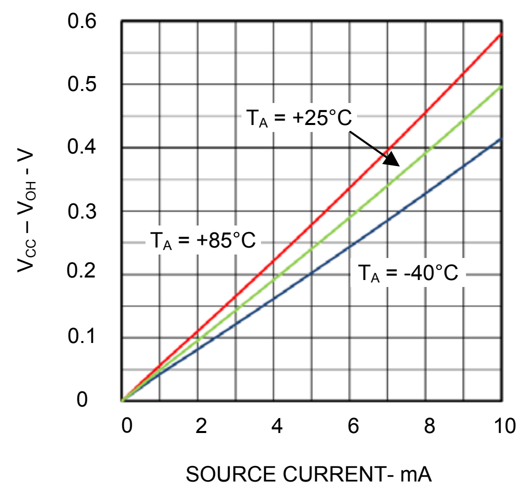
Output Voltage Low vs. Sink Current and Temperature



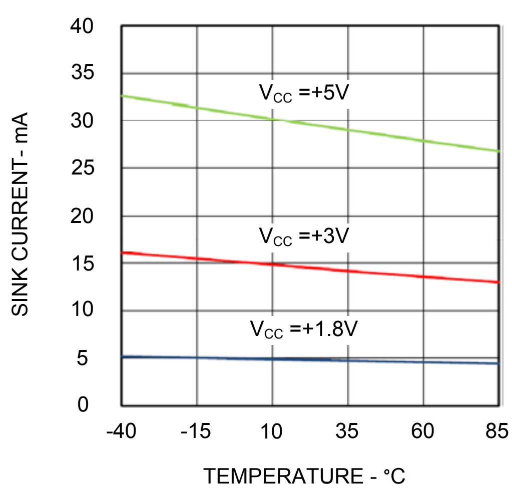
TSM9117/9119 Output Voltage High vs Source Current



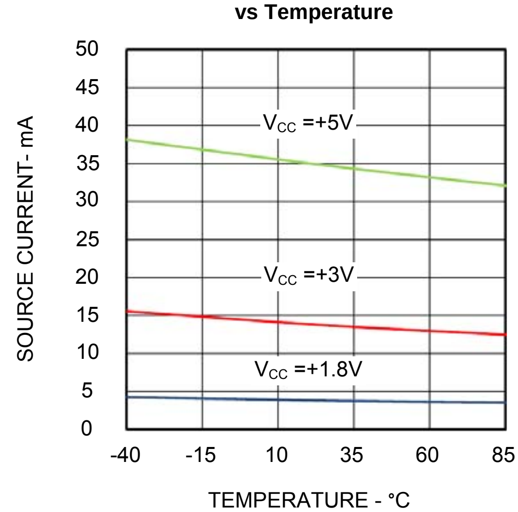
TSM9117/9119 Output Voltage High vs Source Current and Temperature



Short-Circuit Sink Current vs Temperature



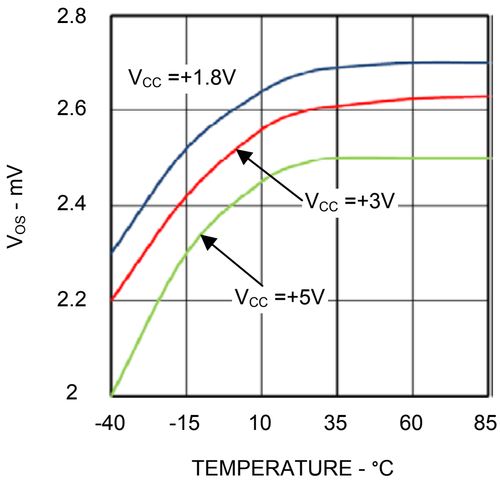
TSM9117/9119 Short-Circuit Source Current vs Temperature



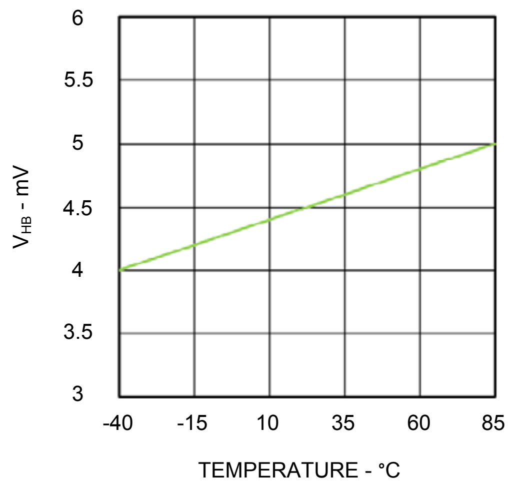
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = +5V; V_{EE} = 0V; C_L = 15pF; $V_{OVERDRIVE}$ = 100mV; T_A = +25°C, unless otherwise noted.

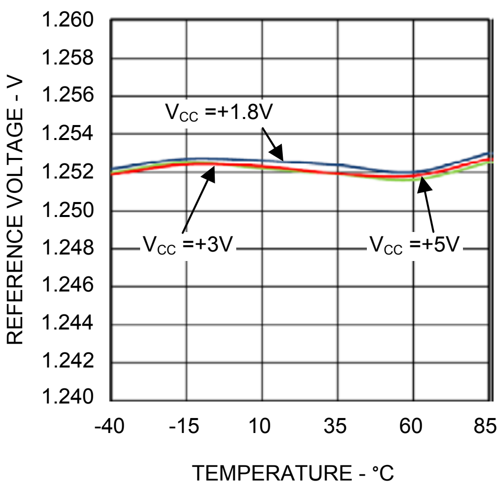
Offset Voltage vs Temperature



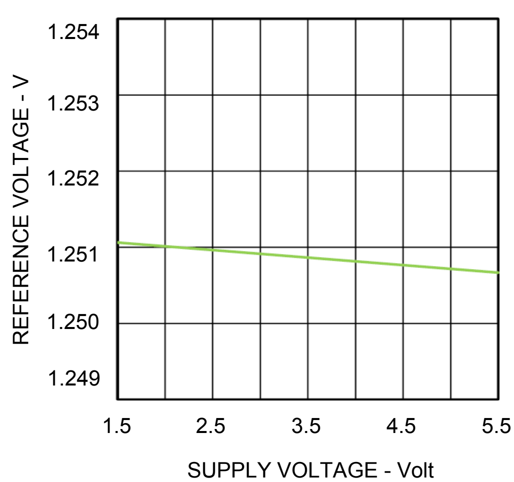
Hysteresis Voltage vs Temperature



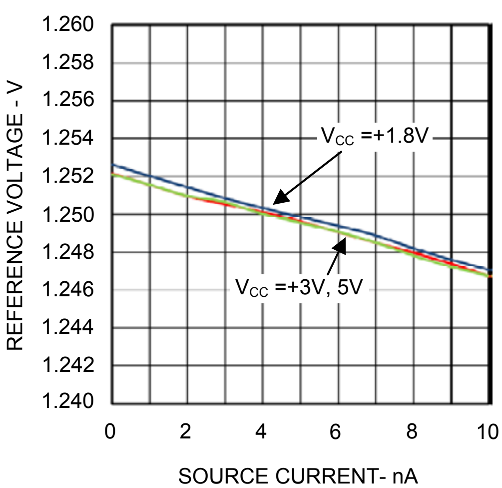
TSM9117/9118 Reference Voltage vs Temperature



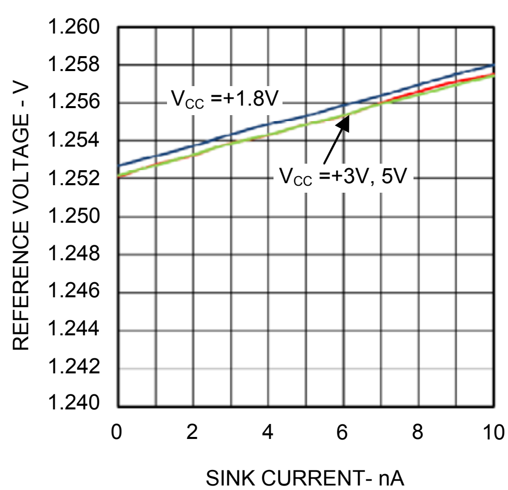
TSM9117/9118 Reference Voltage vs Supply Voltage



TSM9117/9118 Reference Voltage vs Reference Source Current



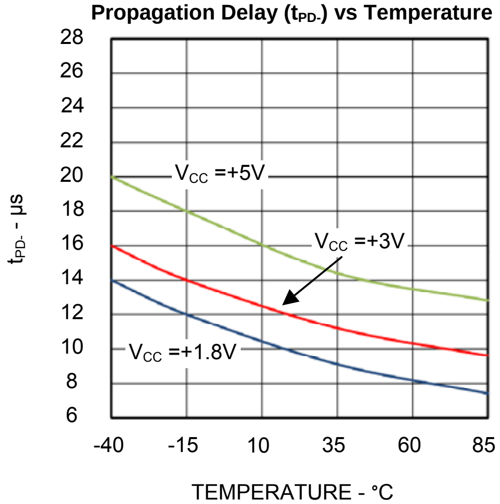
TSM9117/9118 Reference Voltage vs Reference Sink Current



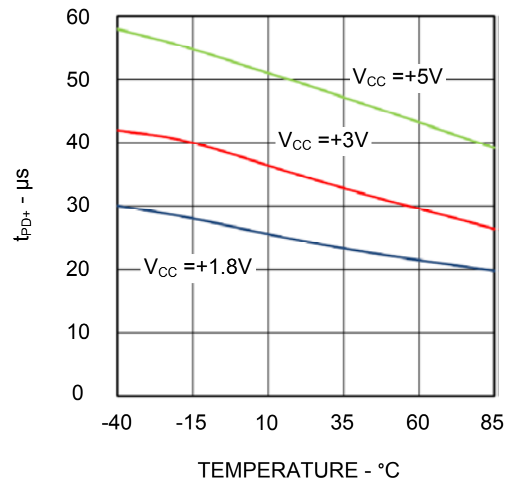
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = +5V; V_{EE} = 0V; C_L = 15pF; $V_{OVERDRIVE}$ = 100mV; T_A = +25°C, unless otherwise noted.

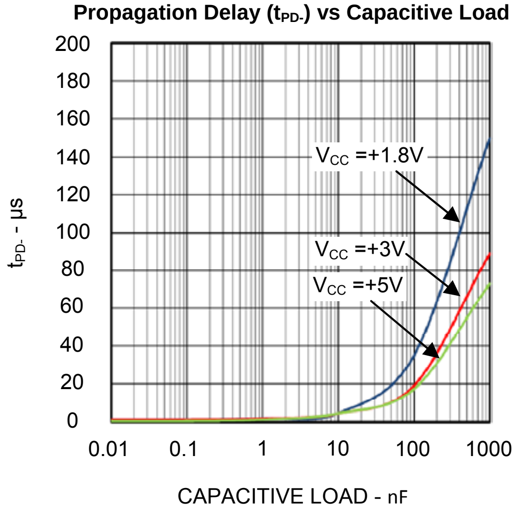
Propagation Delay (t_{PD-}) vs Temperature



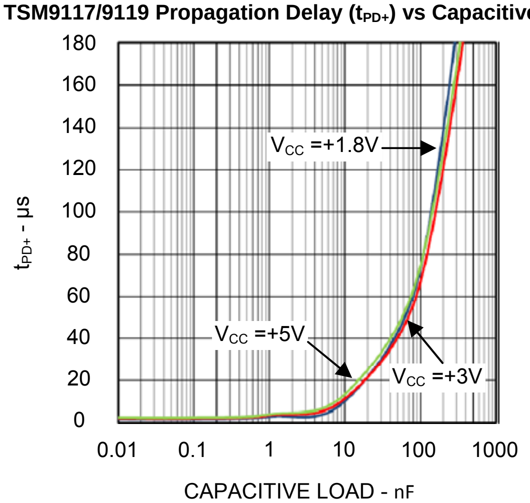
TSM9117/9119 Propagation Delay (t_{PD+}) vs Temperature



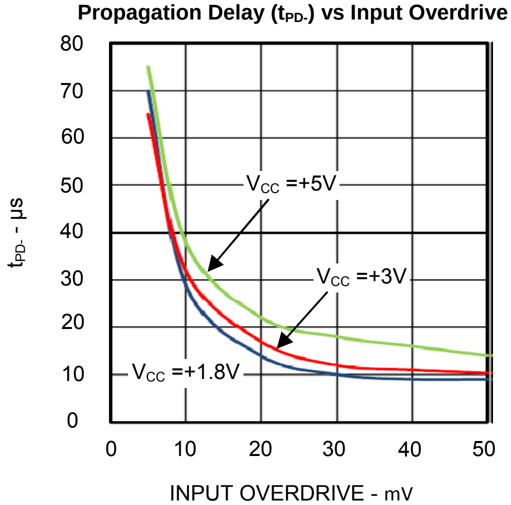
Propagation Delay (t_{PD-}) vs Capacitive Load



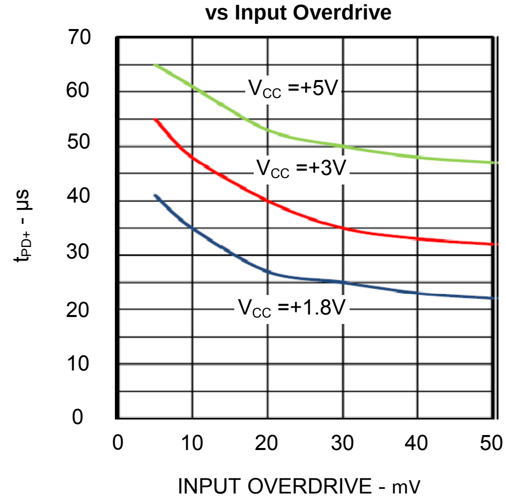
TSM9117/9119 Propagation Delay (t_{PD+}) vs Capacitive Load



Propagation Delay (t_{PD-}) vs Input Overdrive



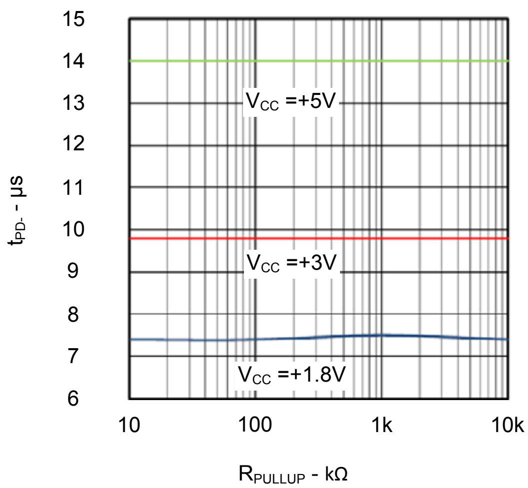
TSM9117/9119 Propagation Delay (t_{PD+}) vs Input Overdrive



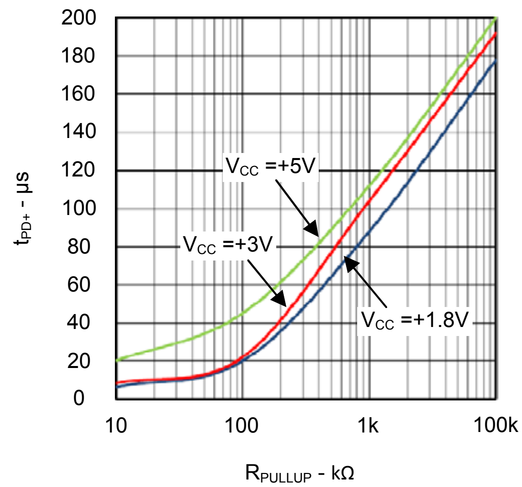
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = +5V; V_{EE} = 0V; C_L = 15pF; $V_{OVERDRIVE}$ = 100mV; T_A = +25°C, unless otherwise noted.

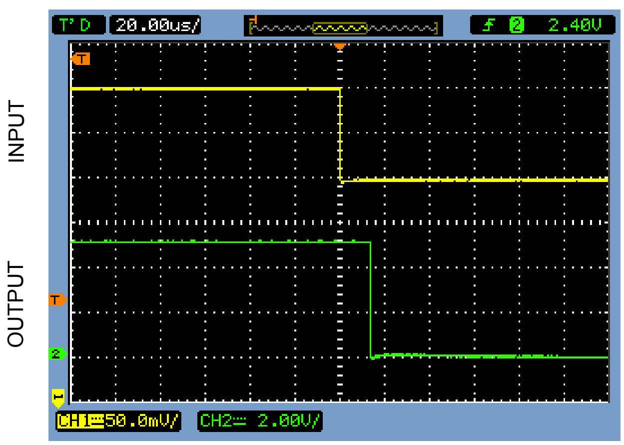
TSM9118/9120 Propagation Delay (t_{PD-}) vs Pullup Resistance



TSM9118/9120 Propagation Delay (t_{PD+}) vs Pullup Resistance

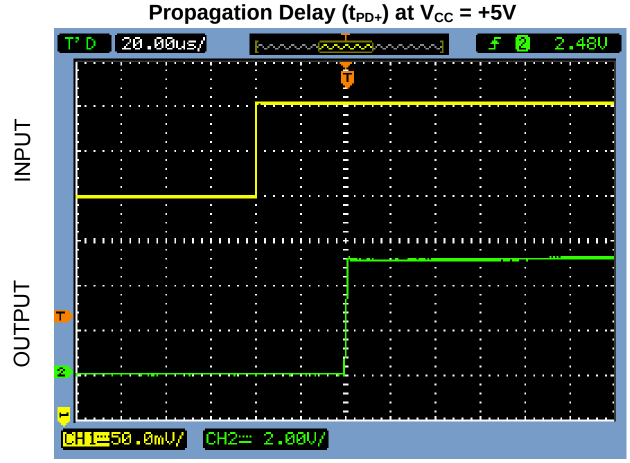


Propagation Delay (t_{PD-}) at V_{CC} = +5V



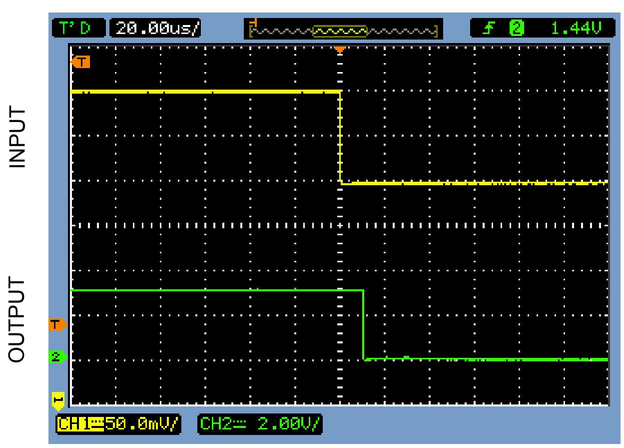
20µs/DIV

TSM9117/9119
Propagation Delay (t_{PD+}) at V_{CC} = +5V



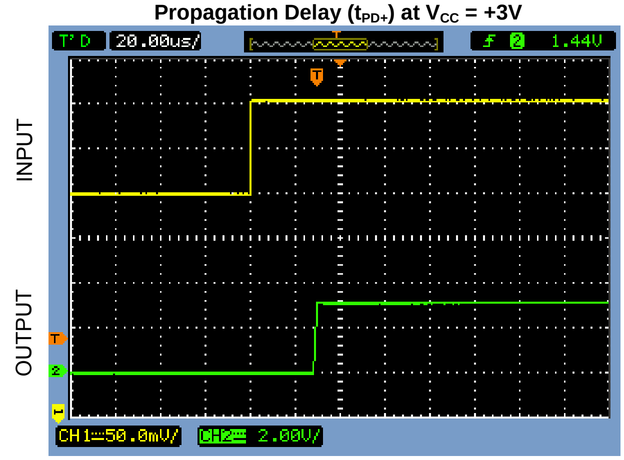
20µs/DIV

Propagation Delay (t_{PD-}) at V_{CC} = +3V



20µs/DIV

TSM9117/9119
Propagation Delay (t_{PD+}) at V_{CC} = +3V

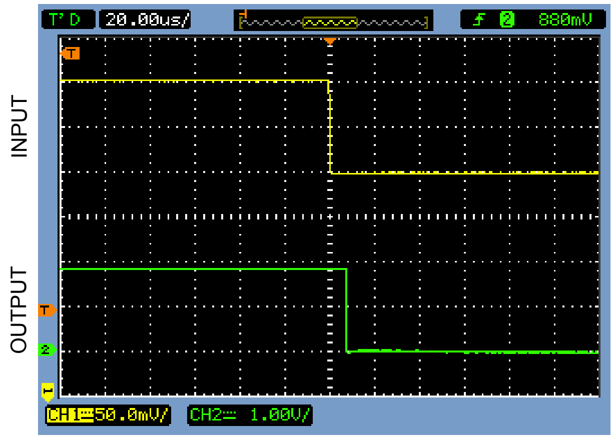


20µs/DIV

TYPICAL PERFORMANCE CHARACTERISTICS

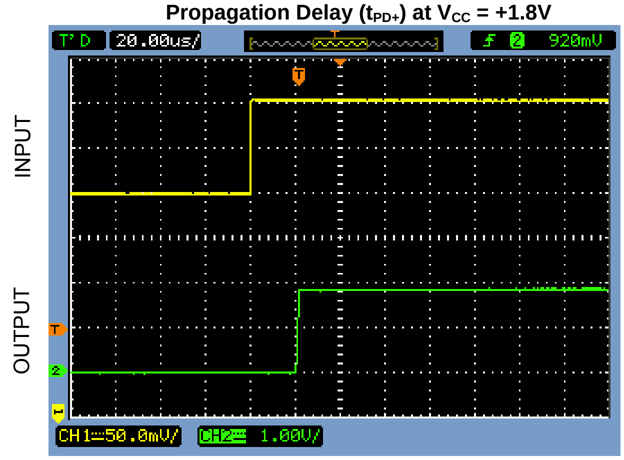
V_{CC} = +5V; V_{EE} = 0V; C_L = 15pF; $V_{OVERDRIVE}$ = 100mV; T_A = +25°C, unless otherwise noted.

Propagation Delay (t_{PD-}) at V_{CC} = +1.8V



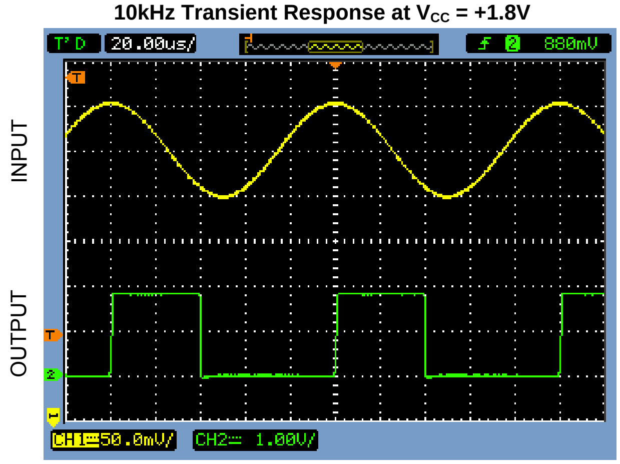
20µs/DIV

TSM9117/9119
Propagation Delay (t_{PD+}) at V_{CC} = +1.8V



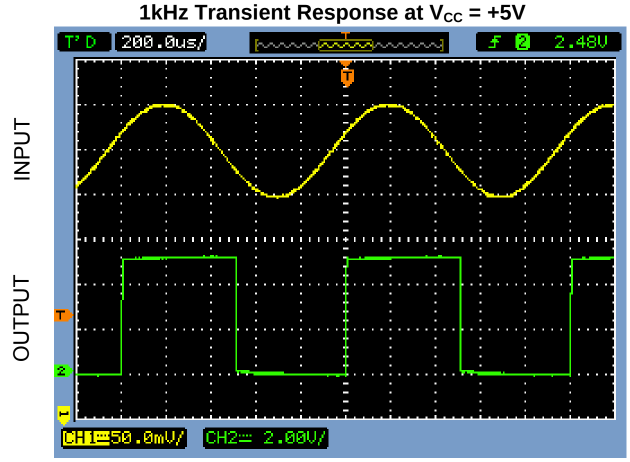
20µs/DIV

TSM9117/9119
10kHz Transient Response at V_{CC} = +1.8V



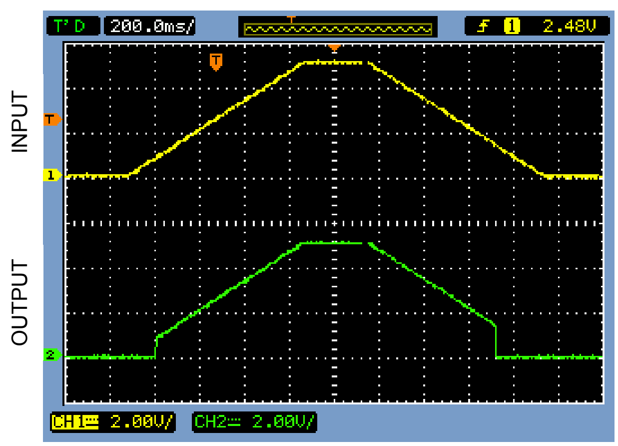
20µs/DIV

TSM9117/9119
1kHz Transient Response at V_{CC} = +5V



200µs/DIV

Power-Up/Power-Down Transient Response

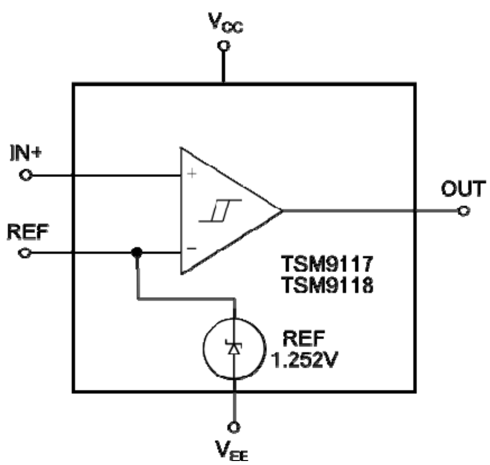


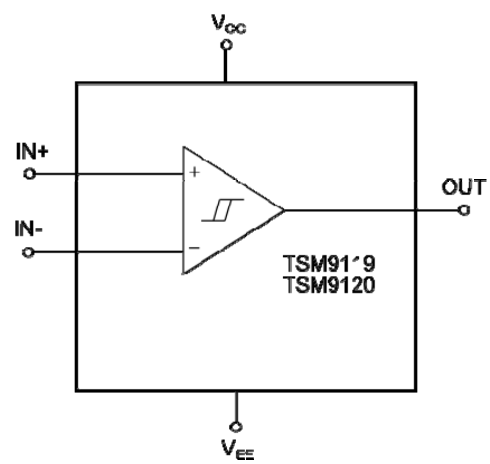
0.2s/DIV

PIN FUNCTIONS

TSM9117/TSM9118		TSM9119/TSM9120		NAME	FUNCTION
SC70	SO	SC70	SO		
1	6	1	6	OUT	Comparator Output
2	4	2	4	VEE	Negative Supply Voltage
3	3	3	3	IN+	Comparator Noninverting Input
4	2	—	—	REF	1.252V Reference Output and Comparator Inverting Input
5	7	5	7	VCC	Positive Supply Voltage
—	—	4	2	IN-	Comparator Inverting Input
—	1, 5, 8	—	1, 5, 8	NC	No Connection. Not internally connected.

BLOCK DIAGRAMS





DESCRIPTION OF OPERATION

Guaranteed to operate from +1.6V supplies, the TSM9117 and the TSM9118 comparators only draw 600nA supply current, feature a robust input stage that can tolerate input voltages 200mV beyond the power supply rails, and include an on-board +1.252V ±1.75% voltage reference. The comparator-only TSM9119 and the TSM9120 have the same attributes and only draw a supply current of 350nA. To insure clean output switching behavior, all four analog comparators feature 4mV internal hysteresis. The TSM9117 and the TSM9119's push-pull output drivers were designed to minimize supply-current surges while driving ±5mA loads with rail-to-rail output swings. The open-drain output stage TSM9118 and TSM9120 can be connected to supply voltages above V_{CC} to an absolute maximum of 6V above V_{EE}. Where wired-OR logic connections are needed, their open-drain output stages make it easy to use these analog comparators.

Input Stage Circuitry

The robust design of the analog comparators' input stage can accommodate any differential input voltage from V_{EE} - 0.2V to V_{CC} + 0.2V. Input bias currents are typically ±0.15nA so long as the applied input voltage remains between the supply rails. ESD protection diodes - connected internally to the supply rails - protect comparator inputs against overvoltage conditions. However, if the applied input voltage exceeds either or both supply rails, an increase in input current can occur when these ESD protection diodes start to conduct.

Output Stage Circuitry

Many conventional analog comparators can draw orders of magnitude higher supply current when switching. Because of this behavior, additional power supply bypass capacitance may be required to provide additional charge storage during switching. The design of the TSM9117–TSM9120's rail-to-rail output stage implements a technique that virtually eliminates supply-current surges when output transitions occur. As shown on Page 5 of the Typical Operating Characteristics, the supply-current change as a function of output transition frequency exhibited by this analog comparator family is very small. Material benefits of this attribute to battery-power applications is the increase in operating time and in reducing the size of power-supply filter capacitors.

TSM9117/9118's Internal +1.252V V_{REF}

The TSM9117 and the TSM9118's internal +1.252V voltage reference exhibits a typical temperature coefficient of 100ppm/°C over the full -40°C to +85°C temperature range. An equivalent circuit for the reference section is illustrated in Figure 1. Since the output impedance of the voltage reference is typically 200kΩ, preventing the reference from driving large loads. The reference is typically 200kΩ, its output can be bypassed with a low-leakage capacitor and is stable for any capacitive load. An external buffer – such as the TS1001 – can be used to buffer the voltage reference output for higher output current drive or to reduce reference output impedance.

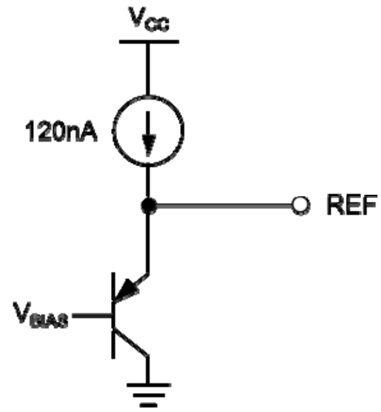


Figure 1: TSM9117 & TSM9118 Internal V_{REF} Output Equivalent Circuit

APPLICATIONS INFORMATION

Low-Voltage, Low-Power Operation

Designed specifically for low-power applications, the TSM9117–TSM9120 comparators are an excellent choice. Under nominal conditions, approximate operating times for this analog comparator family is illustrated in Table 1 for a number of battery types and their charge capacities.

Internal Hysteresis

As a result of circuit noise or unintended parasitic feedback, many analog comparators often break into oscillation within their linear region of operation especially when the applied differential input voltage approaches 0V (zero volt). Externally-introduced hysteresis is a well-established technique to stabilizing analog comparator behavior and requires external components. As shown in Figure 2, adding comparator hysteresis creates two trip points: V_{THR} (for the rising input voltage) and V_{THF} (for the falling input voltage). The hysteresis band (V_{HB}) is defined as the voltage difference between the two trip points. When a comparator's input voltages are equal,

Table 1: Battery Applications using the TSM9117- TSM9120

BATTERY TYPE	RECHARGEABLE	V_{FRESH} (V)	$V_{END-OF-LIFE}$ (V)	CAPACITY, AA SIZE (mA-h)	TSM9117/TSM9118 OPERATING TIME (hrs)	TSM9119/TSM9120 OPERATING TIME (hrs)
Alkaline (2 Cells)	No	3.0	1.8	2000	2.5×10^6	5×10^6
Nickel-Cadmium (2 Cells)	Yes	2.4	1.8	750	937,500	1.875×10^6
Lithium-Ion (1 Cell)	Yes	3.5	2.7	1000	1.25×10^6	2.5×10^6
Nickel-Metal-Hydride (2 Cells)	Yes	2.4	1.8	1000	1.25×10^6	2.5×10^6

hysteresis effectively forces one comparator input to move quickly past the other input, moving the input out of the region where oscillation occurs. out of the region where oscillation occurs. Figure 2 illustrates the case in which an IN- input is a fixed voltage and an IN+ is varied. If the input signals were reversed, the figure would be the same with an inverted output. To save cost and external pcb area, an internal 4mV hysteresis circuit was added to the TSM9117–TSM9120.

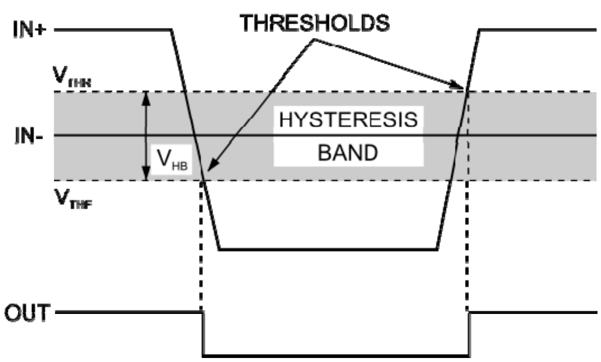


Figure 2: TSM9117-TSM9120 Threshold Hysteresis Band

Adding Hysteresis to the TSM9117/TSM9119

The TSM9117/TSM9119 exhibit an internal hysteresis band (V_{HYSB}) of 4mV. Additional hysteresis can be generated with three external resistors using positive feedback as shown in Figure 3. Unfortunately, this method also reduces the

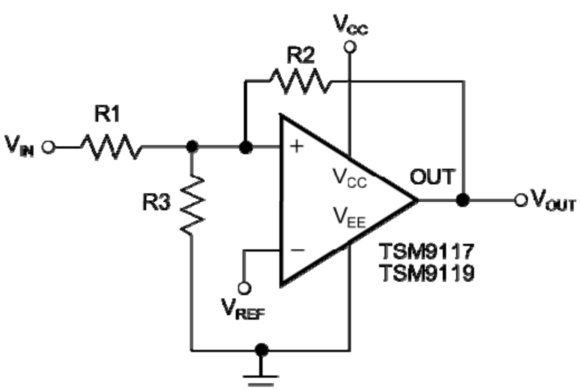


Figure 3: Using Three Resistors Introduces Additional Hysteresis in the TSM9117 & TSM9119.

hysteresis response time. Use the following procedure to calculate resistor values.

1) Setting R2. As the leakage current at the IN pin is less than 2nA, the current through R2 should be at least 0.2µA to minimize offset voltage errors caused by the input leakage current. The current through R2 at the trip point is (V_{REF} - V_{OUT})/R2.
   In solving for R2, there are two formulas – one each for the two possible output states:

   $R2 = V_{REF}/I_{R2}$

   or

   $R2 = (V_{CC} - V_{REF})/I_{R2}$

   From the results of the two formulae, the smaller of the two resulting resistor values is chosen. For example, when using the TSM9117 (V_{REF} = 1.252V) at a V_{CC} = 3.3V and if I_{R2} = 0.2µA is chosen, then the formulae above produce two resistor values: 6.26MΩ and 10.24MΩ - the 6.2MΩ standard value for R2 is selected.

2) Next, the desired hysteresis band (V_{HYSB}) is set. In this example, V_{HYSB} is set to 100mV.

3) Resistor R1 is calculated according to the following equation:

   $R1 = R2 \times (V_{HYSB}/V_{CC})$

   and substituting the values selected in 1) and 2) above yields:

   R1 = 6.2MΩ x (100mV/3.3V) = 187.88kΩ.

   The 187kΩ standard value for R1 is chosen.

4) The trip point for V_{IN} rising (V_{THR}) is chosen such that $V_{THR} > V_{REF} \times (R1 + R2)/R2$ (V_{THF} is the trip point for V_{IN} falling). This is the threshold voltage at which the comparator switches its output from low to high as V_{IN} rises above the trip point. In this example, V_{THR} is set to 3V.

5) With the V_{THR} from Step 4 above, resistor R3 is then computed as follows:

   $R3 = 1/[V_{THR}/(V_{REF} \times R1) - (1/R1) - (1/R2)]$

   R3 = 1/[3V/(1.252V x 187kΩ) - (1/187kΩ) - (1/6.2MΩ)] = 136.9kΩ

In this example, a 137kΩ, 1% standard value resistor is selected for R3.

6) The last step is to verify the trip voltages and hysteresis band using the standard resistance values:

For $_{VIN}$ rising:

$V_{THR} = V_{REF} \times R1 [(1/R1) + (1/R2) + (1/R3)] = 3V$

and, for V_{IN} falling:

$V_{THF} = V_{THR} - (R1 \times V_{CC}/R2) = 2.9V$

and Hysteresis Band = $V_{THR} – V_{THF}$ = 100mV

Adding Hysteresis to the TSM9118/TSM9120

The TSM9118/TSM9120 have a 4mV internal hysteresis band. Both products have open-drain outputs and require an external pullup resistor to V_{CC} as shown in Figure 4. Additional hysteresis can be

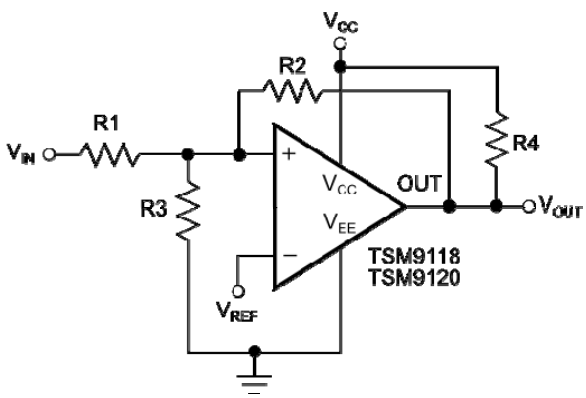


Figure 4: Using Four Resistors Introduces Additional Hysteresis in the TSM9118 & TSM9120.

generated using positive feedback; however, the formulae differ slightly from those of the TSM9117/TSM9119. The procedure to calculate the resistor values for the TSM9118/TSM9120 is as follows:

1) As in the previous section, resistor R2 is chosen according to the formulae:

$R2 = V_{REF}/0.2\mu A$

or

$R2 = (V_{CC} - V_{REF})/0.2\mu A - R4$

where the smaller of the two resulting resistor values is the best starting value.

2) As before, the desired hysteresis band (V_{HYSB}) is set to 100mV.

3) Next, resistor R1 is then computed according to the following equation:

$R1 = (R2 + R4) \times (V_{HYSB}/V_{CC})$

4) The trip point for V_{IN} rising (V_{THR}) is chosen (again, remember that V_{THF} is the trip point for V_{IN} falling). This is the threshold voltage at which the comparator switches its output from low to high as V_{IN} rises above the trip point.

5) With the V_{THR} from Step 4 above, resistor R3 is computed as follows:

$R3 = 1/[V_{THR}/(V_{REF} \times R1) - (1/R1) - (1/R2)]$

6) As before, the last step is to verify the trip voltages and hysteresis band with the standard resistor values used in the circuit:

For V_{IN} rising:

$V_{THR} = V_{REF} \times R1 \times (1/R1+1/R2+1/R3)$

and, for V_{IN} falling:

$V_{THF} = V_{REF} \times R1 \times [1/R1+1/R3+1/(R2+R4)] -[R1/(R2+R4)] \times V_{CC}$

and Hysteresis Band is given by $V_{THR} - V_{THF}$

PC Board Layout and Power-Supply Bypassing

While power-supply bypass capacitors are not typically required, it is good engineering practice to use 0.1µF bypass capacitors close to the device's power supply pins when the power supply impedance is high, the power supply leads are long, or there is excessive noise on the power supply traces. To reduce stray capacitance, it is also good engineering practice to make signal trace lengths as short as possible. Also recommended are a ground plane and surface mount resistors and capacitors.

A Zero-Crossing Detector

To configure a zero-crossing detector using a TSM9119 is illustrated in Figure 5. In this example, the TSM9119's inverting input is connected to ground and its noninverting input is connected to a 100mV$_{P-P}$ signal source. The TSM9119's output changes state as the signal at the noninverting input crosses 0V.

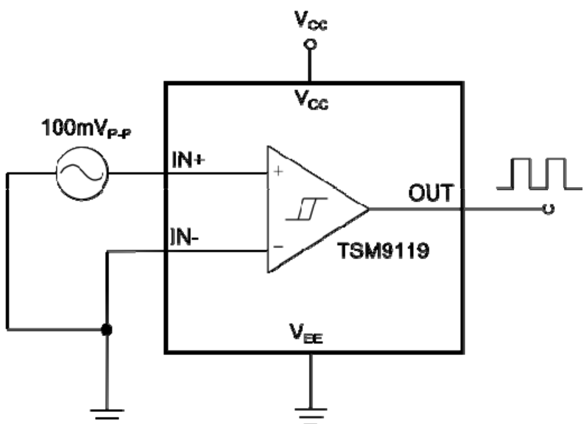


Figure 5: A Simple Zero-Crossing Detector

A Logic-Level Translator

Logic-level translation between two different voltage systems is easy using the TSM9120 as shown in Figure 6. This application circuit converts 5V logic to

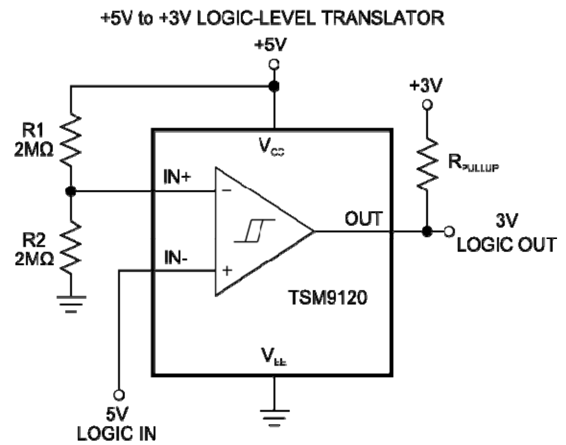


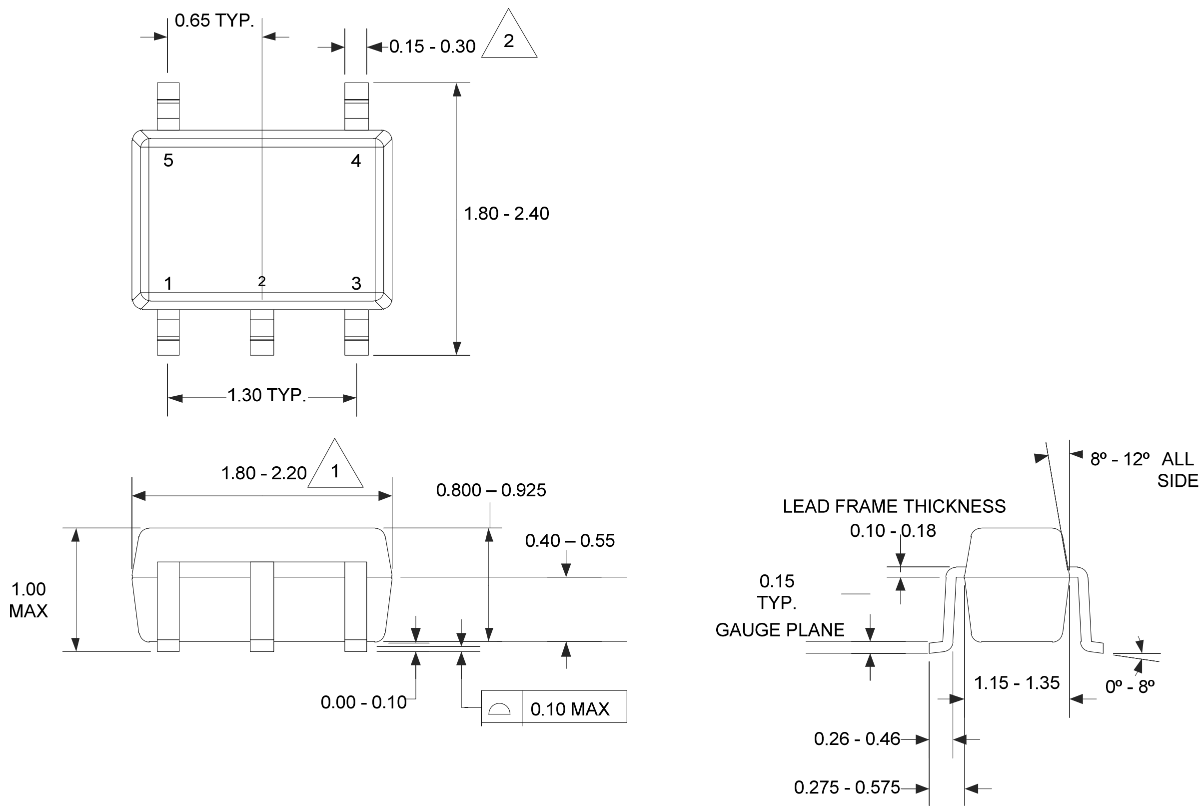
Figure 6: A 5V-to-3V Logic Level Translator

3V logic levels. In this case, the TSM9120 is powered by a +5V system and the external pullup resistor for the TSM9120's open-drain output is connected to a +3V system. This configuration allows the full 5V logic swing without creating overvoltage on the 3V logic inputs. For 3V to 5V logic-level translations, simply interchange the +3V supply voltage connection on the comparator's V_{CC} and the +5V supply voltage to the external pullup resistor

PACKAGE OUTLINE DRAWING

5-Pin SC70 Package Outline Drawing

(N.B., Drawings are not to scale)



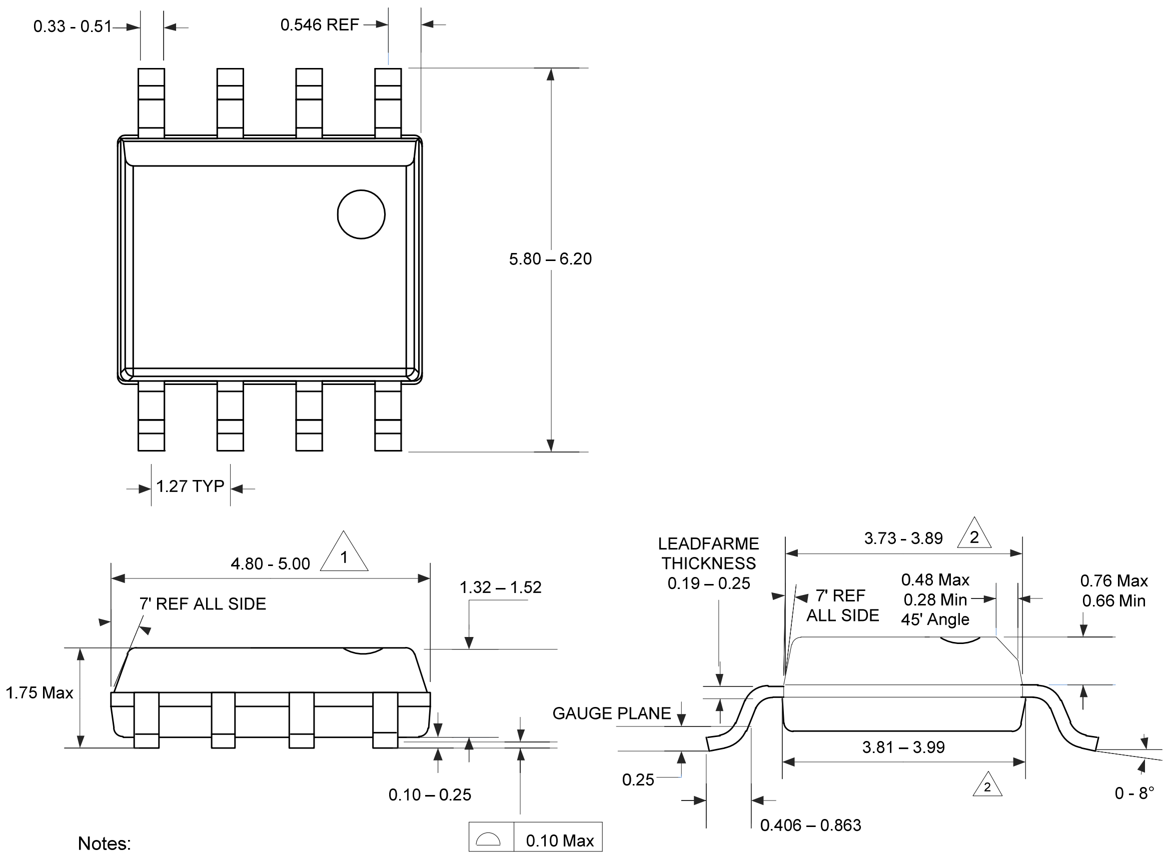
NOTES:

1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
2. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS.
3. DIE IS FACING UP FOR MOLDING. DIE IS FACING DOWN FOR TRIM/FORM.
4. ALL SPECIFICATION COMPLY TO JEDEC SPEC MO-203 AA
5. CONTROLLING DIMENSIONS IN MILIMITERS.
6. ALL SPECIFICATIONS REFER TO JEDEC MO-203 AA
7. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC

PACKAGE OUTLINE DRAWING

8-Pin SOIC Package Outline Drawing

(N.B., Drawings are not to scale)



Notes:

1. Does not include mold flash, protrusions or gate burns. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.
2. Does not include inter-lead flash or protrusions. Inter-lead flash or protrusions shall not exceed 0.25 mm per side.
3. Lead span/stand off height/coplanarity are considered as special characteristic (s).
4. Controlling dimensions are in mm.
5. This part is compliant with JEDEC specification MS-012
6. Lead span/stand off height/coplanarity are considered as Special characteristic.