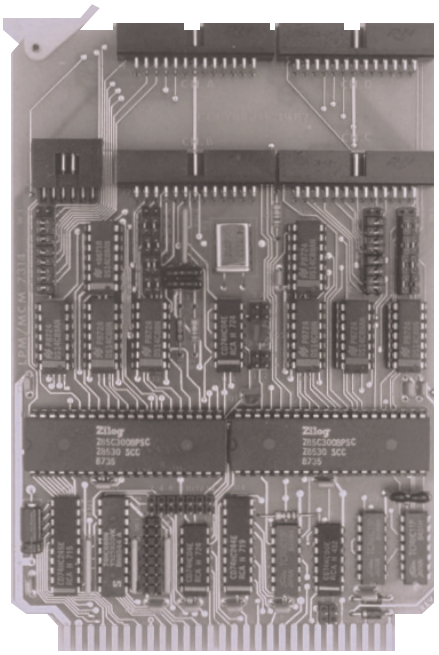
WinSystems®

STD BUS, CMOS STD BUS

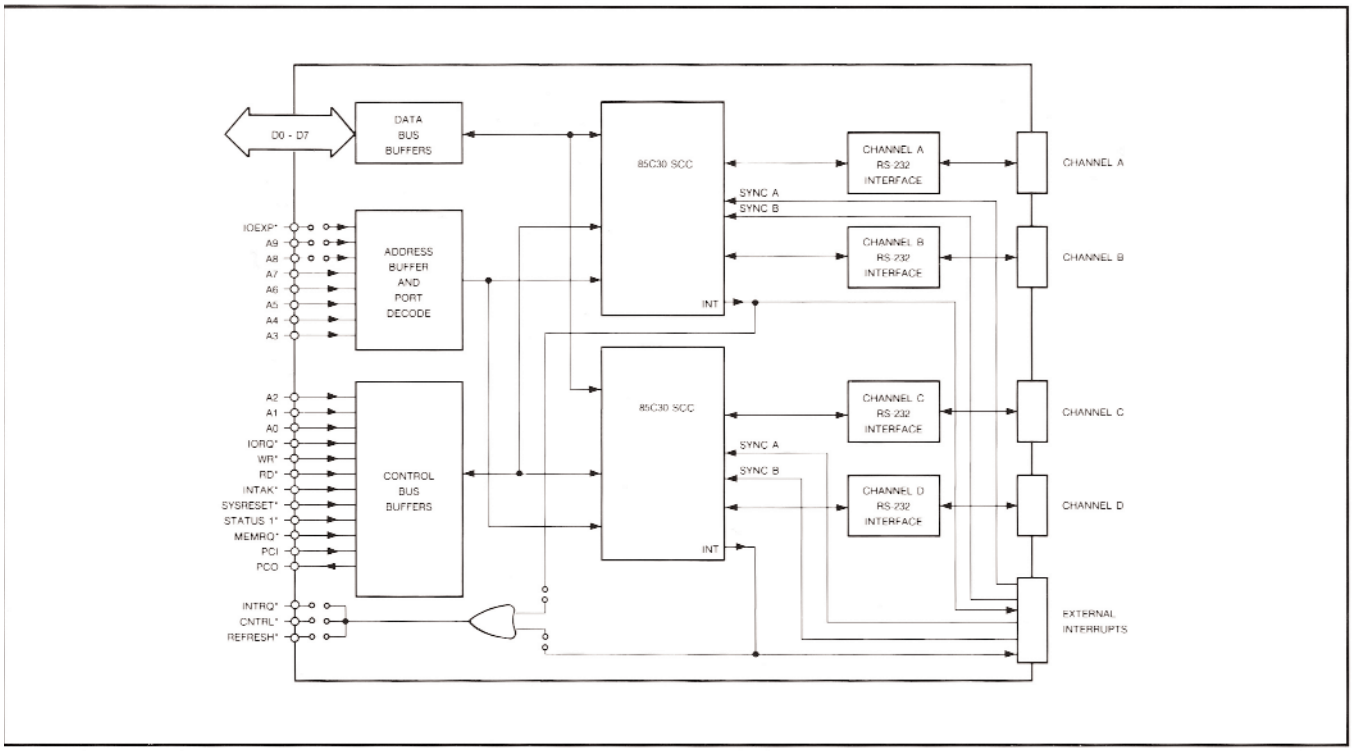
LPM/MCM-7312
LPM-MCM-7314
Quad Multiprotocol I/O

FEATURES

- Four independent, RS-232-C, full-duplex, serial communications channels
- Supports asynchronous and synchronous (BISYNC, SDLC, HDLC, and CCITT-X.25) protocols
- Uses the Z85C30 (CMOS SCC) controller
- Asynchronous data rates 50 to 19.2K bps
- Synchronous data rates to 307.2 Kbps
- Configurable as DTE or DCE Interface with Modem Controls
- Independent programmable baud rate clocks
- 8 or 10-bit I/O mapping
- Programmable Loopback and Auto Echo on each channel
- Interrupts supported
- Available for CMOS STD Bus: LPM-7314
- Requires very low power



The LPM/MCM-7314 is a STD Bus and CMOS STD Bus compatible, four channel, RS-232-C input/output board, designed to be a multiprotocol asynchronous or synchronous serial communications board based upon the Z85C30 CMOS SCC. Each serial channel is independent from the other and capable of data rates of up to 19.2K baud asynchronous or 307.2K baud synchronous. The unit requires very low power and operates over an extended temperature range.



FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-7314 is the CMOS STD Bus version and the MCM-7314 is the STD Bus version of this card. The LPM/MCM prefix indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Addressing - The LPM/MCM-7314 is configured for 8-bit or 10-bit I/O addressing. It is jumper selectable on any even 8 port boundary. IOEXP is decoded as active high, active low, or don't care and can be used to double the addressing range.

Serial Controller - Two Zilog CMOS 85C30 SCC controllers are onboard that provides four independent serial communications channels. The SCC can be software configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, CRC generation/checking, Digital Phase Locked Loops, and crystal oscillator circuits that reduce the need for external logic.

With access to 14 Write registers and 7 Read Registers per channel, the user can configure the SCC chip so that it can handle all standard asynchronous formats regardless of data size, number of stop bits, or parity requirements. It also supports multiple synchronous protocols including character, byte, and bit-oriented protocols such as BiSync, SDLC, HDLC, etc.

Within each operation mode, the Z85C30 SCC allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation and checking, break and abort generation and detection, and many protocol dependent features.

Asynchronous Communications - In the asynchronous mode, the card will work with 5 to 8-bit characters. Transmission and reception can be handled independently on each channel. Reception is protected by a transient spike-rejection mechanism that checks the signal one-half of a bit time after a low level is detected on the receive data input. If the low level does not persist, the character assembly does not start.

The SCC will handle 1, 1½, or 2 stop bits, optional even or odd parity, false start bit detection, and automatic break detection and handling. A built in checking process avoids the interpretation of a framing error as a new start bit. Each channel is setup to provide internal diagnostics such as loopback and echo mode on the data stream.

Synchronous Communications - In synchronous mode, the SCC will support both bit and byte oriented sychronous communications including BiSysnc, SDLC, and HDLC. Synchronous byte oriented protocols can be handled in several modes, allowing character synchronization with a 6-bit or 8-bit synchronous (Monosync), any 12-bit synchronization pattern (Bisync) or with an external sync signal. Leading sync characters can be removed without interrupting the CPU. The External Synchronization mode is supported with an input pin from the channel's respective I/O connector or external interrupt input connector. Five or seven bit synchronous characters can also be detected.

The SCC supports Synchronous bit oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero insertion, and CRC generation. The transmitter can be programmed to send an idle line consisting of continuous flag characters or a steady marking condition. The SCC supports SDLC loop mode in addition to normal SDLC.

NRZ, NRZI, or FM coding may be used. The parity options available in Asynchronous modes are available in Synchronous modes.

Both CRC-16 and CCITT error checking polynomials are supported. Either polynomial may be selected in all Synchronous modes.

Auto Echo and Local Loopback - The SCC is capable of automatically echoing everything it receives. This feature is mainly used in asynchronous modes, but works in synchronous and SDLC modes as well. Auto Echo mode can be used with NRZI and FM encoding with no additional encoding delay.

Baud Rate Generation - The LPM/MCM-7314 has a master 4.9152 MHz crystal oscillator. Each channel contains an independent baud rate generator that can be programmed to generate standard baud rates. It consists of a 16 bit down counter that produces a square wave output. It can be used as a transmit clock, receive clock, or both. It can also drive the Digital Phase-Lock Loop.

Digital Phase-Lock Loop - The SCC contains a Digital Phase-Lock Loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL uses the baud rate clock along with the data stream, to construct a clock for the data.

Serial Configuration - Each channel has 4 modem handshake lines and 3 clock lines in addition to the transmit and receive lines. These lines are RTS, CTS, DTR, DSR, TCLK, and RCLK (DA and DD). Both the serial data and modem control lines are jumper selectable for easy reconfiguration for either DTE or DCE operation. All signals are RS-232 levels except for the External Sync signal (pin 26). The signals from each channel are brought out to separate 26-pin male right angle headers on the card edge which allows easy connections to a flat cable 25-pin "D" type adapter cable. WinSystems offers both male and female type "D" to 26-pin ribbon cables designated CBL-101-3 and CBL-102-3.

The signal assignment on the 26-pin headers is as follows:

Serial I/O Channels A - D

Pin	Signal
1	Ground
2	Transmit Data (TxD)
3	Receive Data (RxD)
4	Request to Send (RTS)
5	Clear to Send (CTS)
6	Data Set Ready (DSR)
7	Signal Ground
15	Receive Clock (DB)
17	Receive Clock (DD)
20	Data Terminal Ready (DTR)
24	Transmit Clock (DA)
26	External Sync

Interrupts - The LPM/MCM-7314 will generate interrupts for 80X88 type processors. The interrupts are driven out on the INTRQ* line on the bus. Acknowledgement is a function of the processor's interrupt acknowledgement scheme.

For 80C85, 80C88, V20, V40, and V50 processors, the LPM/MCM-7314 provides inputs to an off board 82C59A PIC or a processor restart input either via the backplane or over the STD Bus and CMOS STD Bus card's front plane. The LPM/MCM-7314 supports the STDMG's STD-8088 Specification Rev 2.3 for interrupts, but will not support a non-standard 80C88 serial daisy chain configuration.

Interrupt requests can be generated by either chip or by ORing each together as a single interrupt per board. The interrupt requests are wired to pins 9 and 11 of the Interrupt Connector on the top of the board. Alternately, the interrupt requests can be jumper selected to drive INTRQ*, CNTRL*, or REFRESH* on the backplane. This option is provided to allow multiple interrupt souces in a STD BUS and CMOS STD Bus system to input an off board 82C59 PIC without having to connect external wires between boards in a card cage.

Upon detecting an interrupt request by the LPM/MCM-7314, both the vector and status registers in the SCC can be determined by reading Read Register 2 (RR2) and Read Register 3 (RR3) in the respective chip. The interrupt request is simply cleared through software by outputting the correct command word sequence.

External Interrupts - Four external inputs are wired from the external interrupt input connector to the SCC's Sync input pin. These inputs are TTL compatible and serve as either a Sync input or output depending upon the programming. The Sync input can also be programmed to generate an interrupt to the CPU rather than signaling an external sync has been established.

External Interrupt Connector

Pin	Signal
1	Interrupt Request A (input)
3	Interrupt Request B (input)
5	Interrupt Request C (input)
7	Interrupt Request D (input)
9	INTRQ SCC #1 (output)
11	INTRQ SCC #2 (output)
2,4,6,8,10,12	Ground

LPM/MCM-7312 - A dual channel version of the LPM/MCM-7314 is available as the LPM/MCM-7312. It is the same board only depopulated to offer a more cost effective solution when only 2 serial channels are required.

SPECIFICATIONS

Electrical

System Clock: Up to 8.0 MHz

Serial Interface: Synchronous/Asynchronous operation with modem control and receive clock inputs. Jumper configurable as either DCE or DTE; RS-232 signal levels

Baud Rates: 50 to 78.6 Kbaud (Async)

LPM-7314:
Power: = +5V ± 10% at 60mA typ.
+12V ± 10% at 5mA typ.
-12V ± 10% at 5mA typ.
MCM-7314:
Power: = +5V ± 10% at 250mA typ.
+12V ± 10% at 55mA typ.
-12V ± 10% at 55mA typ.

Mechanical

Meets STD Bus mechanical specifications

PC Board: FR4 epoxy glass. Solder mask on both sides, screened component legend and plated through holes.

Connectors

Serial I/O: Four, 26-pin dual on 0.100″ grid
Interrupt: 12-pin dual on 0.100″ grid
Jumpers: 0.025″ square posts

Environmental

Operating Temperature:
LPM-7314 -40°C to +85°C
MCM-7314 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-7314	Quad Serial RS-232 Multiprotocol Card
LPM-7312	Dual Serial RS-232 Multiprotocol Card
MCM-7314	Quad Serial RS-232 Multiprotocol Card
MCM-7312	Dual Serial RS-232 Multiprotocol Card

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