

2Mb Ultra-Low Power Asynchronous Medical CMOS SRAM

256Kx8 bit

Overview

The N02M0818L1A is an integrated memory device **intended for non life-support (Class 1 or 2) medical applications**. This device comprises a 2 Mbit Static Random Access Memory organized as 262,144 words by 8 bits. The device is designed and fabricated using NanoAmp's advanced CMOS technology with reliability enhancements for medical users. The base design is the same as NanoAmp's N02M0818L2A, which has further reliability processing for life-support (Class 3) medical applications. The device operates with two chip enable ($\overline{CE1}$ and $\overline{CE2}$) controls and output enable (\overline{OE}) to allow for easy memory expansion. The N02M0818L1A is optimal for various applications where low-power is critical such as battery backup and hand-held devices. The device can operate over a very wide temperature range of -40°C to $+85^{\circ}\text{C}$ and is available in JEDEC standard packages compatible with other standard 256Kb x 8 SRAMs

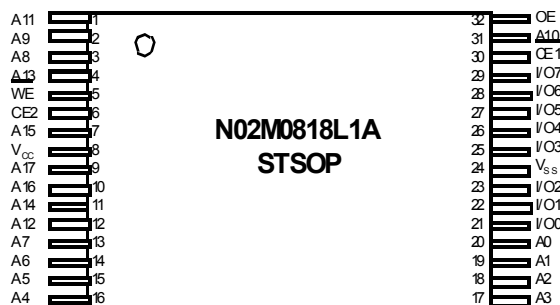
Features

- **Single Wide Power Supply Range**
1.4 to 2.3 Volts - STSOP package
- **Dual Power Supply - Die Only**
1.4 to 2.3 Volts - VCC
1.4 to 3.6 Volts - VCCQ
- **Very low standby current**
200nA maximum at 2.0V and 37 deg C
- **Very low operating current**
1 mA at 2.0V and 1 μs (Typical)
- **Very low Page Mode operating current**
0.5mA at 1.0V and 1 μs (Typical)
- **Simple memory control**
Dual Chip Enables ($\overline{CE1}$ and $\overline{CE2}$)
Output Enable (\overline{OE}) for memory expansion
- **Low voltage data retention**
Vcc = 1.2V
- **Automatic power down to standby mode**
- **Special Processing to reduce Soft Error Rate (SER)**

Product Family

Part Number	Package Type	Operating Temperature	Power Supply (Vcc)	Speed	Standby Current (I _{SB}), Max	Operating Current (I _{CC}), Max
N02M0818L1AN	32 - STSOP I	-40°C to $+85^{\circ}\text{C}$	1.4V - 2.3V	85ns @ 1.7V	20 μA	2.5 mA @ 1MHz
N02M0818L1AD	Known Good Die			150ns @ 1.4V		

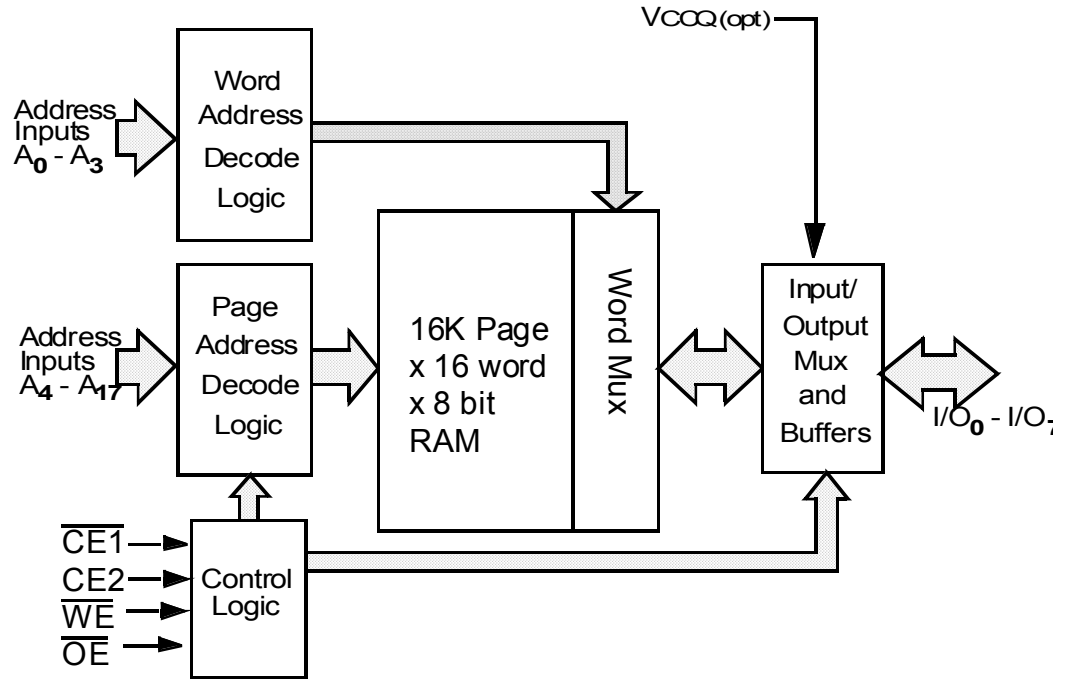
Pin Configuration



Pin Descriptions

Pin Name	Pin Function
A ₀ -A ₁₇	Address Inputs
\overline{WE}	Write Enable Input
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Input
\overline{OE}	Output Enable Input
I/O ₀ -I/O ₇	Data Inputs/Outputs
V _{CCQ}	Output Power (die only)
V _{CC}	Power
V _{SS}	Ground

Functional Block Diagram



Functional Description

$\overline{CE1}$	CE2	\overline{WE}	\overline{OE}	I/O ₀ - I/O ₇	MODE	POWER
H	X	X	X	High Z	Standby ¹	Standby
X	L	X	X	High Z	Standby ¹	Standby
L	H	L	X ²	Data In	Write ²	Active
L	H	H	L	Data Out	Read	Active
L	H	H	H	High Z	Active	Active

1. When the device is in standby mode, control inputs (\overline{WE} and \overline{OE}), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
2. When \overline{WE} is invoked, the \overline{OE} input is internally disabled and has no effect on the circuit.

Capacitance¹

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C _{IN}	V _{IN} = 0V, f = 1 MHz, T _A = 25°C		8	pF
I/O Capacitance	C _{I/O}	V _{IN} = 0V, f = 1 MHz, T _A = 25°C		8	pF

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings¹

Item	Symbol	Rating	Unit
Voltage on any pin relative to V _{SS}	V _{IN,OUT}	-0.3 to V _{CC} +0.3	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-0.3 to 4.5	V
Power Dissipation	P _D	500	mW
Storage Temperature	T _{STG}	-40 to 125	°C
Operating Temperature	T _A	-40 to +85	°C
Soldering Temperature and Time	T _{SOLDER}	240°C, 10sec(Lead only)	°C

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

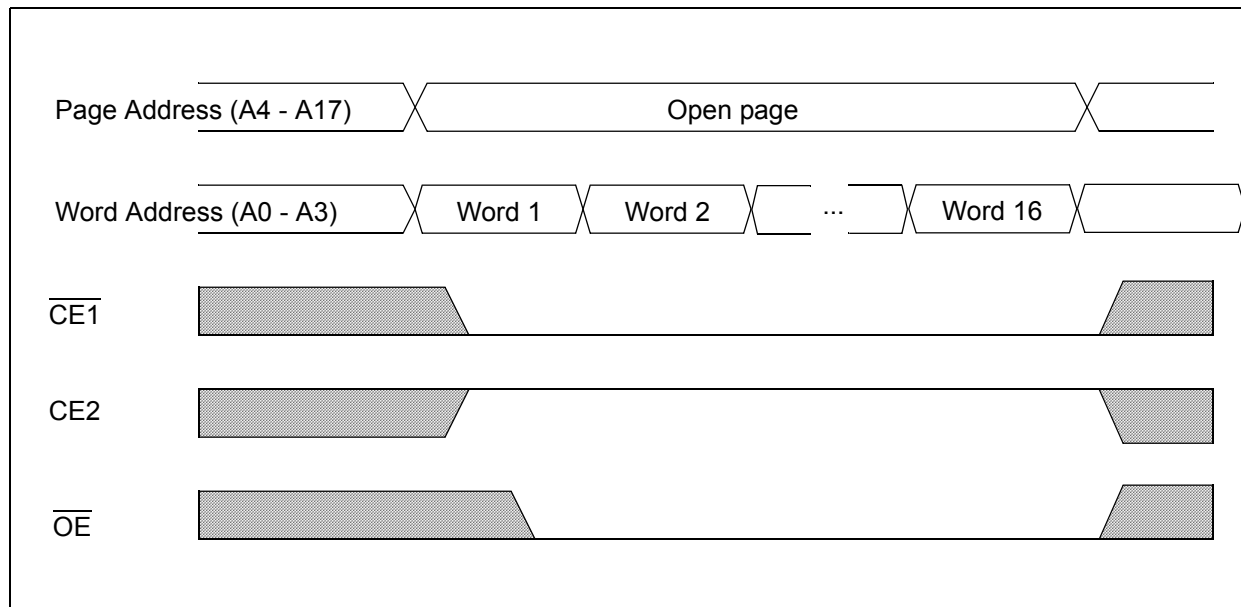
Item	Symbol	Test Conditions	Min.	Typ ¹	Max	Unit
Core Supply Voltage	V _{CC}		1.4	1.8	2.3	V
I/O Supply Voltage	V _{CCQ}	V _{CCQ} > or = V _{CC}	1.4	1.8	3.6	V
Data Retention Voltage	V _{DR}	Chip Disabled ³	1.2			V
Input High Voltage	V _{IH}		V _{CCQ} -0.6		V _{CCQ} +0.3	V
Input Low Voltage	V _{IL}		-0.3		0.6	V
Output High Voltage	V _{OH}	I _{OH} = 0.2mA	V _{CCQ} -0.2			V
Output Low Voltage	V _{OL}	I _{OL} = -0.2mA			0.2	V
Input Leakage Current	I _{LI}	V _{IN} = 0 to V _{CC}			0.1	μA
Output Leakage Current	I _{LO}	\overline{OE} = V _{IH} or Chip Disabled			0.1	μA
Read/Write Operating Supply Current @ 1 μs Cycle Time ²	I _{CC1}	V _{CC} =2.3 V, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0		1.5	2.5	mA
Read/Write Operating Supply Current @ 85 ns Cycle Time ²	I _{CC2}	V _{CC} =2.3 V, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0		10.0	13.0	mA
Page Mode Operating Supply Current @ 85 ns Cycle Time ² (Refer to Power Savings with Page Mode Operation diagram)	I _{CC3}	V _{CC} =2.3 V, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0		3.5		mA
Read/Write Quiescent Operating Supply Current ³	I _{CC4}	V _{CC} =2.3 V, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0, f = 0		0.2		μA
Standby Current ³	I _{SB1}	V _{IN} = V _{CC} or 0V Chip Disabled t _A = 85°C, V _{CC} = 2.3 V		0.2	20.0	μA
Data Retention Current ³	I _{DR}	V _{CC} = 1.8V, V _{IN} = V _{CC} or 0 Chip Disabled, t _A = 85°C		0.1	1.0	μA

1. Typical values are measured at V_{CC}=V_{CC} Typ., T_A=25°C and not 100% tested.

2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

3. This device assumes a standby mode if the chip is disabled ($\overline{CE1}$ high or CE2 low). In order to achieve low standby current all inputs must be within 0.2 volts of either V_{CC} or V_{SS}.

Power Savings with Page Mode Operation ($\overline{WE} = V_{IH}$)



Note: Page mode operation is a method of addressing the SRAM to save operating current. The internal organization of the SRAM is optimized to allow this unique operating mode to be used as a valuable power saving feature.

The only thing that needs to be done is to address the SRAM in a manner that the internal page is left open and 8-bit words of data are read from the open page. By treating addresses A0-A3 as the least significant bits and addressing the 16 words within the open page, power is reduced to the page mode value which is considerably lower than standard operating currents for low power SRAMs.

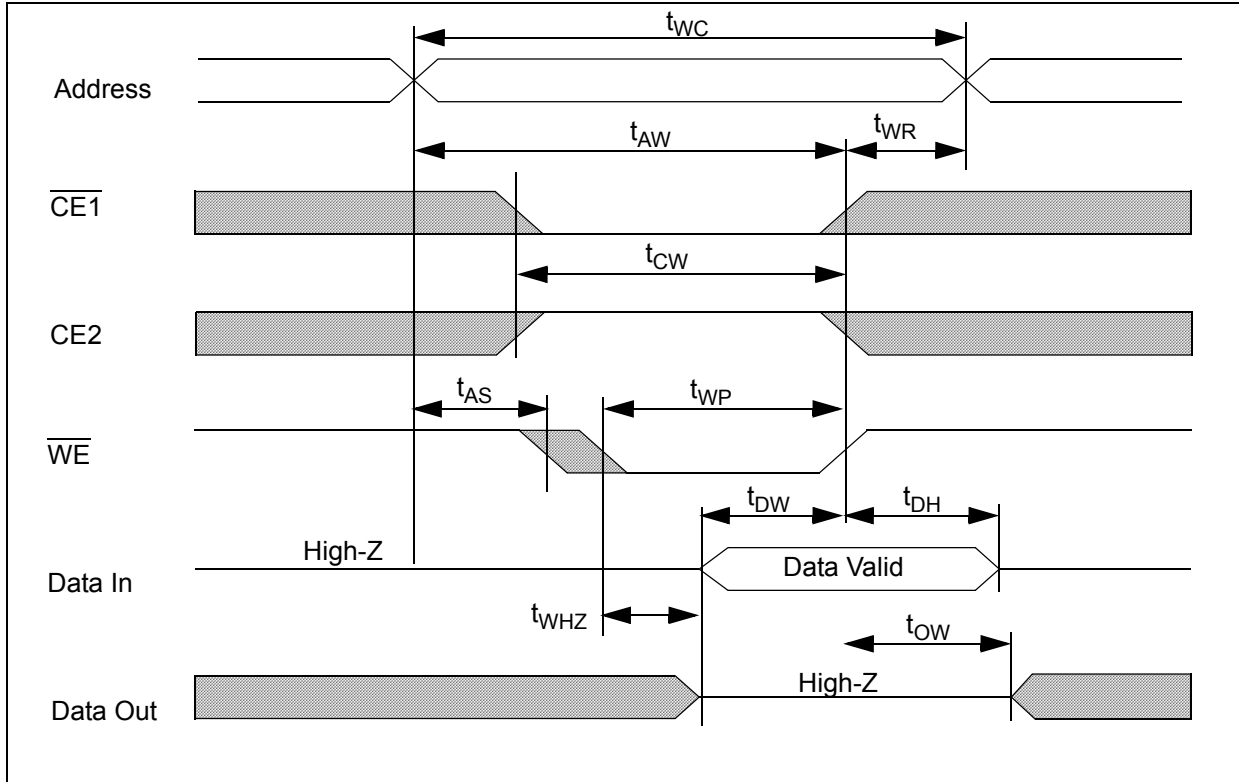
Timing Test Conditions

Item	
Input Pulse Level	0.1V _{CC} to 0.9 V _{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5 V _{CC}
Output Load	CL = 30pF
Operating Temperature	-40 to +85 °C

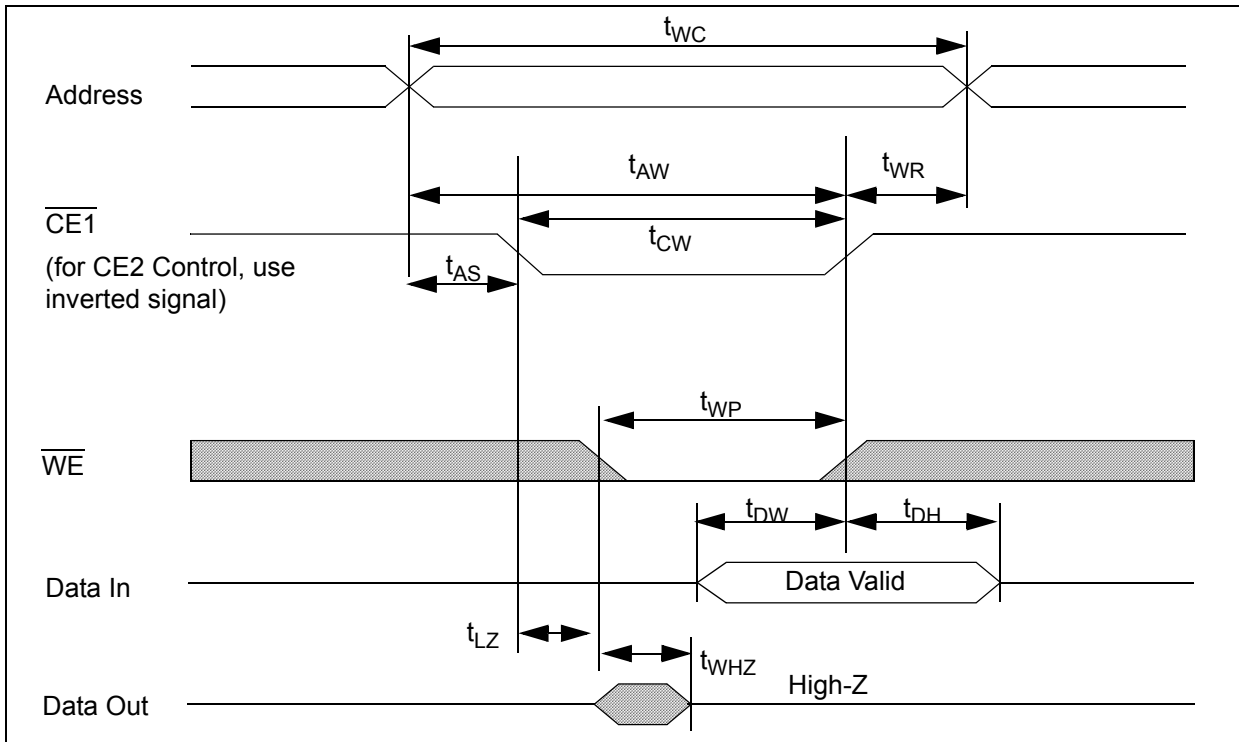
Timing V_{CCQ} > or = V_{CC}

Item	Symbol	V _{CC} = 1.4 - 2.3 V		V _{CC} = 1.7 - 2.3 V		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t _{RC}	150		85		ns
Address Access Time	t _{AA}		150		85	ns
Chip Enable to Valid Output	t _{CO}		150		85	ns
Output Enable to Valid Output	t _{OE}		50		40	ns
Chip Enable to Low-Z output	t _{LZ}	20		10		ns
Output Enable to Low-Z Output	t _{OLZ}	20		5		ns
Chip Disable to High-Z Output	t _{HZ}	0	30	0	15	ns
Output Disable to High-Z Output	t _{OHZ}	0	30	0	15	ns
Output Hold from Address Change	t _{OH}	20		10		ns
Write Cycle Time	t _{WC}	150		85		ns
Chip Enable to End of Write	t _{CW}	75		50		ns
Address Valid to End of Write	t _{AW}	75		50		ns
Write Pulse Width	t _{WP}	50		40		ns
Address Setup Time	t _{AS}	0		0		ns
Write Recovery Time	t _{WR}	0		0		ns
Write to High-Z Output	t _{WHZ}		30		15	ns
Data to Write Time Overlap	t _{DW}	50		40		ns
Data Hold from Write Time	t _{DH}	0		0		ns
End Write to Low-Z Output	t _{OW}	10		5		ns

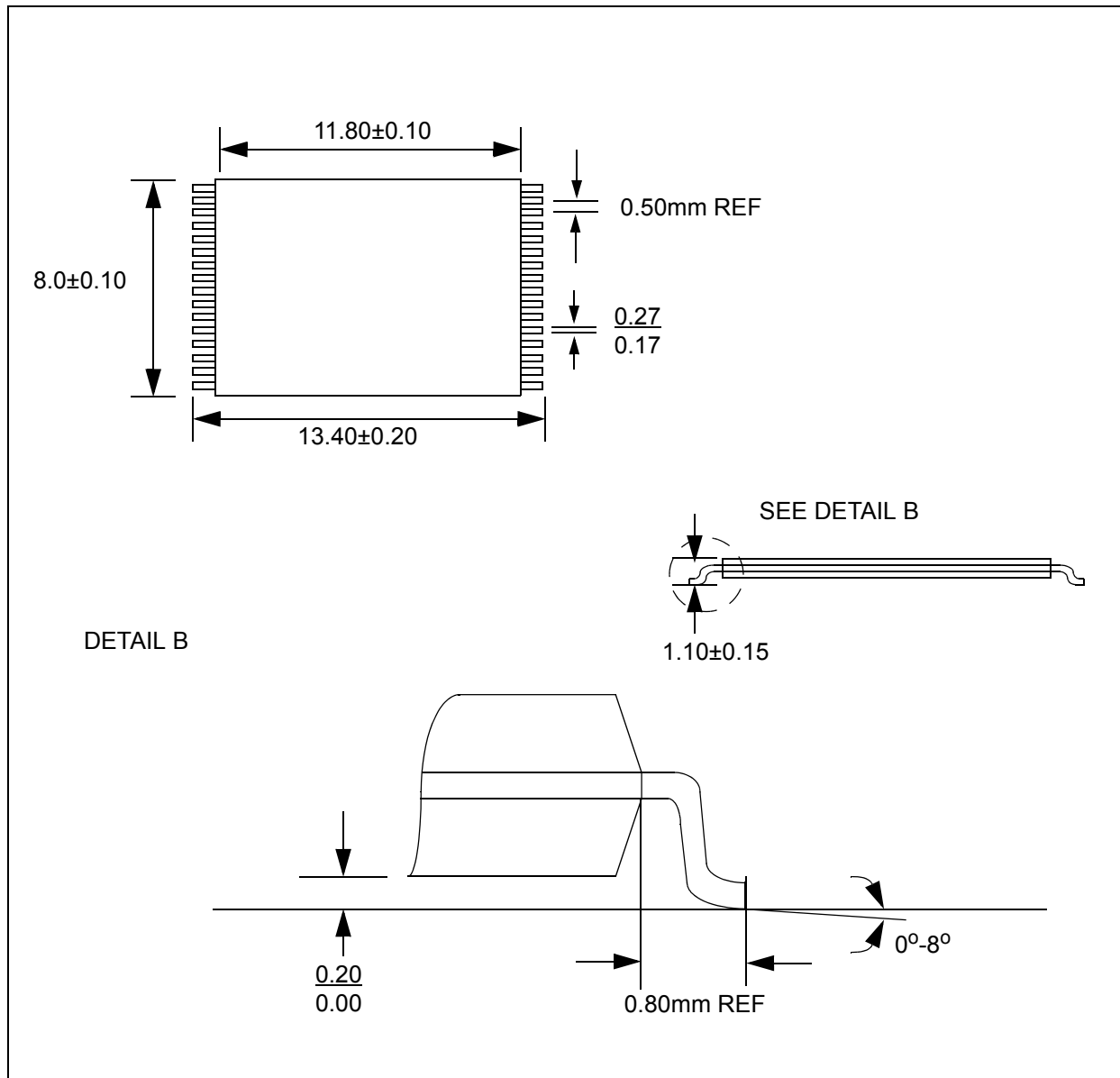
Timing Waveform of Write Cycle (\overline{WE} control)



Timing Waveform of Write Cycle ($\overline{CE1}$ Control)



32-Lead STSOP-I Package (N32)

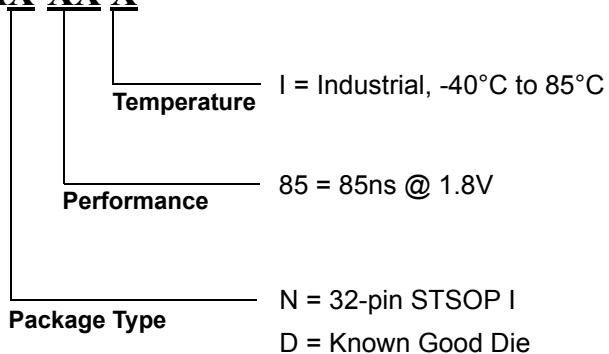


Note:

1. All dimensions in millimeters
2. Package dimensions exclude molding flash

Ordering Information

N02M0818L1AX-XX X



Revision History

Revision #	Date	Change Description
01	11/01/02	Initial Release

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