MIC2588/MIC2594

Single-Channel, Negative High-Voltage Hot Swap Power Controllers

General Description

The MIC2588 and the MIC2594 are single-channel, negative-voltage hot swap controllers designed to address the need for safe insertion and removal of circuit boards into "live" high-voltage system backplanes, while using very few external components. The MIC2588 and the MIC2594 are each available in an 8-pin SOIC package and work in conjunction with an external N-Channel MOSFET for which the gate drive is controlled to provide inrush current limiting and output voltage slew-rate control. Overcurrent fault protection is also provided for which the overcurrent threshold is programmable. During an output overload condition, a constant-current regulation loop is engaged to ensure that the system power supply maintains regulation. If a fault condition exceeds a built-in 400µs nuisance-trip delay, the MIC2588 and the MIC2594 will latch the circuit breaker's output off and will remain in the off state until reset by cycling either the UV/OFF pin or the power to the IC. A master Power-Good signal is provided to indicate that the output voltage of the soft-start circuit is within its valid output range. This signal can be used to enable one or more DC-DC converter modules.

All support documentation can be found on Micrel's web site at www.micrel.com.

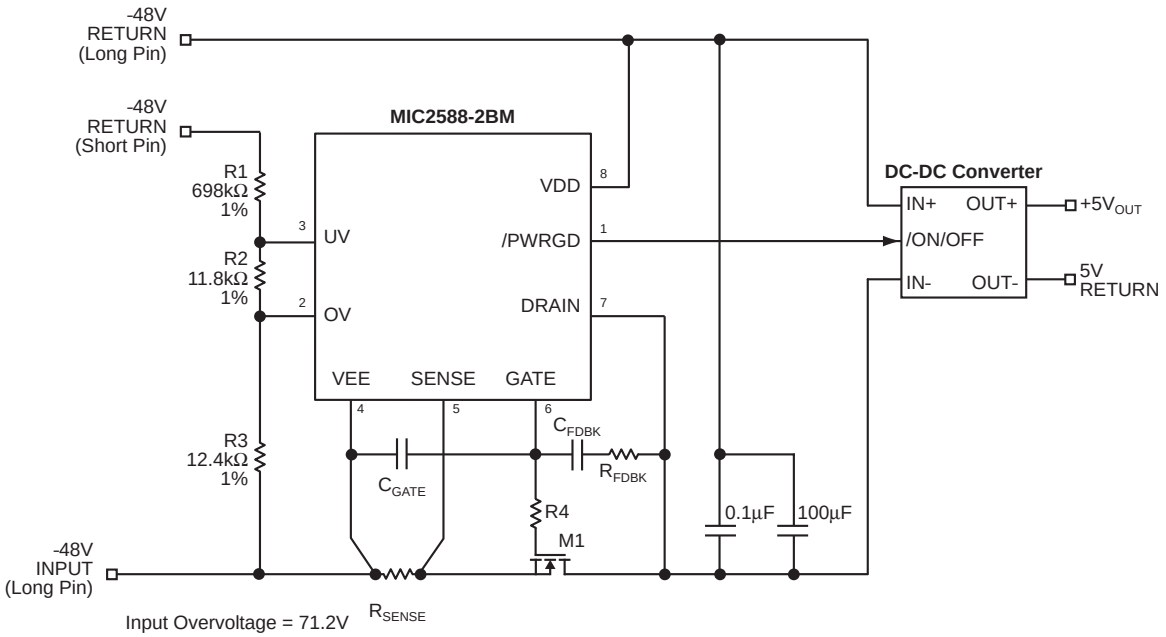
Features

- MIC2588:
  - Pin-for-pin functional equivalent to the LT1640/LT1640A/LT4250
- Provides safe insertion and removal from live –48V (nominal) backplanes
- Operates from –19V to –80V
- Electronic circuit breaker function
- Built-in 400µs "nuisance-trip" delay (t_{FLT})
- Regulated maximum output current into faults
- Programmable inrush current limiting
- Fast response to short circuit conditions (< 1µs)
- Programmable undervoltage and overvoltage lockouts (MIC2588-xBM)
- Programmable UVLO hysteresis (MIC2594-xBM)
- Fault reporting:
  - Active-HIGH (-1BM) and Active-LOW (-2BM) Power-Good signal output

Applications

- Central office switching
- –48V power distribution
- Distributed power systems

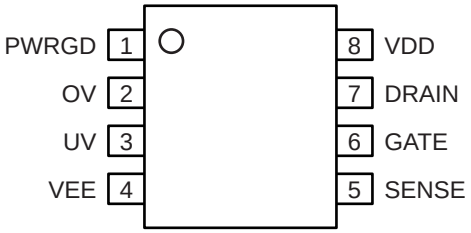
Typical Application



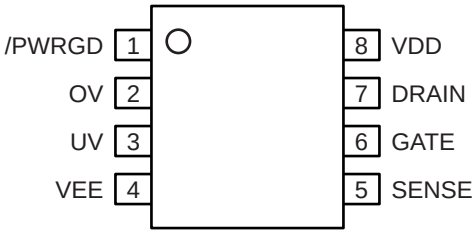
Ordering Information

Part Number	PWRGD Polarity	Lockout Functions	Circuit Breaker Function	Package
MIC2588-1BM	Active-High	Undervoltage and Overvoltage	Latched Off	8-pin SOIC
MIC2588-2BM	Active-Low	Undervoltage and Overvoltage	Latched Off	8-pin SOIC
MIC2594-1BM	Active-High	Programmable UVLO Hysteresis	Latched Off	8-pin SOIC
MIC2594-2BM	Active-Low	Programmable UVLO Hysteresis	Latched Off	8-pin SOIC

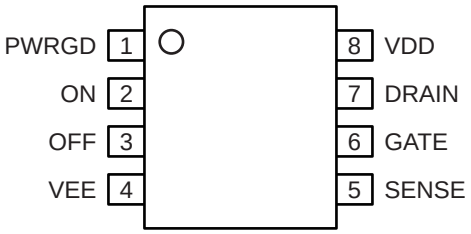
Pin Configuration



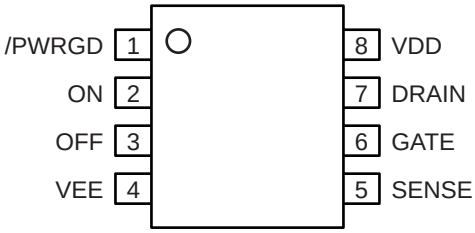
8-Pin SOIC (M)
MIC2588-1BM



8-Pin SOIC (M)
MIC2588-2BM



8-Pin SOIC (M)
MIC2594-1BM



8-Pin SOIC (M)
MIC2594-2BM

Pin Description

Pin Number	Pin Name	Pin Function
1	PWRGD /PWRGD	Power-Good Output: Open-drain. Asserted when the voltage on the DRAIN pin (V_{DRAIN}) is within V_{PGTH} of VEE, indicating that the output voltage is within proper specifications.
1	MIC25XX-1 PWRGD Active-High	MIC2588-1 and MIC2594-1: PWRGD will be high-impedance when V_{DRAIN} is less than V_{PGTH}, and will pull-down to V_{DRAIN} when V_{DRAIN} is greater than V_{PGTH}. Asserted State: Open-Drain.
1	MIC25XX-2 /PWRGD Active-Low	MIC2588-2 and MIC2594-2: /PWRGD will pull-down to V_{DRAIN} when V_{DRAIN} is less than $V_{PGTH,}$ and will be high impedance when V_{DRAIN} is greater than V_{PGTH}. Asserted State: Active-Low.
2	OV Threshold	MIC2588: Overvoltage Threshold Input. When the voltage at the OV pin is greater than the V_{OVH} threshold, the GATE pin is immediately pulled low by an internal 100µA current pull-down.
2	ON Turn-On Threshold	MIC2594: Turn-On Threshold. At initial system power-up or after the device has been shut off by the OFF pin, the voltage on the ON pin must exceed the V_{ONH} threshold in order for the MIC2594 to be enabled.
3	UV Threshold	MIC2588: Undervoltage Threshold Input. When the voltage at the UV pin is less than the V_{UVL} threshold, the GATE pin is immediately pulled low by an internal 100µA current pull-down. The UV pin is also used to cycle the device off and on to reset the circuit breaker. Taken together, the OV and UV pins form a window comparator which defines the limits of V_{EE} within which the load may safely be powered.
3	OFF Turn-Off Threshold	MIC2594: Turn-Off Threshold. When the voltage at the OFF pin is less than the V_{OFFL} threshold, the GATE pin is immediately pulled low by an internal 100µA current pull-down. The OFF pin is also used to cycle the device off and on to reset the circuit breaker. Taken together, the ON and OFF pins provide programmable hysteresis for the turn-on command voltage.
4	VEE	Negative Supply Voltage Input.
5	SENSE	Circuit Breaker Sense Input: The current-limit threshold is set by connecting a resistor between this pin and V_{EE}. When the current-limit threshold of IR = 50mV is exceeded for an internal delay t_{FLT} (400µs), the circuit breaker is tripped and the GATE pin is immediately pulled low. Toggling UV or OV will reset the circuit breaker. To disable the circuit breaker, externally connect SENSE and VEE together.
6	GATE	Gate Drive Output: Connect to the gate of an external N-Channel MOSFET.
7	DRAIN	Drain Sense Input: Connect to the drain of an external N-Channel MOSFET.
8	VDD	Positive Supply Input.

Absolute Maximum Ratings[1]

(All voltages are referred to V_{EE})

Supply Voltage ($V_{DD} - V_{EE}$) ..... –0.3V to 100V
DRAIN, PWRGD pins ..... –0.3V to 100V
GATE pin ..... –0.3V to 12.5V
SENSE, OV, UV, ON, OFF pins ..... –0.3V to 6V
ESD Ratings[3]
  Human Body Model 2kV
Soldering
  Vapor Phase ..... (60 sec.) +220°C +5 ±0°C
  Infrared ..... (15 sec.) +235°C +5 ±0°C

Operating Ratings[2]

Supply Voltage ($V_{DD} - V_{EE}$) ..... +19V to +80V
Ambient Temperature Range (T_A) ..... –40°C to 85°C
Junction Temperature (T_J) ..... 125°C
Package Thermal Resistance
  SOIC (θ_{JA}) ..... 152°C/W

DC Electrical Characteristics[4]

V_{DD} = 48V, V_{EE} = 0V, T_A = 25°C, unless otherwise noted. **Bold** indicates specifications apply over the full operating temperature range of –40°C to +85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD} - V_{EE}$	Supply Voltage		**19**		**80**	
I_{DD}	Supply Current			3	**5**	mA
V_{TRIP}	Circuit Breaker Trip Voltage	$V_{TRIP} = V_{SENSE} - V_{EE}$	**40**	50	**60**	mV
I_{GATEON}	GATE Pin Pull-up Current	$V_{GATE} = V_{EE}$ to 8V $19V \le (V_{DD} - V_{EE}) \le 80V$	**30**	45	**60**	µA
$I_{GATEOFF}$	GATE Pin Sink Current	$(V_{SENSE} - V_{EE}) = 100mV$ $V_{GATE} = 2V$	100	230		mA
V_{GATE}	GATE Drive Voltage, ($V_{GATE} - V_{EE}$)	$15V \le (V_{DD} - V_{EE}) \le 80V$	**9**	10	**11**	V
I_{SENSE}	SENSE Pin Current	V_{SENSE} = 50mV		0.2		µA
V_{UVH}	UV Pin High Threshold Voltage	Low-to-High Transition	**1.213**	1.243	**1.272**	V
V_{UVL}	UV Pin Low Threshold Voltage	High-to-Low Transition	**1.198**	1.223	**1.247**	V
V_{UVHYS}	UV Pin Hysteresis			20		mV
V_{OVH}	OV Pin High Threshold Voltage	Low-to-High Transition	**1.198**	1.223	**1.247**	V
V_{OVL}	OV Pin Low Threshold Voltage	High-to-Low Transition	**1.165**	1.203	**1.232**	V
V_{OVHYS}	OV Pin Hysteresis			20		mV
V_{ONH}	ANSI ON Pin High Threshold Voltage	Low-to-High Transition	**1.198**	1.223	**1.247**	V
V_{OFFH}	ANSI OFF Pin Low Threshold Voltage	High-to-Low Transition	**1.198**	1.223	**1.247**	V
I_{CNTRL}	Input Bias Current (OV, UV, ON, OFF Pins)	V_{UV} = 1.25V			**0.5**	µA
V_{PGTH}	Power-Good Threshold	High-to-Low Transition ($V_{DRAIN} - V_{EE}$)	**1.1**	1.26	**1.40**	V
V_{OLPG}	PWRGD Output Voltage (relative to voltage at the DRAIN pin)	$V_{OLPG} - V_{DRAIN}$ $0mA \le I_{PG(LOW)} \le 1mA$				
	MIC25XX-1	$(V_{DRAIN} - V_{EE}) < V_{PGTH}$	**–0.25**		**0.8**	V
	MIC25XX-2	$(V_{DRAIN} - V_{EE}) > V_{PGTH}$	**–0.25**		**0.8**	V
$I_{LKG(PG)}$	PWRGD Output Leakage Current	$V_{PWRGD} = V_{DD}$ = 80V			**1**	µA

Notes:

1. Exceeding the *"Absolute Maximum Ratings"* may damage the devices.
2. The devices are not guaranteed to function outside the specified operating conditions.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model: 1.5kΩ in series with 100pF. Machine model: 200pF, no series resistance.
4. Specification for packaged product only.

AC Electrical Characteristics[5]

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{FLT}	Built-in Overcurrent Nuisance Trip Time Delay (Figure 1)	**Note 6**		400		µs
$t_{OCSENSE}$	Overcurrent Sense to GATE Low (Figure 2)	$V_{SENSE} - V_{EE} = 100mV$			3.5	µs
t_{OVPHL}	OV to GATE Low (Figure 3)	**Note 6**		1		µs
t_{OVPLH}	OV to GATE High (Figure 3)	**Note 6**		1		µs
t_{UVPHL}	UV to GATE Low (Figure 4)	**Note 6**		1		µs
t_{UVPLH}	UV to GATE High (Figure 4)	**Note 6**		1		µs
$t_{PGL(1)}$	DRAIN High to PWRGD Output Low (-1 Version parts only)	$R_{PULLUP} = 100k\Omega$, C_{LOAD} on PWRGD = 50pF[6]		1		µs
$t_{PGL(2)}$	DRAIN Low to /PWRGD Output Low (-2 Version parts only)	$R_{PULLUP} = 100k\Omega$, C_{LOAD} on /PWRGD = 50pF[6]		1		µs
$t_{PGH(1)}$	DRAIN Low to PWRGD Output High (-1 Version parts only)	$R_{PULLUP} = 100k\Omega$, C_{LOAD} on PWRGD = 50pF[6]		2		µs
$t_{PGH(2)}$	DRAIN High to /PWRGD Output High (-2 Version parts only)	$R_{PULLUP} = 100k\Omega$, C_{LOAD} on /PWRGD = 50pF[6]		2		µs

Notes:

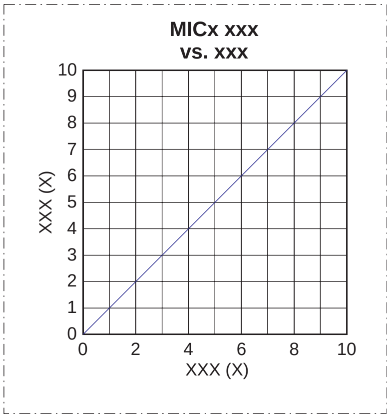
5. Specification for packaged product only.
6. Not 100% production tested. Parameters are guaranteed by design.

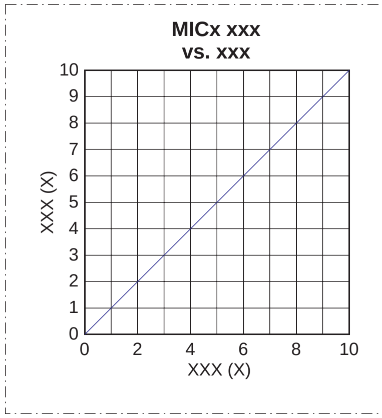
Test Circuit

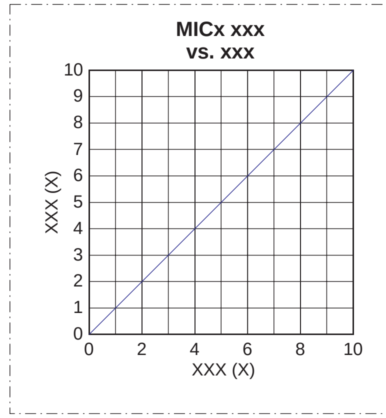
[Section under construction]

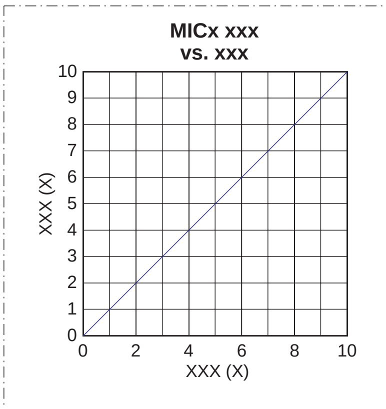
Typical Characteristics

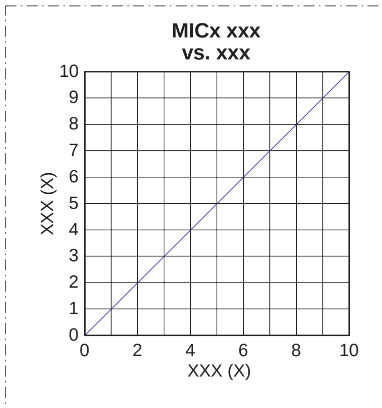
[Section under construction]

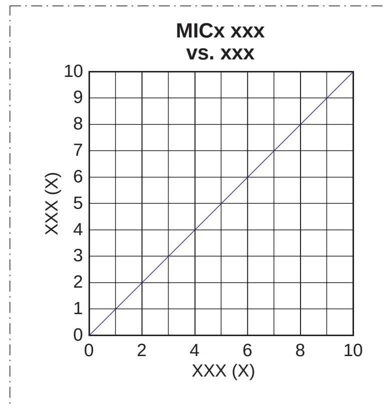


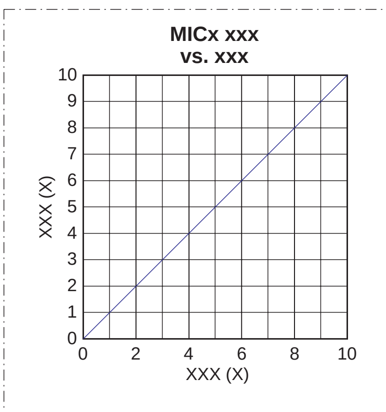


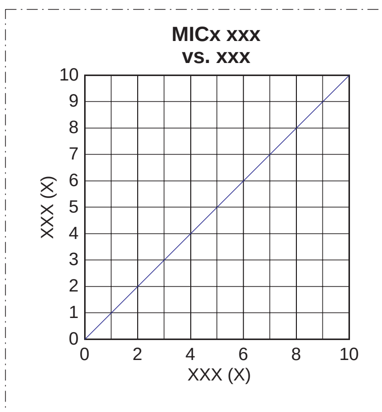


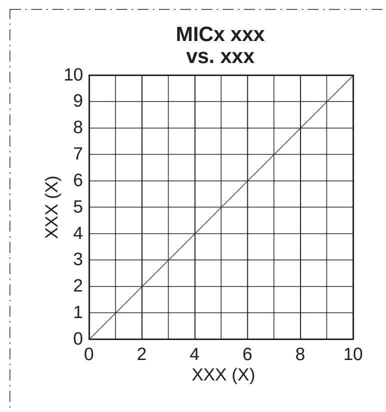


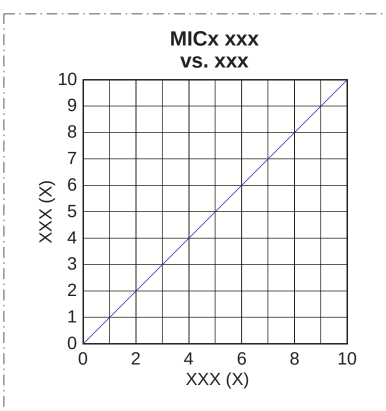


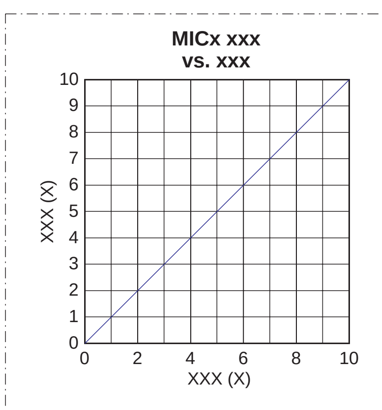


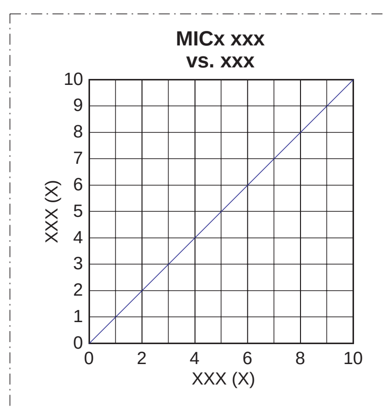












Timing Diagrams

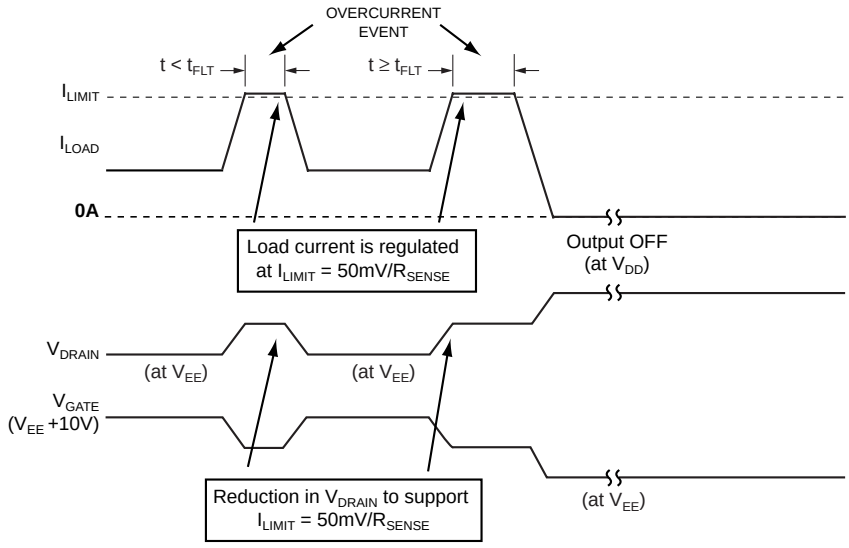


Figure 1. Overcurrent Response

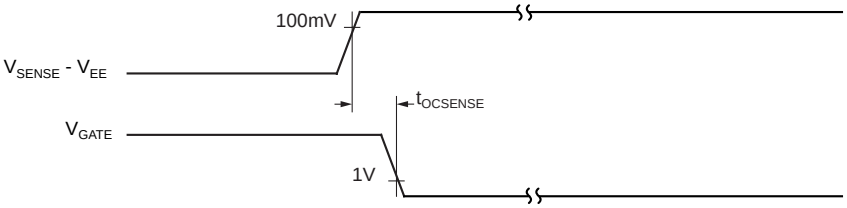


Figure 2. SENSE to GATE LOW Timing Response

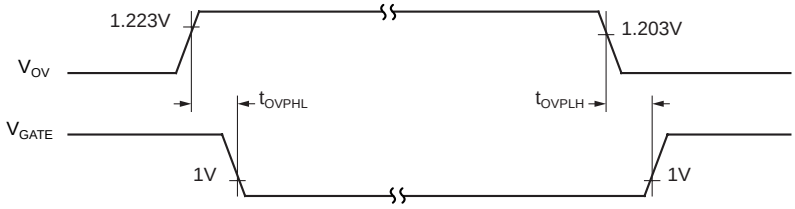


Figure 3. Overvoltage Response

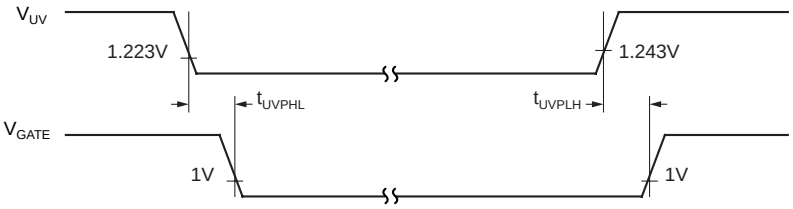
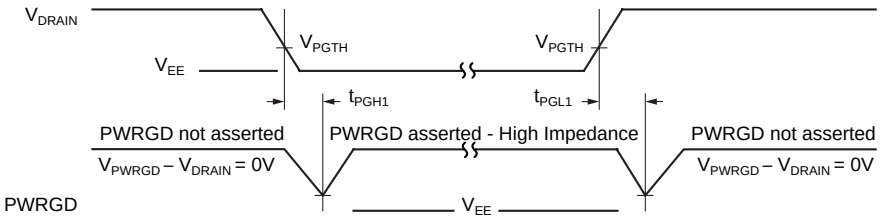


Figure 4. Undervoltage Response

MIC2588/94-1



MIC2588/94-2

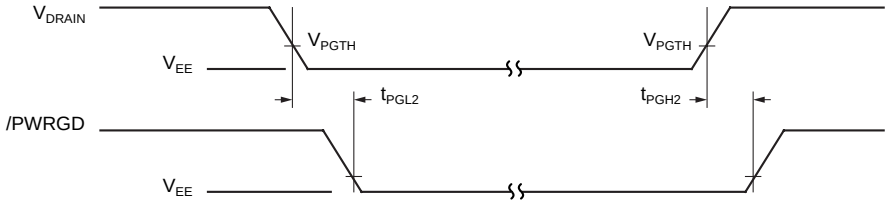
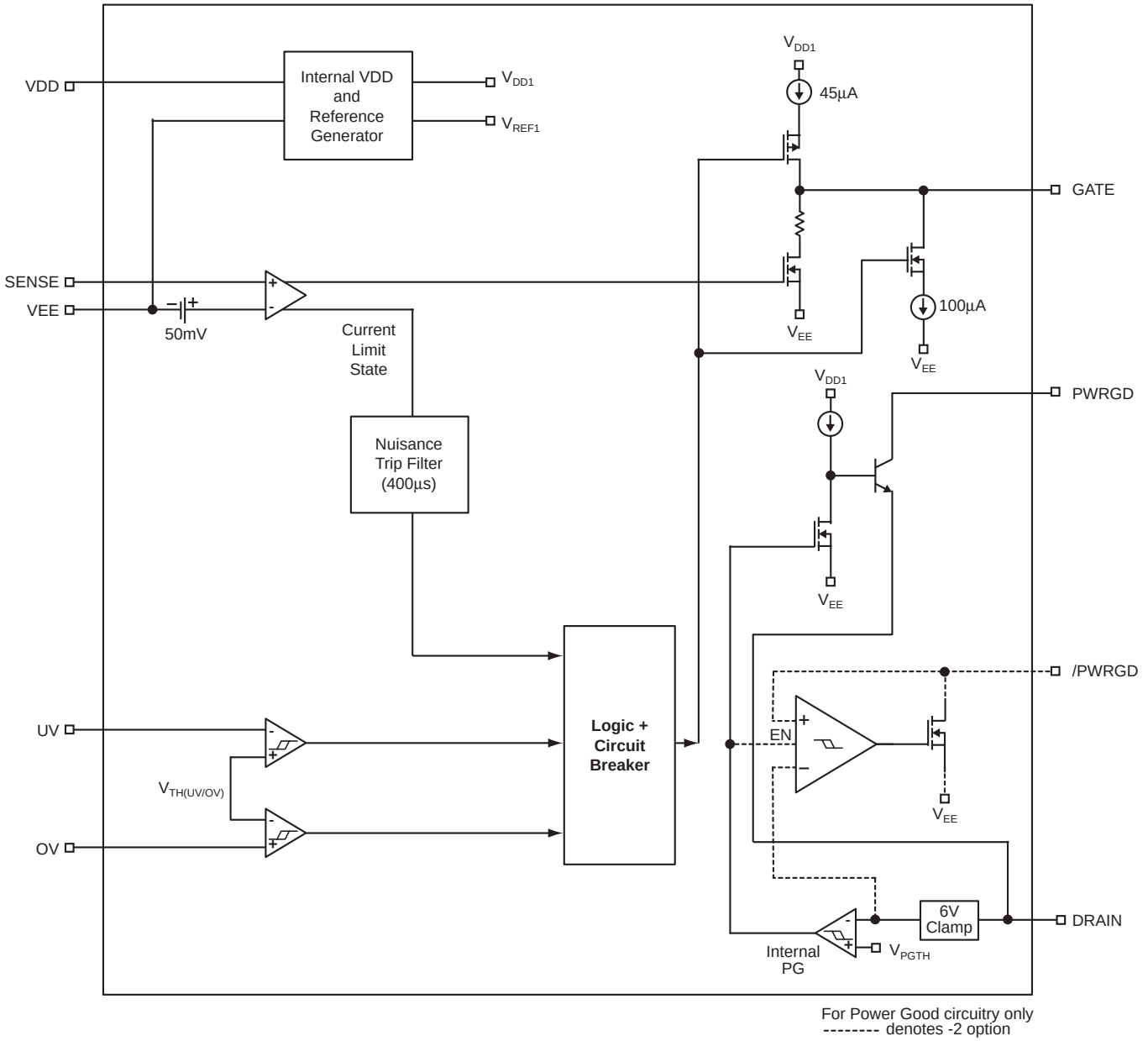


Figure 5. DRAIN to Power-Good Response

Functional Diagram



MIC2588 Block Diagram

Functional Description

Hot Swap Insertion

When circuit boards are inserted into systems carrying live supply voltages ("hot swapped"), high inrush currents often result due to the charging of bulk capacitance that resides across the circuit board's supply pins. These current spikes can cause the system's supply voltages to temporarily go out of regulation, causing data loss or system lock-up. In more extreme cases, the transients occurring during a hot swap event may cause permanent damage to connectors or on-board components.

The MIC2588 and the MIC2594 are designed to address these issues by limiting the magnitude of the transient current during hot swap events. This is achieved by controlling the rate at which power is applied to the circuit board (di/dt and dv/dt management). In addition, to inrush current control, the MIC2588 and the MIC2594 incorporate input voltage supervisory functions and current limiting, thereby providing robust protection for both the system and the circuit board.

Start-Up Cycle

When the input voltage to the IC is between the overvoltage and undervoltage thresholds (MIC2588) or is greater than V_{ON} (MIC2594), a start cycle is initiated. At this time, the GATE pin of the IC applies a constant charging current (I_{GATEON}) to the gate of the external MOSFET (M1). C_{FDBK} creates a Miller integrator out of the MOSFET circuit, which limits the slew-rate of the voltage at the drain of M1. The drain voltage rate-of-change (dv/dt) of M1 is:

$$\frac{dv(M1_{DRAIN})}{dt} = \left(\frac{I_{GATE(-)}}{C_{FDBK}}\right) = -\left(\frac{I_{GATEON}}{C_{FDBK}}\right)$$

where $I_{GATE(+)}$ = Gate Charging Current = I_{GATEON}; $I_{GATE(-)} \cong -I_{GATE(+)}$, due to the extremely high transconductance values of power MOSFETs; and

$$I_{GATE(-)} = C_{FDBK} \times \frac{dv(M1_{DRAIN})}{dt}$$

Relating the above to the maximum transient current into the load capacitance to be charged upon hot swap or power-up involves a simple extension of the same formula:

$$I_{CHARGE} = \frac{C_{LOAD} \times dv(M1_{DRAIN})}{dt}$$

$$I_{CHARGE} = C_{LOAD} \times -\left(\frac{I_{GATEON}}{C_{FDBK}}\right)$$

$$| I_{CHARGE} | = \frac{C_{LOAD} \times I_{GATEON}}{C_{FDBK}}$$

Transposing:

$$C_{FDBK} = \frac{C_{LOAD} \times I_{GATEON}}{| I_{CHARGE} |} \quad (1)$$

C_{GATE} and R_{FDBK} prevent turn-on and hot swap current surges which would otherwise be caused by (C_{FDBK} + $C_{D-G(M1)}$) coupling turn-on transients from the drain to the gate of M1. An appropriate value for C_{GATE} may be determined using the formula for a capacitive voltage divider:

Maximum voltage on C_{GATE} at turn-on must be less than $V_{THRESHOLD}$ of M1:

1. For a standard 10V enhancement N-Channel MOSFET, $V_{THRESHOLD}$ is about 4.25V.
2. Choose 3.5V as a safe maximum voltage to safely avoid turn-on transients.

$$V_{G-S(M1)} \times [C_{GATE} + (C_{FDBK} + C_{D-G(M1)})] = [(V_{DD} - V_{EE}(min)) \times (C_{FDBK} + C_{D-G(M1)})]$$

$$V_{G-S(M1)} \times C_{GATE} = [(V_{DD} - V_{EE}(min)) - V_{G-S(M1)}] \times (C_{FDBK} + C_{D-G(M1)})$$

$$C_{GATE} = \left(C_{FDBK} + C_{D-G(Q1)}\right) \times \frac{\left(V_{DD} - V_{EE}(min)\right) - V_{G-S(M1)}}{V_{G-S(M1)}} \quad (2)$$

While the value for R_{FDBK} is not critical, it should be chosen to allow a maximum of several milliamperes to flow in the gate-drain circuit of M1 during turn-on. While the final value for R_{FDBK} is determined empirically, initial values between R_{FDBK} = 15kΩ to 27kΩ for systems with a maximum value of 75V for (V_{DD} – V_{EE}(min)) are appropriate.

Resistor R4, in series with the MOSFETs gate, minimizes the potential for parasitic high frequency oscillations from occurring in M1. While the exact value of R4 is not critical, commonly used values for R4 range from 10Ω to 33Ω.

For example, let us assume a hot swap controller is required to maintain the inrush current into a 150µF load capacitance at 1.7A maximum, and that this circuit may operate from supply voltages as high as (V_{DD} – V_{EE}) = 75V. The MOSFET to be used with the MIC2588/94 is an IRF540NS 100V D^2PAK device which has a typical (C_{D-G}) of 250pF.

Calculating a value for C_{FBDK} using Equation 1 yields:

$$C_{FDBK} = \frac{150\mu F \times 45\mu A}{1.7A} = 3.97nF$$

Good engineering practice suggests the use of the worst-case parameter values for I_{GATEON} from the *"DC Electrical Characteristics"* section:

$$C_{FDBK} = \frac{150\mu F \times 60\mu A}{1.7A} = 5.3nF$$

where the nearest standard 5% value is 5.6nF. Substituting 5.6nF into Equation 2 from above yields:

$$C_{GATE} = (5.6nF + 250pF) \times \frac{(75V - 3.5V)}{3.5V} = 0.12\mu F$$

Finally, choosing R4 = 10Ω and R_{FDBK} = 20kΩ will yield a suitable, initial design for prototyping.

Power-Good (PWRGD or /PWRGD) Output

For the MIC2588-1 and the MIC2594-1, the Power-Good output signal (PWRGD) will be high impedance when V_{DRAIN} drops below V_{PGTH}, and will pull down to V_{DRAIN} when V_{DRAIN} is above V_{PGTH}. For the MIC2588-2 and the MIC2594-2, /PWRGD will pull down to the potential of the V_{DRAIN} pin when V_{DRAIN} drops below V_{PGTH}, and will be high impedance when V_{DRAIN} is above V_{PGTH}. Hence, the -1 parts have an active-high PWRGD signal and the -2 parts have an active-low /PWRGD output. Either PWRGD or /PWRGD may be used as an enable signal for one or more subsequent DC/DC converter modules or for other system uses as desired. When used as an enable signal, the time necessary for the PWRGD (or /PWRGD) signal to pull-up (when in high impedance state) will depend upon the load (RC) that is present on this output.

Circuit Breaker Function

The MIC2588 and the MIC2594 employ an electronic circuit breaker that protects the MOSFET and other system components against faults such as short circuits. The current limit threshold is set via an external resistor, R_{SENSE}, connected between the V_{EE} and SENSE pins. An internal 400µs timer limits the length of time (t_{FLT}) for which the circuit can draw current in excess of its programmed threshold before the circuit breaker is tripped. This short delay prevents nuisance tripping of the circuit breaker due to system transients while providing rapid protection against large-scale transient faults. Whenever the voltage across R_{SENSE} exceeds 50mV, two things happen:

1. A constant-current regulation loop is engaged designed to hold the voltage across R_{SENSE} equal to 50mV. This protects both the load and the MIC2588 circuit from excessively high currents. This loop will engage in less than 1µs from the time at which the overvoltage condition on R_{SENSE} occurs.
2. The internal 400µs timer is started. If the 400µs timeout period is exceeded, the circuit breaker trips and the GATE pin is immediately pulled low by an internal current pull-down. This operation turns off the MOSFET quickly and disconnects the input from the load.

Current Sensing

As mentioned before, the MIC2588 and the MIC2594 employ an external low-value resistor in series with the source of the external MOSFET to measure the current flowing into the load. The V_{EE} connection to the IC from the negative supply is also one input to the part's internal current sensing circuits and the SENSE input is the other input.

Sense Resistor Selection

The sense resistor is nominally valued at:

$$R_{SENSE}(nom) = \frac{V_{TRIP}(typ)}{I_{HOT\_SWAP}(nom)}$$

where V_{TRIP}(typ) is the nominal circuit breaker threshold voltage (= 50mV) and I_{HOT_SWAP}(nom) is the nominal hot swap load current level to trip the internal circuit breaker in the application.

To accommodate worst-case tolerances in the sense resistor (for a ±1% initial tolerance, allow ±3% tolerance for variations over time and temperature) and circuit breaker threshold voltages, a slightly more detailed calculation must be used to determine the minimum and maximum hot swap load currents.

As the MIC2588/94's minimum current limit threshold voltage is 40mV, the minimum hot swap load current is determined where the sense resistor is 3% high:

$$I_{HOT\_SWAP}(min) = \frac{40mV}{\left(1.03 \times R_{SENSE}(nom)\right)} = \frac{38.8mV}{R_{SENSE}(nom)}$$

Keep in mind that the minimum hot swap load current should be greater than the application circuit's upper steady-state load current boundary. Once the lower value of R_{SENSE} has been calculated, it is good practice to check the maximum hot swap load current (I_{HOT_SWAP}(max)) which the circuit may let pass in the case of tolerance build-up in the opposite direction. Here, the worst-case maximum is found using a V_{TRIP}(max) of 60mV and a sense resistor, 3% low in value:

$$I_{HOT\_SWAP}(max) = \frac{60mV}{\left(0.97 \times R_{SENSE}(nom)\right)} = \frac{61.9mV}{R_{SENSE}(nom)}$$

In this case, the application circuit must be sturdy enough to operate over a ~1.6-to-1 range in hot swap load currents. For example, if an MIC2594 circuit must pass a minimum hot swap load current of 4A without nuisance trips, R_{SENSE} should be set to $\frac{38.8mV}{4A} = 9.7m\Omega$, and the nearest 1% standard value is 9.76mΩ. At the other tolerance extremes, I_{HOT_SWAP}(max) for the circuit in question is then simply

$$I_{HOT\_SWAP}(max) = \frac{61.9mV}{9.76m\Omega} = 6.3A$$

With a knowledge of the application circuit's maximum hot swap load current, the power dissipation rating of the sense resistor can be determined using $P = I^2 \times R$. Here, the I is I_{HOT_SWAP}(max) = 6.3A and the R is R_{SENSE}(min) = (0.97)(R_{SENSE}(nom)) = 9.47mΩ. Thus, the sense resistor's maximum power dissipation is:

$$P_{MAX} = (6.3A)^2 \times (9.47m\Omega) = 0.376W$$

A 0.5Ω sense resistor is a good choice in this application.

Undervoltage/Overvoltage Detection—MIC2588

The MIC2588 has "UV" and "OV" input pins. These pins can be used to detect input supply rail undervoltage and overvoltage conditions. Undervoltage lockout prevents energizing the load until the supply input is stable and within tolerance. In a similar fashion, overvoltage turn-off prevents damage to sensitive circuit components should the input voltage exceed normal operational limits. Each of these pins is internally connected to an analog comparator with 20mV of hysteresis. When the UV pin falls below its V_{UVL} threshold or the OV pin is above its V_{OVH} threshold, the GATE pin is immediately pulled low. The GATE pin will be held low until UV exceeds its V_{UVH} threshold or OV drops below its V_{OVL} threshold. The UV and OV circuit's threshold trip points are programmed using the resistor divider

R1, R2, and R3 as shown in the *"Typical Application."* The equations to set the trip points are shown below. For the following example, the circuit's UV threshold is set to V_{UV} = 37V and the OV threshold is placed at V_{OV} = 72V, values commonly used in Central Office power distribution applications.

$$V_{UV} = V_{UVL}(typ) \times \frac{(R1+R2+R3)}{(R2+R3)}$$

$$V_{OV} = V_{OVH}(typ) \times \frac{(R1+R2+R3)}{R3}$$

Given V_{UV}, V_{OV}, and any one resistor value, the remaining two resistor values can be found. A suggested value for R3 is that which will provide approximately 100µA of current through the voltage divider chain at $V_{DD} = V_{UV}$. This yields the following as a starting point:

$$R3 = \frac{V_{OVH}(typ)}{100\mu A} = 12.23k\Omega$$

The closest standard 1% value for R3 = 12.4kΩ. Solving for R2 and R1 yields:

$$R2 = R3 \times \left[\left(\frac{V_{OV}}{V_{UV}}\right) - 1\right]$$

$$R2 = 12.4k\Omega \times \left[\left(\frac{72V}{37V}\right) - 1\right]$$

$$R2 = 11.729k\Omega$$

The closest standard 1% value for R2 = 11.8kΩ. Next, the value for R1 is calculated:

$$R1 = R3 \times \left(\frac{V_{OV} - 1.223V}{1.223V}\right) - R2$$

$$R1 = 12.4k\Omega \times \left(\frac{72V - 1.223V}{1.223V}\right) - R2$$

$$R1 = 705.808k\Omega$$

The closest standard 1% value for R1 = 698kΩ.

Using standard 1% resistor values, the circuit's nominal UV and OV thresholds are:

V_{UV} = 36.5V
V_{OV} = 71.2V

Programmable UVLO Hysteresis—MIC2594

The MIC2594 has user-programmable hysteresis by means of the ON and OFF pins. This allows setting the part to turn on at a voltage V1, and not turn off until a second voltage V2, where V2 < V1. This can significantly simplify dealing with source impedances in the supply bus while at the same time increasing the amount of available operating time from a loosely regulated power supply (for example, a battery supply). Similarly to the MIC2588, each of these pins is internally connected to an analog comparator with 20mV of hysteresis. The MIC2594 holds the output off until the voltage at the ON pin exceeds its V_{ONH} threshold value given in the *"Electrical Characteristics"* table. Once the output has been enabled by the ON pin, it will remain on until the voltage at the OFF pin falls below its V_{OFFL} threshold value, or the part turns off due to a fault. Should either event occur, the GATE pin is immediately pulled low and will remain low until the ON pin once again exceeds its V_{ONH} threshold. The circuit's turn-on and turn-off points are set using the resistor divider R1, R2, and R3 as shown in the *"Typical Application."* The equations to establish the trip points are shown below. In the following example, the circuit's ON threshold is set to V_{ON} = 40V and the circuit's OFF threshold is V_{OFF} = 35V.

$$V_{ON} = V_{ONH}(typ) \times \frac{(R1+R2+R3)}{R3}$$

$$V_{OFF} = V_{OFFL}(typ) \times \frac{(R1+R2+R3)}{(R2+R3)}$$

Given V_{OFF}, V_{ON}, and any one resistor value, the remaining two resistor values can be readily found. A suggested value for R3 is that which will provide approximately 100µA of current through the voltage divider chain at $V_{DD} = V_{OFF}$. This yields the following as a starting point:

$$R3 = \frac{V_{OFFL}(typ)}{100\mu A} = 12.23k\Omega$$

The closest standard 1% value for R3 = 12.4kΩ.

Then, solving for R2 and R1 yields:

$$R2 = R3 \times \left[\left(\frac{V_{ON}}{V_{OFF}}\right) - 1\right]$$

$$R2 = 12.4k\Omega \times \left[\left(\frac{40V}{35V}\right) - 1\right]$$

$$R2 = 1.771k\Omega$$

The closest standard 1% value for R2 = 1.78kΩ.

$$R1 = R3 \times \frac{(V_{ON} - 1.223V)}{1.223V} - R2$$

$$R1 = 12.4k\Omega \times \frac{(40V - 1.223V)}{1.223V} - R2$$

$$R1 = 391.380k\Omega$$

The closest standard 1% value for R1 = 392kΩ.

Using standard 1% resistor values, the circuit's nominal ON and OFF thresholds are:

V_{ON} = 40.1V
V_{OFF} = 35V

Applications Information

4-Wire Kelvin Sensing

Because of the low value typically required for the sense resistor, special care must be used to measure accurately the voltage drop across it. Specifically, the measurement technique across each R_{SENSE} must employ 4-wire Kelvin sensing. This is simply a means of making sure that any voltage drops in the power traces connecting to the resistors are not picked up by the signal conductors measuring the voltages across the sense resistors.

Figure 6 illustrates how to implement 4-wire Kelvin sensing. As the figure shows, all the high current in the circuit (from V_{EE} through R_{SENSE}, and then to the source of the output MOSFET) flows directly through the power PCB traces and R_{SENSE}. The voltage drop resulting across R_{SENSE} is sampled in such a way that the high currents through the power traces will not introduce any parasitic voltage drops in the sense leads. It is recommended to connect the hot swap controller's sense leads directly to the sense resistor's metalized contact pads.

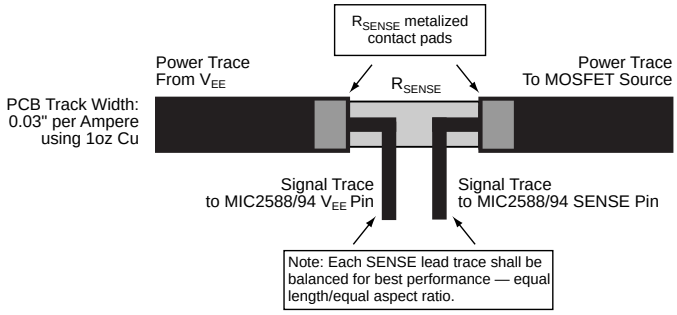


Figure 6. 4-Wire Kelvin Sense Connections for R_{SENSE}

Protection Against Voltage Transients

In many telecom applications, it is very common for circuit boards to encounter large-scale supply-voltage transients in backplane environments. Because backplanes present a complex impedance environment, these transients can be as high as 2.5 times steady-state levels, or 120V in worst-case situations. In addition, a sudden load dump anywhere on the circuit card can generate a very high voltage spike at the drain of the output MOSFET which, in turn, will appear at the DRAIN pin of the MIC2588/MIC2594. In both cases, it is good engineering practice to include protective measures to avoid damaging sensitive ICs or the hot swap controller from these large-scale transients. Two typical scenarios in which large-scale transients occur are described below:

1. An output current load dump with no bypass (charge bucket or bulk) capacitance to V_{EE}. For example, if L_{LOAD} = 5µH, V_{IN} = 56V and t_{OFF} = 0.7µs, the resulting peak short-circuit current prior to the MOSFET turning off would reach:

$$\frac{(55V \times 0.7\mu s)}{5\mu H} = 7.7A$$

   If there is no other path for this current to take when the MOSFET turns off, it will avalanche the drain-source junction of the MOSFET. Since the total energy represented is small relative to the sturdiness of modern power MOSFETs, it's unlikely that this will damage the transistor. However, the actual avalanche voltage is unknown; all that can be guaranteed is that it will be greater than the $V_{BD(D-S)}$ of the MOSFET. The drain of the transistor is connected to the DRAIN pin of the MIC2588/94, and the resulting transient does have enough voltage and energy and can damage this, or any, high-voltage hot swap controller.

2. If the load's bypass capacitance (for example, the input filter capacitors for a set of DC-DC converter modules) are on a board from which the board with the MIC2589/MIC2595 and the MOSFET can be unplugged, the same type of inductive transient damage can occur to the MIC2588/MIC2594.

Protecting the controller and the power MOSFET from damage against these large-scale transients can take the forms shown in Figure 7. It is not mandatory that these techniques are used—the application environment will dictate suitability. As protection against sudden on-card load dumps at the DRAIN pin of the controller, a 2.2µF or larger capacitor directly from DRAIN to V_{EE} of the controller can be used to serve as a charge reservoir. Alternatively, a 68V, 1W, 5% Zener diode clamp can be installed in a similar fashion. Note that the clamp diode's cathode is connected to the DRAIN pin as shown in Figure 7. To protect the hot swap controller from large-scale transients at the card input, a 100V clamp diode (an SMAT70A or equivalent) can be used. In either case, the lead lengths should be short and the layout compact to prevent unwanted transients in the protection circuit.

[Circuit drawing under construction]

Figure 7. Using Large-Scale Transient Protection Devices Around the MIC2588/94

Power buss inductance could easily result in localized high-voltage transients during a turn-off event. The potential for overstressing the part in such a case should be kept in check with a suitable input capacitor and/or transient clamping diode.

Power MOSFET Selection

[Section under construction]

Power MOSFET Operating Voltage Requirements

[Section under construction]

Power MOSFET Steady-State Thermal Issues

[Section under construction]

Power MOSFET Transient Thermal Issues

[Section under construction]

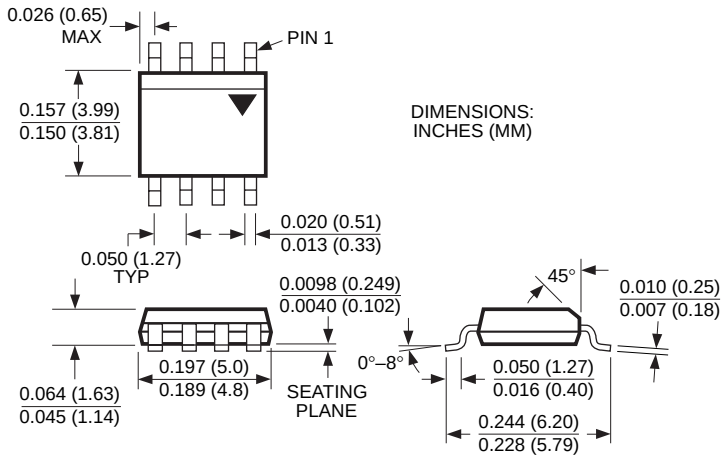
PCB Layout Considerations

[Section under construction]

Power MOSFET and Sense Resistor Vendors

[Section under construction]

Package Information



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