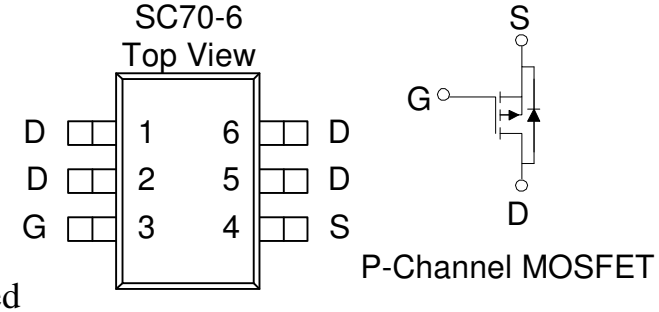
P-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SC70-6 saves board space
- Fast switching speed
- High performance trench technology

ESD Protected

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (OHM)	I_D (A)
-30	0.064 @ V_{GS} = -10V	-4.1
	0.096 @ V_{GS} = -4.5V	-3.3



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[a]	T_A=25°C	I_D	-4.1	A
	T_A=70°C		-3.3	
Pulsed Drain Current[b]		I_{DM}	-10	
Continuous Source Current (Diode Conduction)[a]		I_S	±1.4	A
Power Dissipation[a]	T_A=25°C	P_D	1.56	W
	T_A=70°C		0.81	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient[a]	t <= 5 sec	R_{THJA}	80	°C/W
	Steady-State		125	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

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SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Limits**			**Unit**
			Min	**Typ**	**Max**	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 uA	-1			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		V_{DS} = -24 V, V_{GS} = 0 V, T_J = 55°C			-10	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = -5 V, V_{GS} = -4.5 V	-5			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = -10 V, I_D = -1 A			64	mΩ
		V_{GS} = -4.5 V, I_D = -1 A			96	
Forward Tranconductance[A]	g_{fs}	V_{DS} = -5 V, I_D = -1 A		9		S
Diode Forward Voltage	V_{SD}	I_S = -0.46 A, V_{GS} = 0 V		-0.65		V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = -10 V, V_{GS} = -4.5 V, I_D = -1 A		4		nC
Gate-Source Charge	Q_{gs}			1		
Gate-Drain Charge	Q_{gd}			2		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -10 V, I_L = -1 A, V_{GEN} = -4.5 V, R_G = 6 Ω		9		ns
Rise Time	t_r			4		
Turn-Off Delay Time	$t_{d(off)}$			1		
Fall-Time	t_f			2		

Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

c. Repetitive rating, pulse width limited by junction temperature.

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