Power Management ICs for Automotive Body Control

Regulator with
Voltage Detector and Watchdog Timer

BD3021HFP-M   No.10039EAT10

● Description

BD3021HFP-M is a regulator IC with integrated WDT (Watch Dog Timer), high output voltage accuracy ±2.0% and 80μA (Typ.) low circuit current consumption. BD3021HFP-M supports usage of low ESR ceramic capacitor for output stability. BD3021HFP-M can be a stable power supply for any applications while detecting malfunction of microcontrollers.

● Features

1) WDT Can be Switched ON/OFF by Using INH Pin
2) Low Circuit Current: 80μA(Typ.)
3) Output Circuit: Pch DMOS
4) High Output Voltage Accuracy: 5V±2%
5) Supports Low ESR Ceramic Capacitor
6) Vcc Max Voltage: 50V
7) Integrated Over Current Protection and Thermal Shut Down
8) HRP7 packaging

● Applications

Any application using a microcontroller or a DSP such as automotive (body control), display, server, DVD, phone, etc…

● Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply Voltage [*1]	Vcc	-0.3 ~ +50	V
INH pin voltage	VINH	-0.3 ~ +15	V
Regulator output pin voltage	VOUT	-0.3 ~ +15	V
Reset output pin voltage	VRESET	-0.3 ~ +15	V
Watchdog input pin voltage	VCLK	-0.3 ~ +15	V
Reset delay setting pin voltage	VCT	-0.3 ~ +15	V
Power dissipation [*2]	Pd	1.6	W
Operating temperature range	Topr	-40 ~ +125	℃
Storage temperature range	Tstg	-55 ~ +150	℃
Maximum junction temperature	Tjmax	150	℃

*1 Not to exceed Pd.
*2 Reduced by 12.8W / °C over Ta = 25°C, when mounted on glass epoxy board: 70mm×70mm×1.6mm.

● Operating conditions (Ta=-40~125°C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage [*3]	Vcc	5.6	36.0	V
Output Current	Io	0	500	mA

*3 For the output voltage, consider the voltage drop (dropout voltage) due to the output current.

NOTE: This product is not designed for protection against radioactive rays.

2010.11 - Rev.A

●**Electrical characteristics** (Unless otherwise specified, Ta=25°C, Vcc=13.5V, CLK=GND)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Overall Device						
Bias current 1	Icc1	—	80	130	μA	Io=0mA
Bias current 2	Icc2	—	150	300	μA	Io=50mA(Ta=25°C)
Regulator						
Output voltage	VOUT	4.90	5.00	5.10	V	Io=200mA
Line regulation	Line.Reg	—	5	35	mV	Vcc=5.6 ~ 36V
Load regulation	Load.Reg	—	30	70	mV	Io=5 ~ 200mA
Dropout voltage	ΔVd	—	0.3	0.6	V	Vcc=4.75V, Io=200mA
Ripple rejection	R.R.	45	55	—	dB	f=120Hz, ein=1Vrms, Io=100mA
Reset						
Detection voltage	Vdet	4.40	4.50	4.60	V	
Hysteresis width	VHS	50	100	150	mV	
Output delay time Low→High (Power on reset time)	TdLH	1.1	1.9	2.7	ms	Vcc=Vdet±0.5V(Vcc=VOUT) INH=Open,CT=0.01μF
Output delay time High→Low	TdHL	—	100	300	μs	Vcc=Vdet±0.5V(Vcc=VOUT) INH= Open,CT=0.01μF
RESET discharge urrent	IRESET	0.2	—	—	mA	Vcc=1.5V,RESET=0.5V (Vcc=VOUT)
CT discharge current	Ict	0.1	—	—	mA	Vcc=1.5V,CT=0.5V (Vcc=VOUT)
Low output voltage	VRST	—	0.1	0.2	V	VOUT=4.0V
Min. operating voltage	VOPL	1.5	—	—	V	
Watchdog timer						
CT switching threshold voltage High	VthH	1.08	1.15	1.25	V	WDT ON, INH= Open
CT switching threshold voltage Low	VthL	0.13	0.15	0.17	V	WDT ON, INH= Open
WDT Charge current	Ictc	3.5	6.0	8.5	μA	WDT ON, INH= Open, CT=0V
WDT Discharge current	Ictd	1.2	2.0	2.8	μA	WDT ON, INH= Open, CT=1.3V
Watchdog monitor time Low	TWH	3.0	5.0	7.0	ms	WDT ON, INH= Open, CT=0.01μF(Ceramic Cap) ※Characteristics of ceramic cap not considered.
Watchdog reset time	TWL	1.0	1.7	2.4	ms	
CLK Input pulse width	TWCLK	500	—	—	ns	
INH						
WDT OFF threshold Voltage	VHINH	VOUT×0.8	—	VOUT	V	
WDT ON threshold voltage	VLINH	0	—	VOUT×0.3	V	
INH Input current	IINH	—	10	20	μA	INH=5V

●**Electrical characteristics** (Unless otherwise specified, Ta=25°C, Vcc=13.5V, CLK=GND)
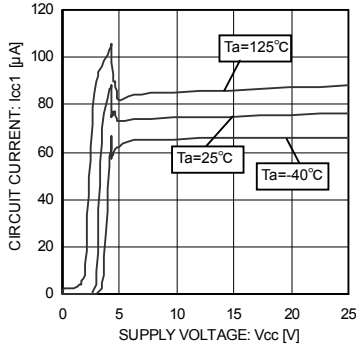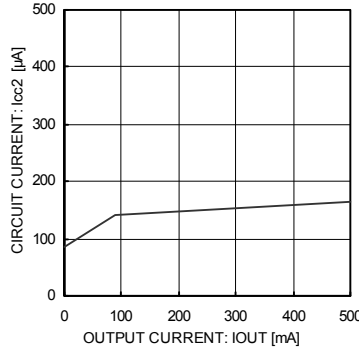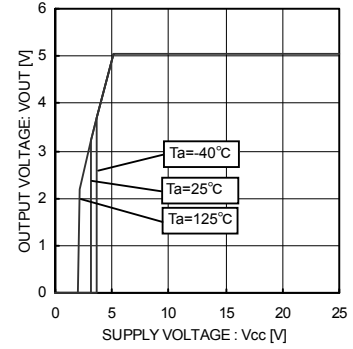
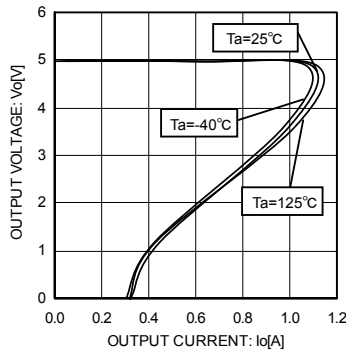Fig.1 Circuit Current

Fig.2 Circuit Current

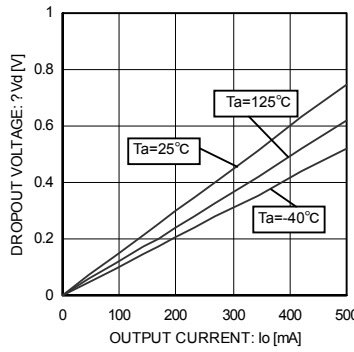Fig.3 Input Stability

Fig. 4 Load Stability
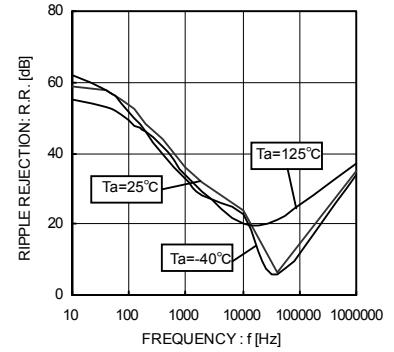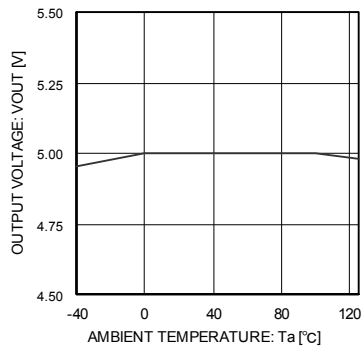
Fig.5 Dropout Voltage

Fig. 6 Ripple Rejection
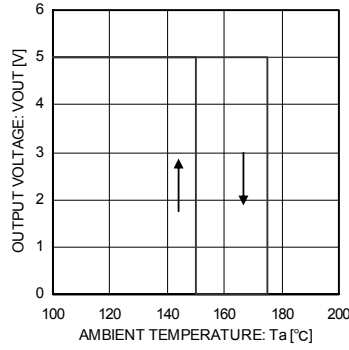
Fig. 7 Output Voltage
Temperature Characteristics

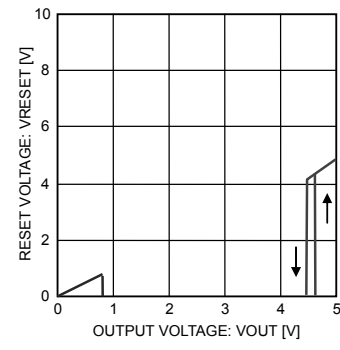Fig.8 Thermal Shutdown
Circuit Characteristics
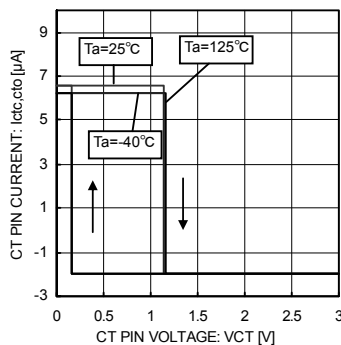
Fig.9 Restion Voltage
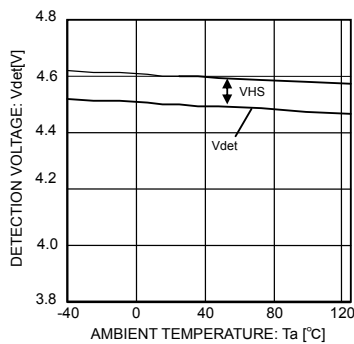(Vcc=VOUT)

Fig.10 CT Pin Charge / Discharge
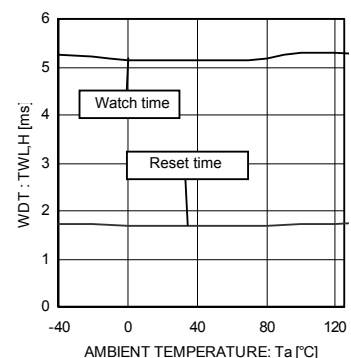Current (Vcc=5V)

Fig.11 Reset Detection
Voltage vs. Temperature
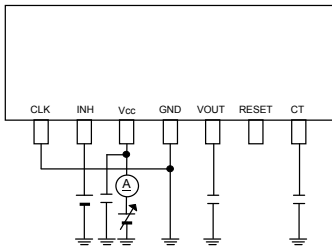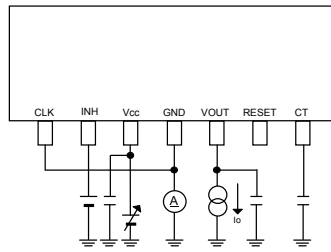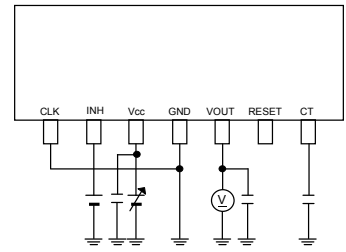
Fig.12 WDT Time vs. Temperature
(CT=0.01µF)

●Measurement Circuit for Reference Data

Measurement Circuit of Fig.1

Measurement Circuit of Fig.2

Measurement Circuit of Fig.3
and Fig.7 and Fig.8
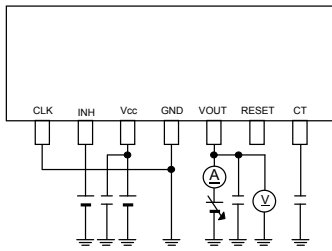
Measurement Circuit of Fig.4
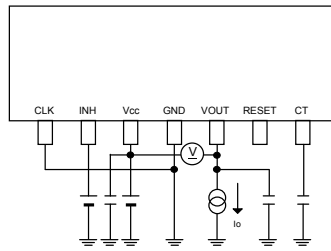
Measurement Circuit of Fig.5
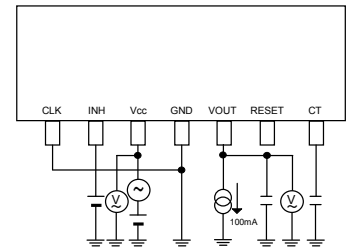
Measurement Circuit of Fig.6
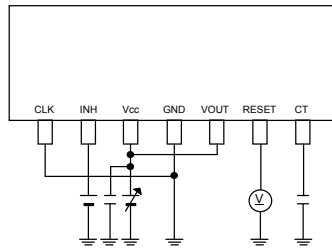
Measurement Circuit of Fig.9
and Fig11
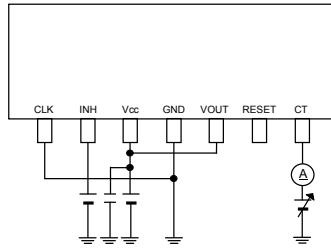
Measurement Circuit of Fig.10
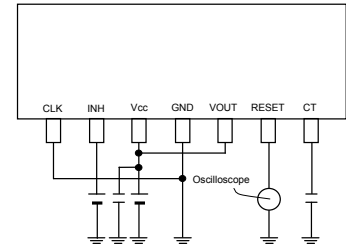
Measurement Circuit of Fig.12

●Block diagrams
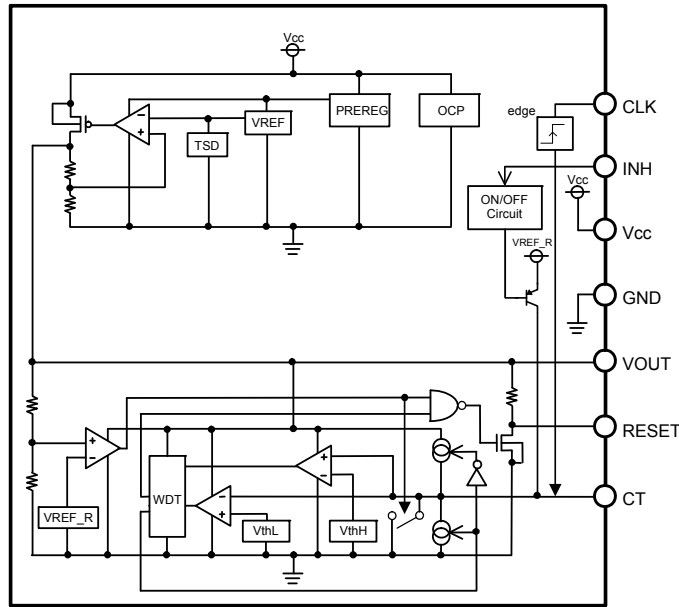
Fig.13

Pin No.	Pin Name	Function
1	CLK	Clock Input from Microcontroller
2	INH	WDT ON/OFF Function Pin
3	Vcc	Power Supply Pin
4	GND	GND
5	VOUT	Voltage Output Pin
6	RESET	Reset Output Pin
7	CT	External Capacitance for Reset Output Delay Time, WDT Monitor Time Setting Connection Pin
Fin	GND	GND

●TOP VIEW (Package dimension)

HRP7

(Unit : mm)
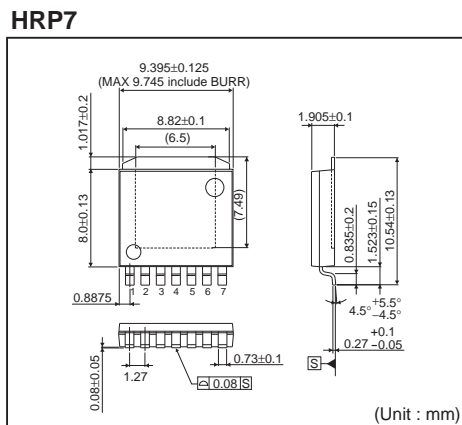
●Input / Output Equivalent Circuit Diagrams (Resistance value is typical value)
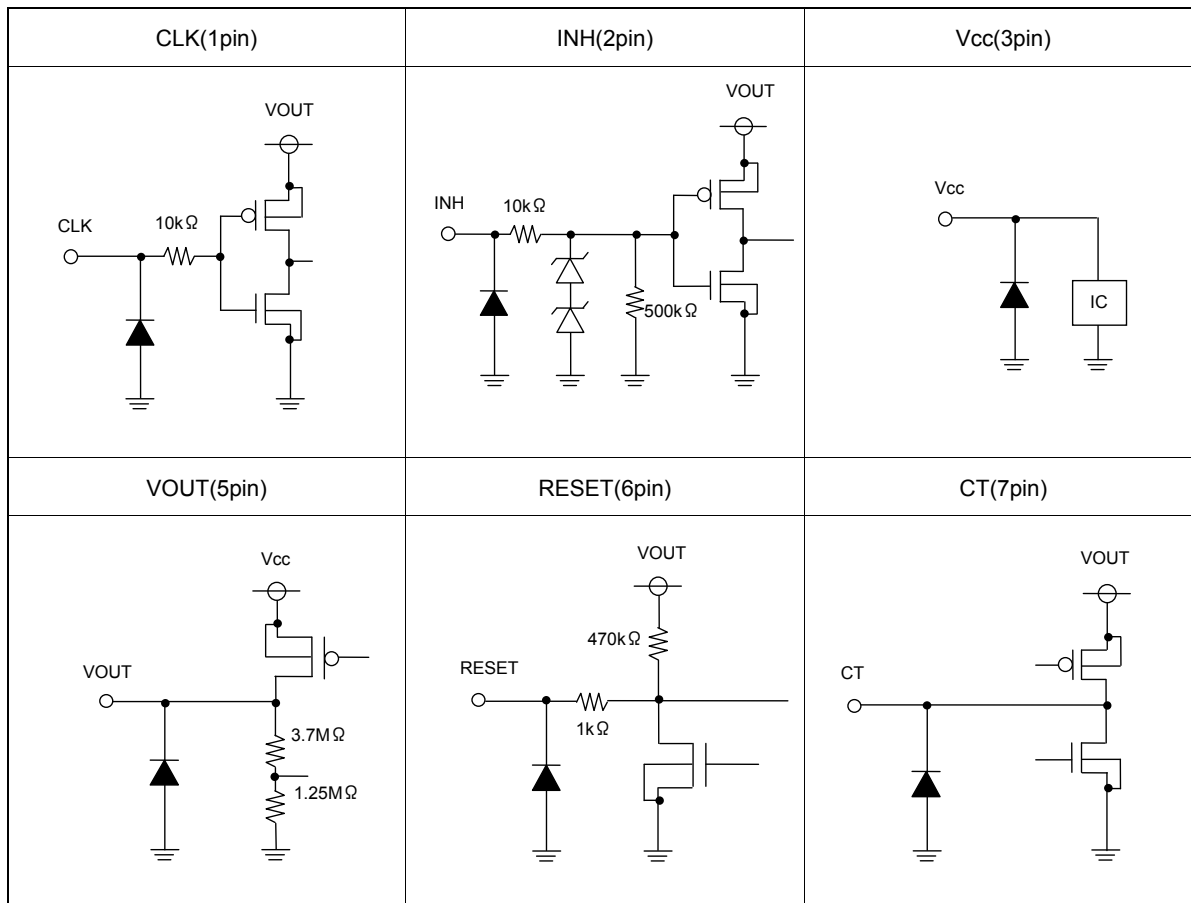
●**BD3021HFP-M** (Power on Reset / Watchdog Timer)

Power ON reset (output delay time) is adjustable by CT pin capacitor.

TdLH(S) ≒(1.15V × CT capacitance(µF) / Ictc(µA)   (Typ.)

・TdLH   :Output delay time(power ON reset)
・1.15V   :Upper switching threshold voltage(Typ.)
・CT capacitance   :capacitor connected to CT pin
・Ictc   :WDT charge current

Calculation example) with 0.01µF CT pin capacitor

TdLH(S)=1.15V × 0.01µF/6µA

≒1.9msec

※If the CT capacitance is not the same as the condition on the electrical characteristics table, i.e., 0.01µF, choose the capacitance value in ratio referring to the above equation.

Watch Dog Timer (WDT watch time, reset time) is adjustable by the CT pin capacitor

TWH(S) ≒(1.00V × CT capacitance (µF))/ Ictd(µA) (Typ.)

TWL(S) ≒(1.00V × CT capacitance (µF))/ Ictc(µA) (Typ.)

・TWH   :WDT watch time (delay time to turn the reset ON)
・TWL   :WDT reset time (time the reset is ON)
・1.00V   :Upper switching threshold voltage － lower switching threshold voltage
・CT capacitance :CT pin capacitor   ※Shared with power ON reset
・Ictc   :WDT charge current
・Ictd   :WDT discharge current

Calculation example) with 0.01µF CT pin capacitor

TWH(S)≒1.00V × 0.01µF/2µA≒5.0msec   (Typ.)

TWL(S)≒1.00V × 0.01µF/6µA≒1.7msec   (Typ.)

※If the CT capacitance is not the same as the condition on the electrical characteristics table, i.e., 0.01µF, choose the capacitance value in ratio referring to the above equation.

＜Timing Chart＞
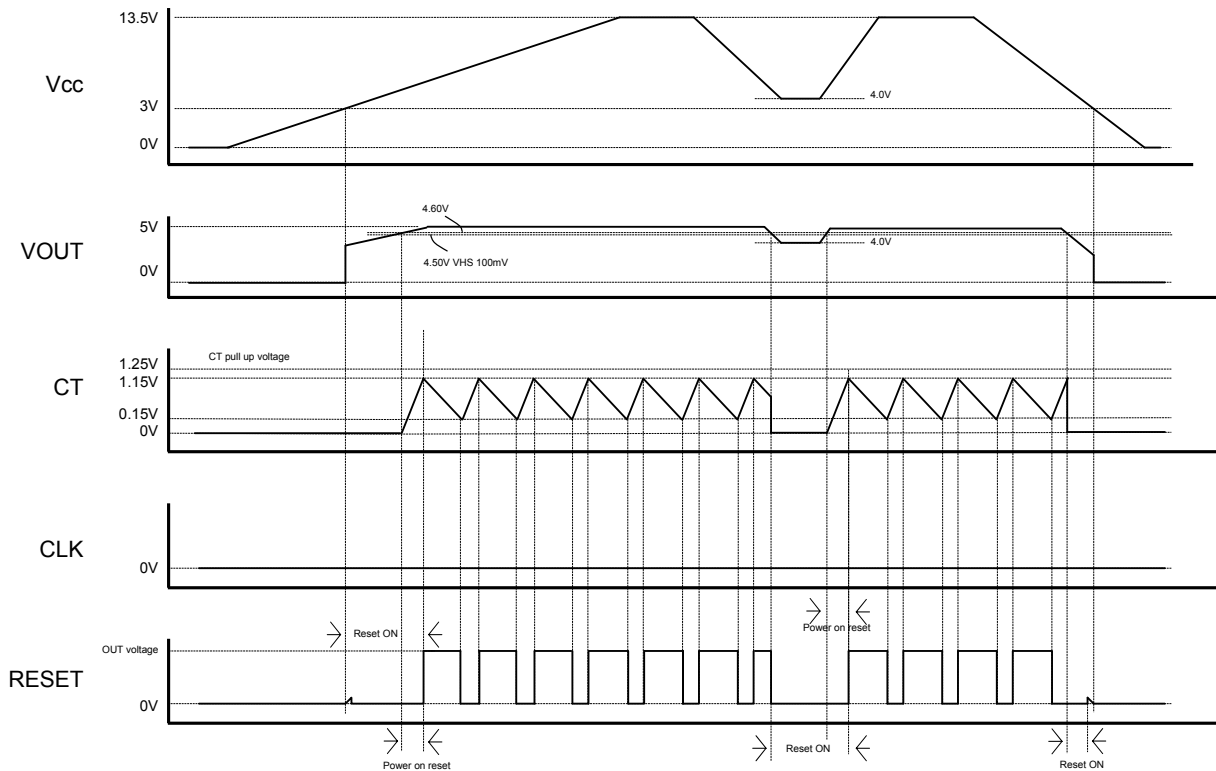
●**WDT timer ON/OFF switch INH** (Resistance value is typical value)

BD3021HFP-M has a switch INH to turn the WDT ON/OFF
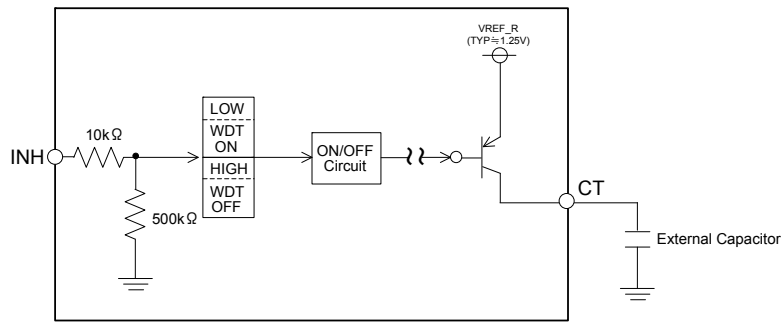
IC Internal Block Diagram

By using INH ON, CT potential can be pulled up to internal voltage VREF_R (invalid with power ON reset))

<**Timing Chart**>

＜Timing Chart＞
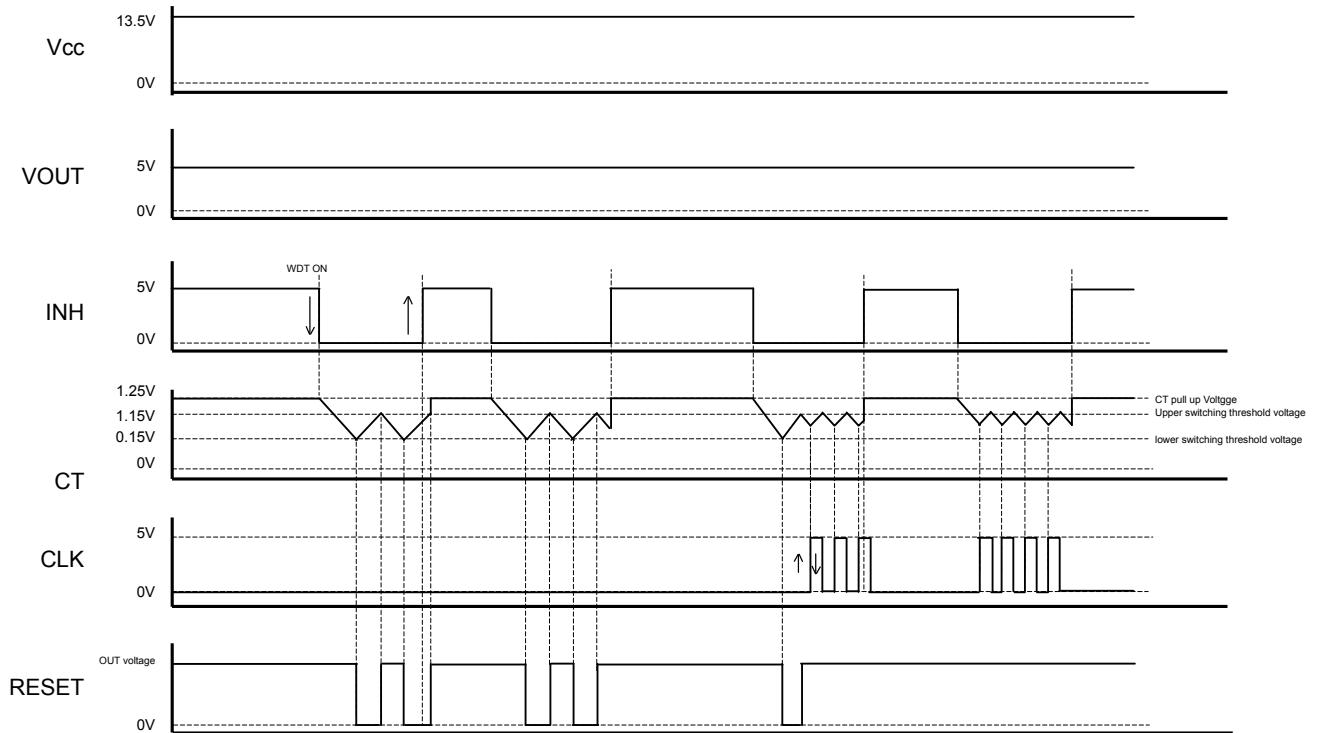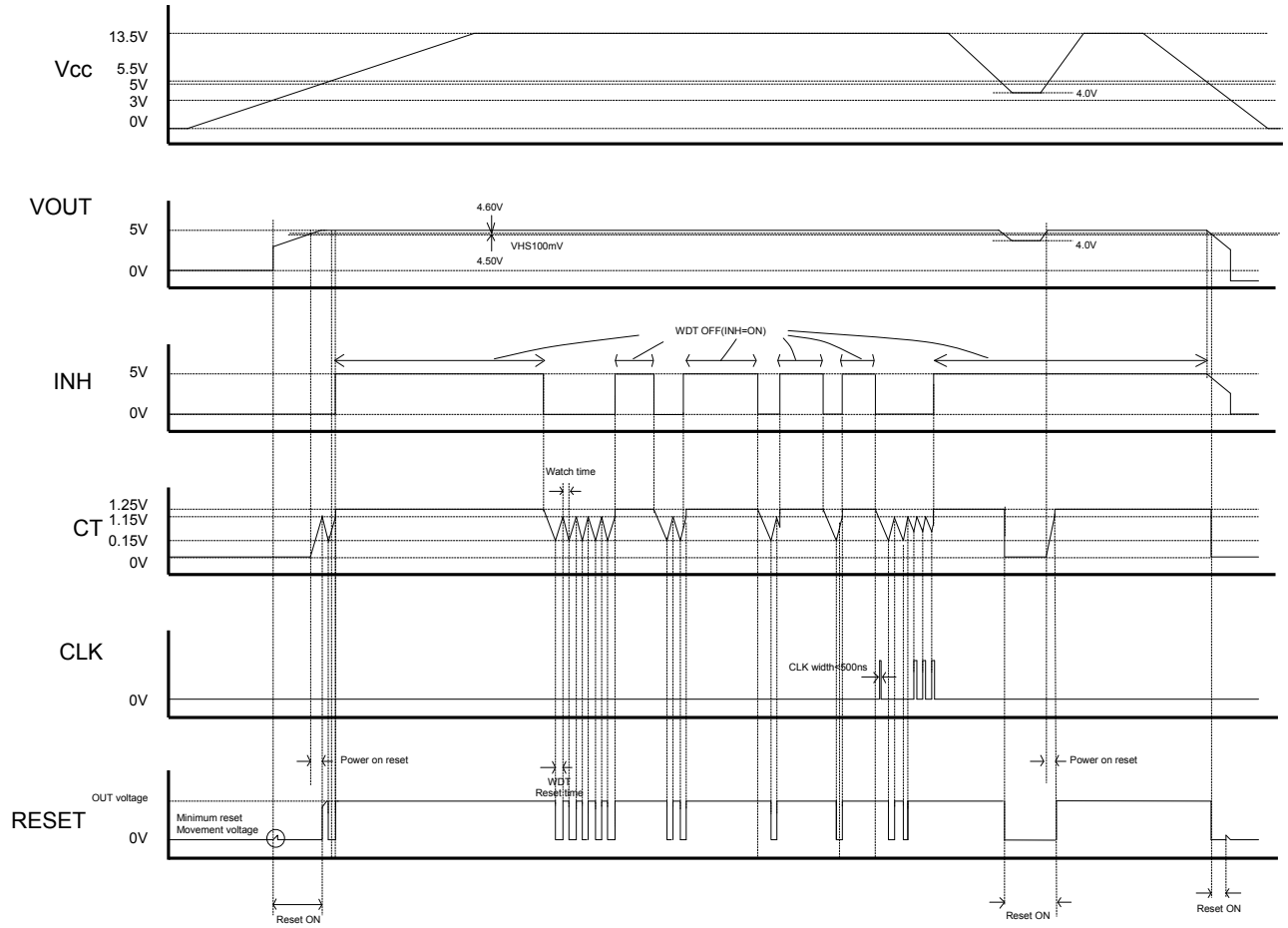
●Thermal Design
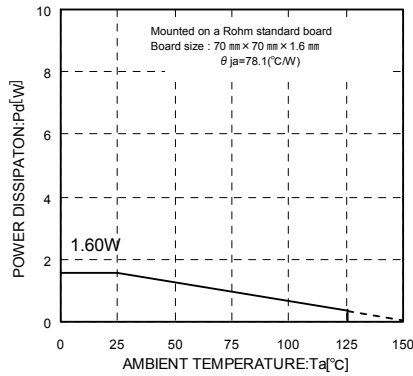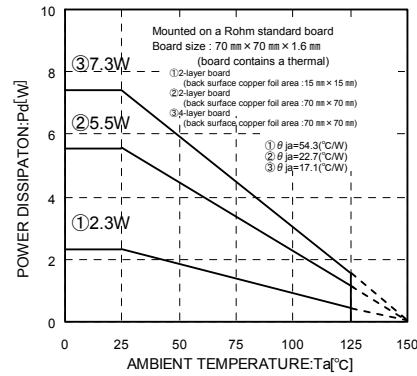
Fig.14

Fig.15

Refer to Fig.14 and Fig.15 thermal dissipation characteristics for usage above Ta=25℃. The IC's characteristics are affected heavily by the temperature, and if is exceeds its max junction temperature (Tjmax), the chip may degrade or destruct. Thermal design is critical in terms of avoiding Instantaneous destruction and reliability in long term usage. The IC needs to be operated below its max junction temperature (Tjmax) to avoid thermal destruction. Refer to Fig.14 and Fig.15 for HRP7 package thermal dissipation characteristics. Operate the IC within power dissipation (Pd) when using this IC.
Power consumption Pc(W) calculation will be as below (for Fig.15③)

Pc=(Vcc−VOUT)×Io+Vcc×Icc2
Power dissipation Pd≧Pc

Vcc : Input Voltage
VOUT : Output Voltage
Io : Load Current
Icc2 : Circuit Current

If load current Io is calculated to operate within power dissipation, it will be as below, where you can find the max load current IoMax for the applied voltage Vcc of the thermal design.

$$Io \leqq \frac{Pd - Vcc \times Icc2}{Vcc - VOUT}$$ (Refer to Fig2 for Icc2)

Example) at Ta=125℃,Vcc=12V,VOUT=5V

$$Io \leqq \frac{1.46 - 12 \times Icc2}{12 - 5}$$
Io ≦ 208mA (Icc2=150μA)

Fig.15③ : θja=17.1℃/W → -58.4mW/℃
25℃=7.3W → 125℃=1.46W

Refer to above and adjust the thermal design so it will be within power dissipation within the entire operation temperature range.   Below is the power consumption Pc calculation when (VOUT-GND short)

Pc=Vcc×(Icc2+Ishort)   Ishort: short current

(Refer to Fig.4 for I short)

●Pin Settings / Precautions

1. Vcc Pin
    Insert a 0.33 ~ 1000μF capacitor between the Vcc and GND pins. The appropriate capacitance value varies by application. Be sure to allow a sufficient margin for input voltage levels.

2. Output pins
    It is necessary to place capacitors between each output pin and GND to prevent oscillation on the output. Usable capacitance values range from 0.1μF ~ 1000μF. Abrupt fluctuations in input voltage and load conditions may affect the output voltage. Output capacitance values should be determined only through sufficient testing of the actual application.

Vcc=5.6V～36V
Ta=-40℃～+125℃   Io=0A～500mA
Cin=0.33μF～100μF   Cout=0.1μF～100μF
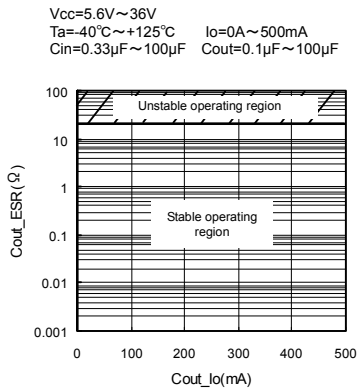
ESR vs Io(reference data)
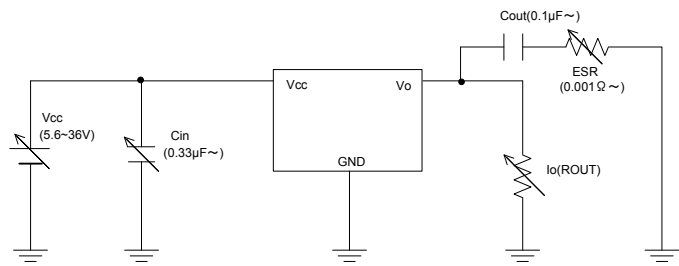
※Pin Settings / Precautions 2 Measurement circuit

3. CT pin
    Connecting a capacitance of 0.01μF　 ~ 1μF on the CT pin is recommended.

●Notes for use

1. Absolute maximum ratings
   Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.

2. Electrical characteristics described in these specifications may vary, depending on temperature, supply voltage, external circuits and other conditions. Therefore, be sure to check all relevant factors, including transient characteristics.

3. GND potential
   The potential of the GND pin must be the minimum potential in the system in all operating conditions. Ensure that no pins are at a voltage below the GND at any time, regardless of transient characteristics.

4. Ground wiring pattern
   When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents.   Also ensure that the GND traces of external components do not cause variations on GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

5. Inter-pin shorts and mounting errors
   Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply or GND pins (caused by poor soldering or foreign objects) may result in damage to the IC.

6. Operation in strong electromagnetic fields
   Using this product in strong electromagnetic fields may cause IC malfunction. Caution should be exercised in applications where strong electromagnetic fields may be present.

7. Testing on application boards
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Thermal consideration
   Use a thermal design that allows for a sufficient margin in light of the Pd in actual operating conditions.
   Consider Pc that does not exceed Pd in actual operating conditions. (Pd≧Pc)

   > Tjmax : Maximum junction temperature=150℃, Ta : Peripheral temperature[℃] ,
   > θja : Thermal resistance of package-ambience[℃/W], Pd : Package Power dissipation [W],
   > Pc : Power dissipation [W],   Vcc : Input Voltage, VOUT : Output Voltage, Io : Load, Icc2 : Bias Current2

   Package Power dissipation : Pd (W)=(Tjmax－Ta)/θja
   Power dissipation   : Pc (W)=(Vcc－VOUT)×Io+Vcc×Icc2

9. Over current protection circuit (OCP)
   The IC incorporates an integrated over-current protection circuit that operates in accordance with the rated output capacity. This circuit serves to protect the IC from damage when the load becomes shorted. It is also designed to limit output current (without latching) in the event of a large and instantaneous current flow from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous or transitive operation of the protection circuits.

10. Thermal shutdown circuit (TSD)
    The IC incorporates a built-in thermal shutdown circuit, which is designed to turn the IC off completely in the event of thermal overload. It is not designed to protect the IC from damage or guarantee its operation. ICs should not be used after this function has activated, or in applications where the operation of this circuit is assumed.

11. Applications or inspection processes where the potential of the Vcc pin or other pins may be reversed from their normal state may cause damage to the IC's internal circuitry or elements. Use an output pin capacitance of 1000μF or lower in case Vcc is shorted with the GND pin while the external capacitor is charged. Insert a diode in series with Vcc to prevent reverse current flow, or insert bypass diodes between Vcc and each pin.
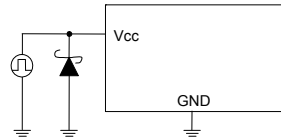
12. Positive voltage surges on VCC pin
    A power zener diode should be inserted between VCC and GND for protection against voltage surges of more than 50V on the VCC pin.
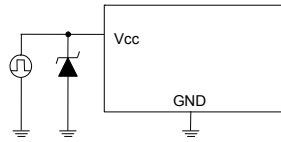
13. Negative voltage surges on VCC pin
    A schottky barrier diode should be inserted between VCC and GND for protection against voltages lower than GND on the VCC pin.

14. Output protection diode
    Loads with large inductance components may cause reverse current flow during startup or shutdown.
    In such cases, a protection diode should be inserted on the output to protect the IC.
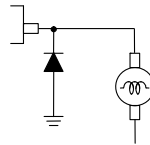
15. Regarding input pins of the IC
    This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors.
    For example (refer to the figure below):
    ○When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
    ○When GND > Pin B, the PN junction operates as a parasitic transistor
    Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.
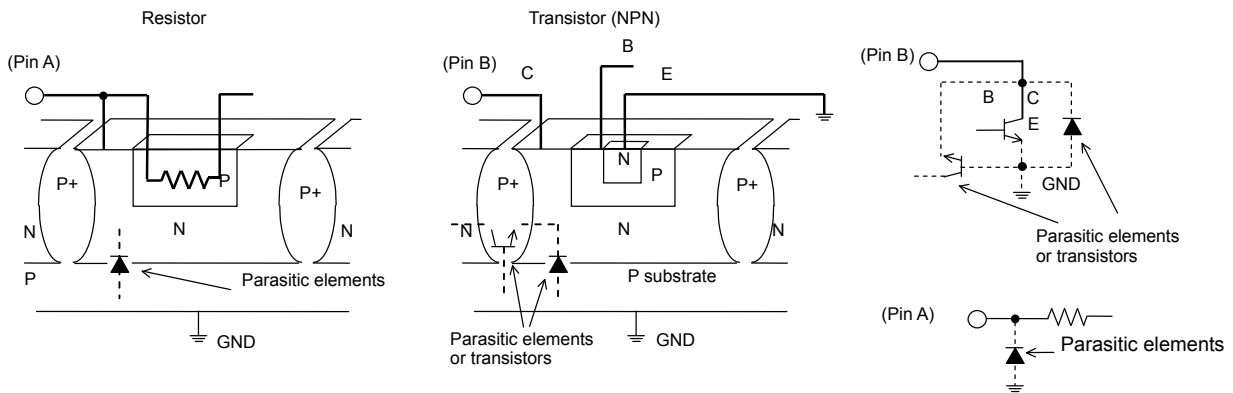
Example of Simple Monolithic IC Architecture

●Ordering part number

| B | D | | 3 | 0 | 2 | 1 | | H | F | P | - | M | | T | R |

Part No.　　　Part No.

Package
HFP:HRP7

Packaging and forming specification
E2: Embossed tape and reel

HRP7

9.395±0.125
(MAX 9.745 include BURR)
1.017±0.2
8.82±0.1
(6.5)
1.905±0.1
8.0±0.13
(7.49)
0.835±0.2
1.523±0.15
10.54±0.13
0.8875
1 2 3 4 5 6 7
4.5° +5.5°/−4.5°
0.27 +0.1/−0.05
0.08±0.05
1.27
0.73±0.1
0.08 S
S
(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)

1pin

Reel

Direction of feed

＊Order quantity needs to be multiple of the minimum quantity.

Notes

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