

Process C1227

HV BiCMOS 1.2 μ m

30V Double Metal - Double Poly

Electrical Characteristics

T=25°C Unless otherwise noted

	Symbol	Minimum	Typical	Maximum	Unit	Comments
N-Channel High Voltage Transistor						
Threshold Voltage	HVT _N	0.7	0.9	1.1	V	
Punch Through Voltage	HVBVDSS _P	36			V	
ON Resistance	HVPR _{ON}		1.4		m Ω -cm ²	@V _{GS} = 5V V _{DS} = 0.1V
Operating Voltage			V _{GS} = 5V V _{DS} = 30V		V	
N-Channel Low Voltage Transistor						
Threshold Voltage	VT _N	0.4	0.6	0.8	V	100x1.4 μ m
Body Factor	γ _N	0.50	0.65	0.80	V ^{1/2}	100x1.4 μ m
Conduction Factor	β _N	64.0	75.0	86.0	μ A/V ²	100x100 μ m
Effective Channel Length	Leff _N	1.20	1.35	1.50	μ m	100x1.4 μ m
Width Encroachment	Δ W _N		0.45		μ m	Per side
Punch Through Voltage	BVDSS _N	8			V	
Poly Field Threshold Voltage	VTFP _N	10	18		V	

	Symbol	Minimum	Typical	Maximum	Unit	Comments
P-Channel High Voltage Transistor						
Threshold Voltage	HVT _P	-0.7	-0.9	-1.1	V	
Punch Through Voltage	HVBVDSS _P	-36			V	
ON Resistance	HVPR _{ON}		11.0		m Ω -cm ²	@V _{GS} = -5V @V _{DS} = -0.1V
P-Channel Low Voltage Transistor						
Threshold Voltage	VT _P	-0.8	-0.6	-0.4	V	100x1.4 μ m
Body Factor	γ _P	0.35	0.50	0.65	V ^{1/2}	100x1.4 μ m
Conduction Factor	β _P	20.0	25.0	30.0	μ A/V ²	100x100 μ m
Effective Channel Length	Leff _P	1.35	1.50	1.65	μ m	100x1.4 μ m
Width Encroachment	Δ W _P		0.40		μ m	Per side
Punch Through Voltage	BVDSS _P	-8			V	
Poly Field Threshold Voltage	VTF _{P(P)}	-10	-18		V	

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C _{OX}	1.338	1.439	1.569	fF/ μ m ²	
Metal-1 to Poly1	C _{M1P}	0.040	0.046	0.052	fF/ μ m ²	
Metal-2 to Metal-1	C _M	0.043	0.050	0.057	fF/ μ m ²	

Vertical NPN Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h _{FE}	50	140	240		4.5x4.5 μ m
Early Voltage	V _A		34		V	
Cut-Off Frequency	f _t		1.89		GHz	

Physical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Starting Material $\rho < 100 >$						
Well(field)Sheet Resistance	$\rho_{N\text{-well}(f)}$	1.5	2.1	2.7	K Ω/\square	n-well
N+ Sheet Resistance	ρ_{N+}	20.0	35.0	50.0	Ω/\square	
N+ Junction Depth	X_{jN+}		0.4		μm	
P+ Sheet Resistance	ρ_{P+}	50.0	75.0	100.0	Ω/\square	
P+ Junction Depth	X_{jP+}		0.4		μm	
Base Resistance	RSHB_RB	1.33	1.66	2.00	K Ω/sq	
High-Voltage Gate Oxide	HT _{GOX}		22		nm	
Gate Oxide Thickness	T _{GOX}		22		nm	
Interpoly Oxide Thickness	IP _{OX}	33.6	42	50.4	nm	
Gate Poly Sheet Resistance	$\rho_{\text{POLY}1}$	15.0	22.0	30.0	Ω/\square	
Poly2 Resistivity	RSH_PL P	1.5	2	2.5	k Ω/\square	
Metal-1 Sheet Resistance	ρ_{M1}	35.0	45.0	65.0	m Ω/\square	
Metal-2 Sheet Resistance	ρ_{M2}	19.0	25.0	35.0	m Ω/\square	
Passivation Thickness	T _{PASS}		200+900		nm	oxide+nitride

Layout Rules

Min Channel Width	4.0 μm	Diffusion Overlap of Contact	1.0 μm
Min Spacing, Active Region, 5V	2.0 μm	Poly Overlap of Contact	1.0 μm
Poly1 Width/Space	1.4/2.0 μm	Metal-1 Overlap of Contact	1.5 μm
Poly2 Width/Space	3.0/2.0 μm	Contact to Poly Space	1.5 μm
Contact Width/Space	1.4x1.4 μm	Minimum Pad Opening	65x65 μm
Via Width/Space	1.4/1.6 μm	Metal-1 Overlap of Via	1.0 μm
Metal-1 Width/Space	2.6/1.6 μm	Metal-2 Overlap of Via	1.0 μm
Metal-2 Width/Space	2.6/1.6 μm	Minimum Pad Opening	65x65 μm
Gate Poly Width/Space	1.5/2.0 μm	Minimum Pad to Pad Spacing	5.0 μm
N+/P+ Width/Space	2.5/2.0 μm	Minimum Pad Pitch	80 μm