National Semiconductor

PRELIMINARY
November 2004

LP3942
The Dual RGB LED Controller with 1.5x/2x Charge Pump and SPI Interface

General Description

The LP3942 is an integrated stand-alone RGB LED controller with a high efficiency and low noise programmable 1.5x and 2x charge pump. The RGB LEDs are controlled through the low voltage SPI interface. RGB programmability allows unique color and brightness control with both RGB outputs. The color control has preselected color settings for color blending. The LED current control is done using constant current sinks that can be also used as switches. The non-overlapping RGB output PWM control minimizes the input noise.

See also: LP3931, LP3933 and LP3936 Lighting Management Units

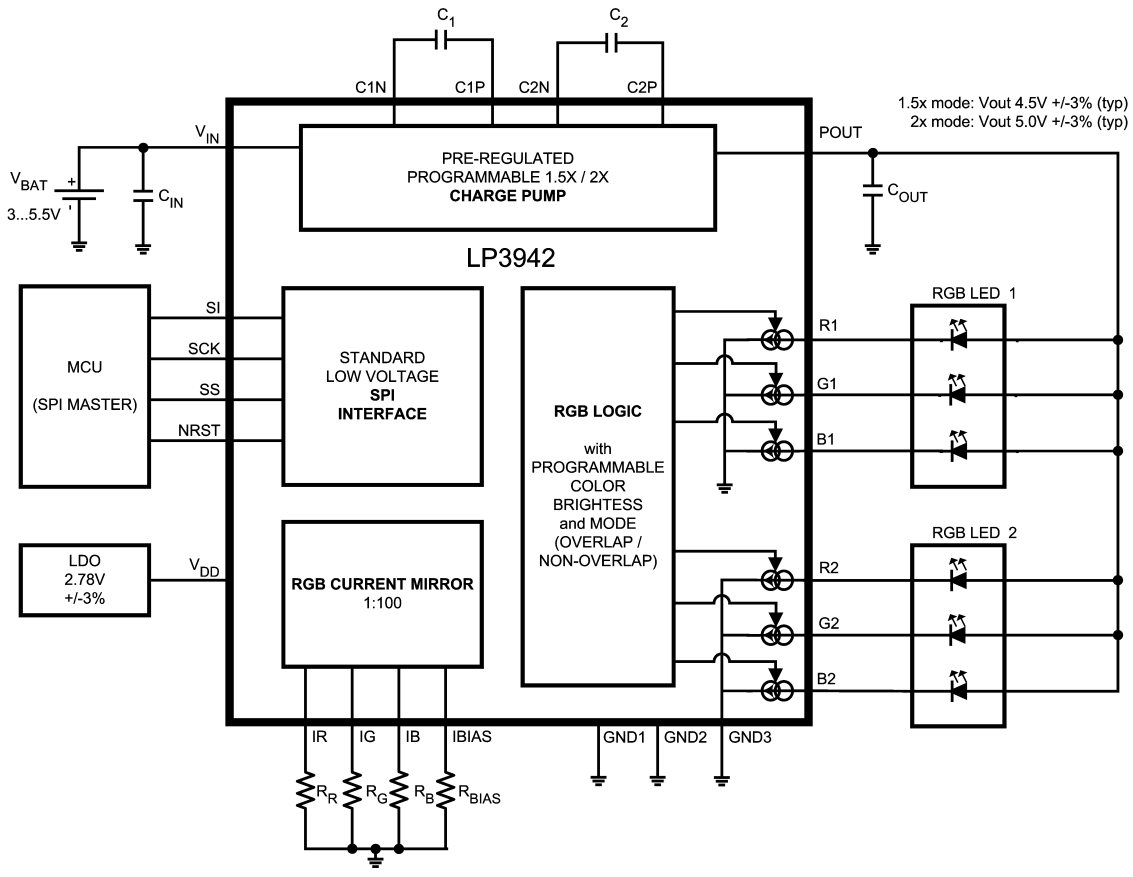
Features

- Pre-regulated 1.5x and 2x charge pump with regulated output (4.5V and 5.0V)
- 2 separately controlled PWM RGB LED drivers with programmable color and brightness
- Overlapping and non-overlapping RGB mode
- Wide input voltage range 3V–5.0V
- Output current up to 120 mA
- Low voltage SPI interface
- Programmable low current Standby mode
- Tiny LLP24 package (5mm*4mm*0.8mm)

Applications

- Cellular Phones, PDAs

Typical Application



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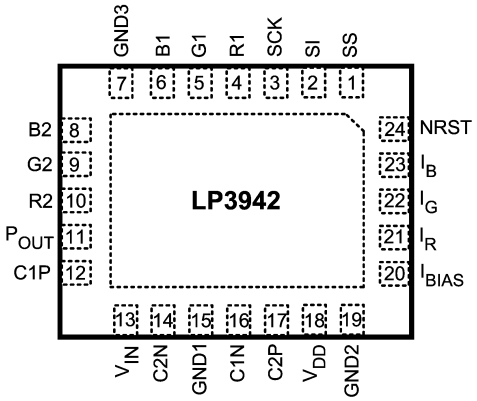
Connection Diagrams and Package Mark Information

24-Lead LLP package (5 mm*4 mm*0.8 mm), Bumped
See NS Package Number YQA24A



TOP VIEW

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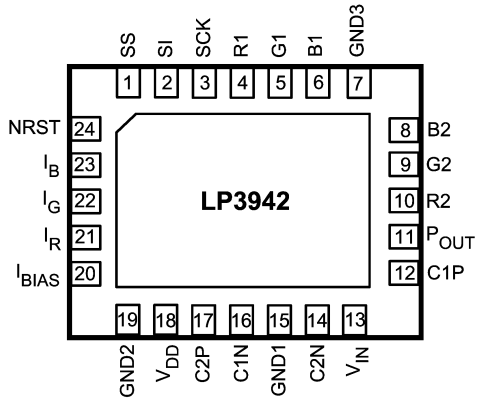
Top View



BOTTOM VIEW

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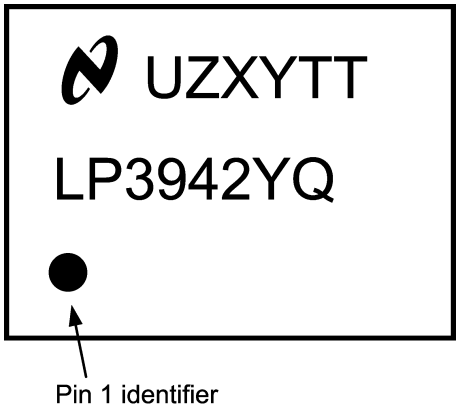
Bottom View



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Package Mark—Top View

Note: The actual physical placement of the package marking will vary from part to part. The package marking "XY" designates the date code. "UZ" and "TT" are NSC internal codes for die manufacturing and assembly traceability. Both will vary considerably.

Ordering Information

Order Number	Package Marking	Supplied As
LP3942YQ	LP3942YQ	1000 units, Tape-and-Reel
LP3942YQX	LP3942YQX	2500 units, Tape-and-Reel

Pin Description

Pin #	Name	Type	Description
1	SS	Logic Input	SPI Slave Select
2	SI	Logic Input	SPI Serial Data
3	SCK	Logic Input	SPI Clock
4	R1	Output	Open Drain, Red LED (1)
5	G1	Output	Open Drain, Green LED (1)
6	B1	Output	Open Drain, Blue LED (1)
7	GND3	Ground	Ground 3
8	B2	Output	Open Drain, Blue LED (2)
9	G2	Output	Open Drain, Green LED (2)
10	R2	Output	Open Drain, Red LED (2)
11	P_{OUT}	Output	Charge Pump Output
12	C1P		Flying capacitor C1 connection
13	V_{IN}	Power	Input voltage from battery
14	C2N		Flying capacitor C2 connection
15	GND1	Ground	Ground 1
16	C1N		Flying capacitor C1 connection
17	C2P		Flying capacitor C2 connection
18	V_{DD}	Power	LDO/Supply voltage input
19	GND2	Ground	Ground 2
20	I_{BIAS}	Input	Bias resistor connection
21	I_R	Input	Red LED current set resistor
22	I_G	Input	Green LED current set resistor
23	I_B	Input	Blue LED current set resistor
24	NRST	Logic Input	Low active reset input pin. (Internal pull down 1 MΩ)

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN} Pin: Voltage to GND	−0.3V to +6.0V
Voltage on R1, G1, B1, R2, G2, B2 Pins	−0.3V to P_{OUT} + 0.3V, with 6.0V max
Voltage on All Other Pins	−0.3V to V_{IN} +0.3V, with 6.0V max
Continuous Power Dissipation (Note 3)	Internally Limited
Junction Temperature (T_{J-MAX})	150˚C
Storage Temperature Range	−65˚C to +150˚C
Maximum Lead Temperature (Soldering)	(Note 4)

ESD Rating (Note 5)

Human Body Model:	2.0 kV
Machine Model:	200V

Operating Ratings (Notes 1, 2)

Input Voltage Range	3.0V to 5.0V
V_{DD} Voltage Range	2.69V to 2.87V
Recommended Load Current	0 mA to 120 mA
Junction Temperature (T_J) Range	−30˚C to +105˚C
Ambient Temperature (T_A) Range (Note 6)	−30˚C to +85˚C

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), LLP24 Package (Notes 6, 7)	∼34˚C/W

Electrical Characteristics (Notes 2, 8)

Limits in standard typeface are for T_J = +25˚C. Limits in **boldface** type apply over the operating junction temperature range (−30˚C ≤ T_A ≤ +105˚C). Unless otherwise noted, specifications apply to the LP3942 Typical Application Circuit (pg. 1) with: V_{VDD} = 2.78V, V_{IN} 3.6V, C_{IN} = 2.2 µF, C_1 = 1.0 µF, C_2 = 1.0 µF, C_{OUT} = 3.0 µF, R_{BIAS} = 27k. (Note 9).

Symbol	Parameter	Condition	Min	Typ	Max	Units
CHARGE PUMP 1.5x MODE						
V_{POUT}	Output Voltage	3.4V < V_{IN} < 5.0V, I_{OUT} ≤ 120 mA		4.5		V
		3.0V < V_{IN} < 3.4V		($1.5xV_{IN}$) − (I_{OUT} x R_{OUT})		
	Accuracy (Note 10)	3.4V < V_{IN} < 5.0V, I_{OUT} ≤ 120 mA		±3	**±5**	%
R_{OUT}	Output Resistance	V_{DD} = 3.0V		5	**7**	Ω
G_{CP}	Charge Pump Gain			1.5		
CHARGE PUMP 2x MODE						
V_{POUT}	Output Voltage (Note 10)	3.20V < V_{IN} < 5.0V, I_{OUT} ≤ 120 mA	**4.75**	5.0 ±3	**5.25** **±5**	V %
		3.0V < V_{IN} < 3.2V, I_{OUT} ≤ 80 mA	**4.75**	5.0 ±3	**5.25** **±5**	V %
R_{OUT}	Output Resistance	V_{DD} = 3.0V		5		Ω
G_{CP}	Charge Pump Gain			2		

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_Q(V_{IN})$	Operating Quiescent Current	$I_{(OUT)}$ = 0A (Note 11)		1.0	3.0	mA
$I_Q(V_{DD})$	Operating Quiescent Current			200	300	µA
$I_{SD}(V_{IN})$	Standby Quiescent Current	NSTBY = 0 NRST pin current excluded		4	**10**	µA
$I_{SD}(V_{DD})$	Standby Quiescent Current	NSTBY = 0, SPI interface inputs at 0V or 1.8V NRST pin current excluded		0.5	**2**	µA
f_{sw}	Switching Frequency	R_{BIAS} = 27 kΩ ± 1%	**500**	625	**750**	kHz
t_{start}	Startup Time	After writing '1' to NSTBY AND CP_ON. NRST must be '1'.		1	**2**	ms
T_{SHD}	Shutdown Threshold. Hysteresis			160 20		˚C ˚C

Logic Interface Characteristics (1.8V Logic)

Symbol	Parameter	Conditions	Limit			Units
			Min	Typ	Max	
LOGIC INPUTS						
V_{IL}	Input Low Level	SS, SI, SCK, NRST			0.5	V
V_{IH}	Input High Level	SS, SI, SCK, NRST	1.2			V
I_H	Logic Input Current	SS, SI, SCK	**–1**		**1**	µA
		NRST (1 MΩ pull-down)	**–1**		**3**	µA
f_{SPI}	Interface Clock				**10**	MHz
t_{NRST}	Reset Pulse Width	NRST	50			µs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pins.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160˚C (typ.) and disengages at T_J = 140˚C (typ.).

Note 4: For detailed soldering specifications and information, please refer to National Semiconductor Application Note 1187: Leadless Leadframe Package (LLP).

Note 5: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Note 6: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 105˚C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Note 7: Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102 mm x 76 mm x 1.6 mm with a 2x1 array of thermal vias. The ground plane on the board is 50 mm x 50 mm. Thickness of copper layers are 36 µm/18 µm/18 µm/36 µm (1.5 oz/1 oz/1 oz/1.5 oz). Ambient temperature in simulation is 22˚C, still air. Power dissipation is 1W.

The value of θ_{JA} of the LP3942 in LLP-24 could vary widely, depending on PWB material, layout, and environmental conditions. In applications where high maximum power dissipation exists (high V_{IN}, high I_{OUT}), special care must be paid to thermal dissipation issues. For more information on these topics, please refer to **Application Note 1187: Leadless Leadframe Package (LLP)** and the *Power Efficiency and Power Dissipation* section of this datasheet.

Note 8: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 9: C_{IN}, C_{OUT}, C1, and C2 : Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics. Minimum capacitance value for C_{IN}, C_1, and C_2 capacitors is 70% of nominal value. This tolerance includes manufacturing tolerance, temperature coefficient and voltage dependency (roll-off). C_{OUT} minimum effective capacitance value is 3.0 µF.

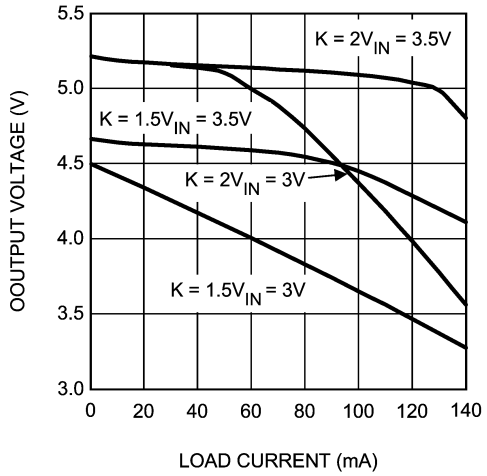
Note 10: Output voltage accuracy does not include V_{DD} (2.78V supply voltage) tolerance.

Note 11: The quiescent current does not include the current setting resistors' current.

Typical Performance Characteristics

Unless otherwise specified V_{VDD} = 2.78V, V_{IN} = 3.5V, C_{IN} = 2.2 µF, C_1 = 1.0 µF, C_2 = 1.0 µF, C_{OUT} = 3.3 µF, R_{BIAS} = 27k.

Charge Pump Voltage vs Load Current



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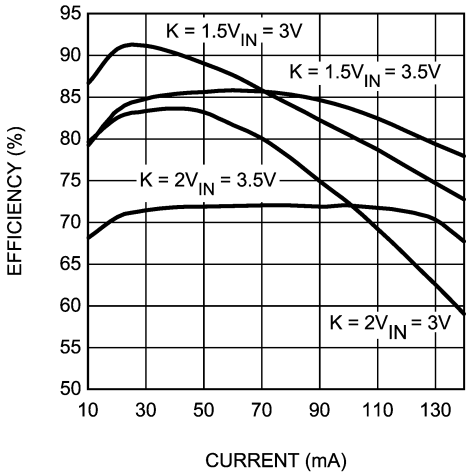
Charge Pump Efficiency vs Load Current



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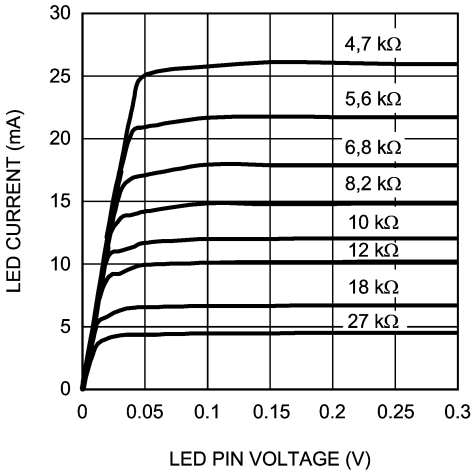
LED Current vs Output Pin Voltage



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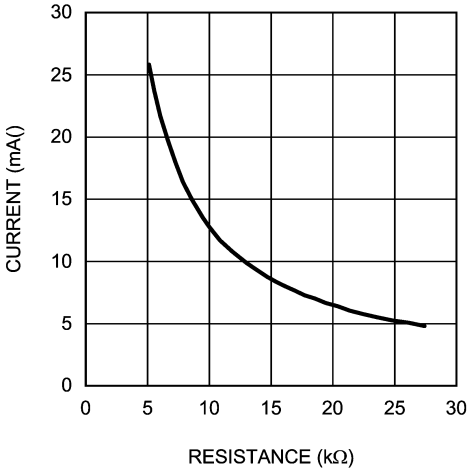
LED Current vs Set Resistance



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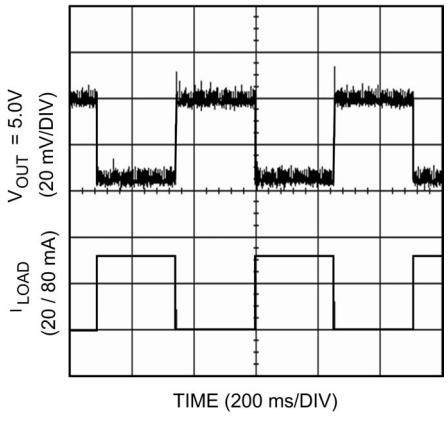
Charge Pump Load Regulation



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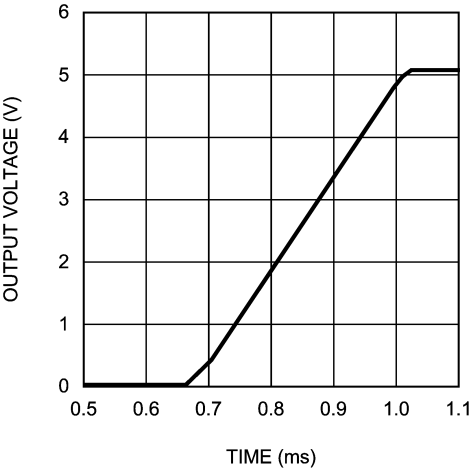
Charge Pump Startup



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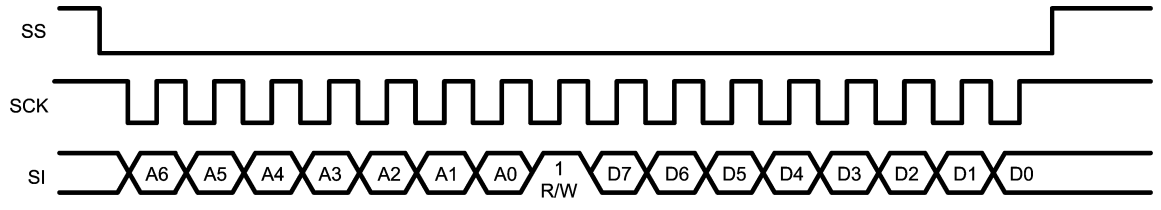
SPI Interface

LP3942 is compatible with SPI serial bus specification and it operates as a write-only slave. One write cycle consists of 7 Address bits, 1 Read/Write (RW, always high) bit and 8 Data bits. The Address and Data are transmitted MSB first.

The Slave Select signal SS must be low during the Cycle transmission. SS resets the interface when high and it has to be taken high between successive Cycles. Data is clocked in on the rising edge of the SCK clock signal.



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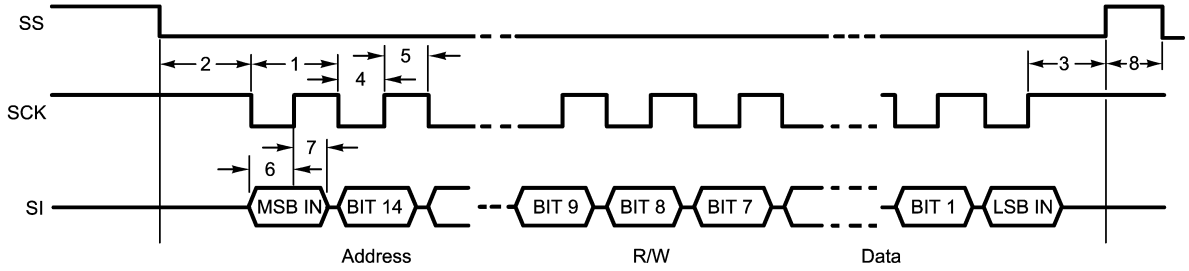
SPI Write Cycle



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SPI Timing Diagram

SPI TIMING PARAMETERS

Symbol	Parameter	Limit		Units
		Min	Max	
1	Cycle Time	80	-	ns
2	Enable Lead Time	5	-	ns
3	Enable Lag Time	5	-	ns
4	Clock Low Time	35	-	ns
5	Clock High Time	35	-	ns
6	Data Setup Time	15	-	ns
7	Data Hold Time	10	-	ns
8	SS Inactive Time	40	-	ns

Charge Pump Mode Selection

Charge pump mode is controlled through the SPI interface. The mode selection is shown in the following tables.

Addr.	Reg.	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
02'h	**CTRL**	**NSTBY**	**CP_ON**	CC/SW2	CC/SW1	**1.5x/2x**	reserved	reserved	reserved
	default	0	0	0	0	0	0	0	0

Control Bit	Parameter	State	Function
NSTBY	Low Active Standby	NSTBY = 0	LP3942 is disabled
		NSTBY = 1	LP3942 is active
CP_ON	Charge Pump Enable	CP_ON = 0	Charge Pump is disabled
		CP_ON = 1	Charge Pump is active
1.5x/2x	Charge Pump Mode 1.5x/2x	1.5x/2x = 0	1.5x mode, V_{OUT} = 4.5V
		1.5x/2x = 1	2x mode, V_{OUT} = 5V

If charge pump is disabled (CP_ON = 0) and LP3942 is active (NSTBY = 1), then charge pump output (P_{OUT}) pin must be connected externally to the same supply voltage (max 5.0V) which is used to drive LEDs with RGB1 or RGB2 outputs.

Start-Up Sequence of LP3942

The LP3942 start-up sequence can be triggered in the following way: V_{DD} power is connected to the device and NRST pin is '0' (or floating) and NSTBY is set to '1' via SPI.

The LP3942 activates first internal oscillator and waits for appr. 0.8 ms. Then, if CP_ON bit is set to '1', LP3942 enables internal soft-start circuitry to start-up the charge pump smoothly. Soft-start sequence takes appr. 200 µs. After this start-up sequence, P_{OUT} is settled to correct value and RGB outputs can be enabled via SPI.

Modes of Operation

RESET: In the RESET mode all the internal registers are reset to the default values. Reset is entered always if input NRST is LOW or internal Power On Reset is active.

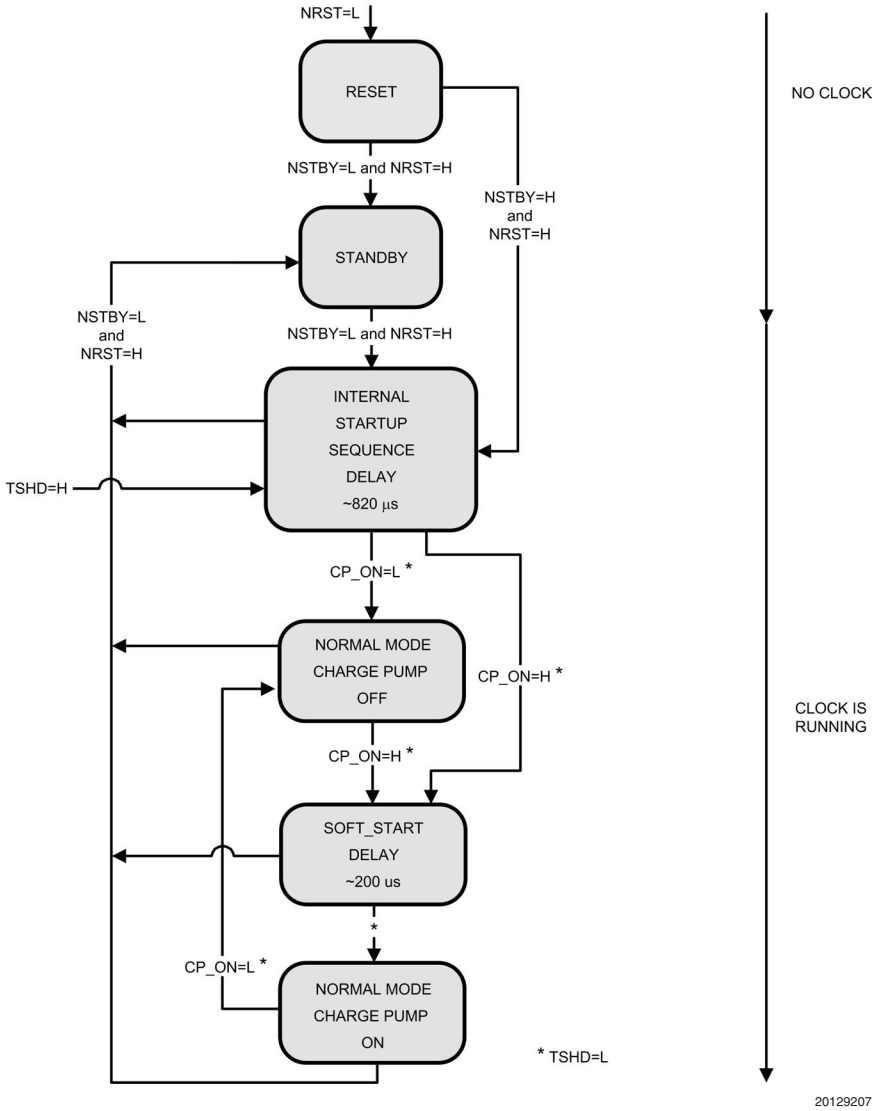
STANDBY: The STANDBY mode is entered if the register bit NSTBY is HIGH and Reset is not active. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode and the control bits are effective immediately after power up.

STARTUP: INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks. To ensure the correct oscillator initialization, a 0.8 ms delay is generated by the internal state-machine. Thermal shutdown (T_{SHD}) stops the chip operation and Startup mode is entered. Normal mode is entered after the device has cooled down.

NORMAL/CP OFF During NORMAL MODE WITH CHARGE PUMP OFF all LED controls can be used but the charge pump is not active.

NORMAL/CP ON In NORMAL MODE WITH CHARGE PUMP ON all the chip functions are active.

Internal Start-Up Sequence



RGB Driver Electrical Characteristics

Limits in standard typeface are for T_J = +25˚C. Limits in **boldface** type apply over the full operating junction temperature range (−30˚C ≤ T_J ≤ +105˚C). Unless otherwise noted, specifications apply to the LP3942 Typical Application Circuit (pg. 1) with: V_{VDD} = 2.78V, V_{IN} = 3.6V, C_{IN} = 2.2 µF, C_1 = 1.0 µF, C_2 = 1.0 µF, C_{OUT} = 3.0 µF, R_{BIAS} = 27k. (Note 9).

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{Leakage}$	R1/2, G1/2, B1/2 Pin Leakage Current	V_{RGB} = 5V			**1**	µA
$I_{MAX(RGB)}$	Maximum Sink Current	Constant Current Mode: Limited with external Rr, Rg, Rb resistors by user 3.20V < V_{IN} < 5.0V			40	mA
		Constant Current Mode: 3.0 < V_{IN} < 3.2V			30	mA
		Switch Mode: Limited with ballast resistors by user			50	mA
	Accuracy @ 20 mA	V_{DD} = 2.78V V_{RGB} = 0.2V	−10	±3	10	%
	Current Mirror Ratio			1:100		
	RGB1 and RGB2 Mismatch	20 mA LED Current		±5		%
R_{RGB}		Switch mode		2	3.5	Ω
f_{RGB}	RGB Switching Frequency	Accuracy proportional to internal clock freq.	15	20	26	kHz

RGB1 and RGB2 Output Description

RGB1 and RGB2 outputs can be used in two modes: constant current and switch modes. There are few basic parameters in the RGB1 and RGB2 outputs, which can cause lowered output current values and/or extra current mismatch, if not considered carefully in application. This chapter helps to do this analysis.

CONSTANT CURRENT MODE

Outputs can be understood as Ideal current sources with certain output resistance Rds. Additionally, outputs have a minimum voltage Vsat, which must be exceeded at the output. If voltage limit is not reached, the ideal current source's current will be less than expected. Taking as an example the R1 output and defining the voltage between R1 pin and GND3 pin to Vr, and defining the ideal output current as Ir, one can estimate the true output current with following simple formula: Ireal ∼ Ir + (Vr / Rds). This is true only, if Vr > Vsat. In the LP3942, the nominal value for Rds is 10 kΩ, and for Vsat is 200 mV.

For example, if we have a LED that has 3.0V forward bias voltage at 10 mA and we have set the LED current to 10 mA. Then we can estimate the true LED current to be appr. 10 mA + ((4.5V-3.0V) / 10 kΩ) = 10.15 mA. And voltage on RGB output pin is 1.5V, which is high enough for the constant current generator. Note that this example does not consider the worst case tolerance of output current which results from tolerance of external bias resistor and current mismatch in the LP3942.

SWITCH MODE

In switch mode the function is more straightforward. Designer needs to only consider the output resistance of the switch, which is typically 2Ω.

Using now the case from previous example and setting the LED current with an external ballast resistor of 150Ω. Now, we get true output current of 1.5V/(150 + 2)∼ 9.9 mA. Note that this example does not consider the worst case tolerance of output current which results from tolerance of POUT voltage and LED forward voltage.

RGB Functionality

Both RGB outputs RGB1 and RGB2 have separate control for mode, brightness and color. The RGB LEDs are controlled through the SPI interface. The control register table is shown below.

Addr.	Reg.	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
00'h	**RGB1**	**Color[3]**	**Color[2]**	**Color[1]**	**Color[0]**	**Bright[2]**	**Bright[1]**	**Bright[0]**	**Enable1**
	default	0	0	0	0	0	0	0	0
01'h	**RGB2**	**Color[3]**	**Color[2]**	**Color[1]**	**Color[0]**	**Bright[2]**	**Bright[1]**	**Bright[0]**	**Enable2**
	default	0	0	0	0	0	0	0	0
02'h	**CTRL**	**NSTBY**	**CP_ON**	**CC/SW2**	**CC/SW1**	**1.5x/2x**	**reserved**	**reserved**	**reserved**
	default	0	0	0	0	0	0	0	0
03'h	**OVL**	**Overlap2**	**R2SW**	**G2SW**	**B2SW**	**Overlap1**	**R1SW**	**G1SW**	**B1SW**
	default	0	0	0	0	0	0	0	0

Enable1 and **Enable2** bits are used to enable RGB1 and RGB2 outputs.

OVL register can be used, if overlapping mode is needed, default mode is non-overlapping. If overlapping mode is

RGB Functionality (Continued)

needed, then **Overlap1** and/or **Overlap2** bits are written to '1'. Switch enable bits **G1SW**, **R1SW** and **B1SW** bits need to be written to '1' if corresponding RGB1 output is to be activated. The switch enable bits **G2SW**, **R2SW** and **B2SW** have same effect to RGB2 outputs. Switch enable bits have effect only in overlapping mode.

Following chapters describe RGB functionality and modes in more details.

MODES OF OPERATION

Constant Current/Switch Mode

The LEDs are driven either by constant current sink or switches.

By using constant current mode the LED current is limited based on external resistors Rr, Rg and Rb connected to pins IR, IG and IB. Only one RGB LED per output is recommended in this mode.

The LED currents can be adjusted with resistors based on the following table.

RR or RG or RB [Ω]	Typical I_{LED} [mA]
5.6k	22.0
6.8k	18.1
8.2k	15.0
10k	12.3
12k	10.3
15k	8.2
18k	6.8

The switch mode uses constant current mirrors as low ohmic switches. Switch mode requires an external ballast resistor to limit the LED current. This mode is used if 2 or more RGBs are connected in parallel. To prevent the current variation due output voltage accuracy it is recommended to use charge pump in double (2x) mode.

The mode selection is shown on the following table.

CC/SW(1/2)	Mode	Comment
0	Constant Current Mode	LEDs are driven with constant current sinks. Maximum current is limited by Rr, Rg and Rb
1	Switch Mode	LEDs are driven with switches. Maximum current is limited by ballast resistors.

Overlapping/Non-Overlapping Mode

This mode control defines how the RGBs are controlled by PWM timing logic. Overlapping mode turns on and off the RGBs at the same time. Non-overlapping mode splits the R, G and B to phases based on selected color and thus limits the maximum output current through the RGB LED.

The selection for this mode is as follows.

Overlap(1/2)	Mode	Comment
0	Non-overlapping Mode	LEDs are driven with non-overlapping method to minimize the noise and current consumption. Frame based color control is enabled.
1	Overlapping Mode	LEDs are driven with overlapping method. Maximum current consumption is 6*Imax. Color control is disabled.

Overlapping Mode

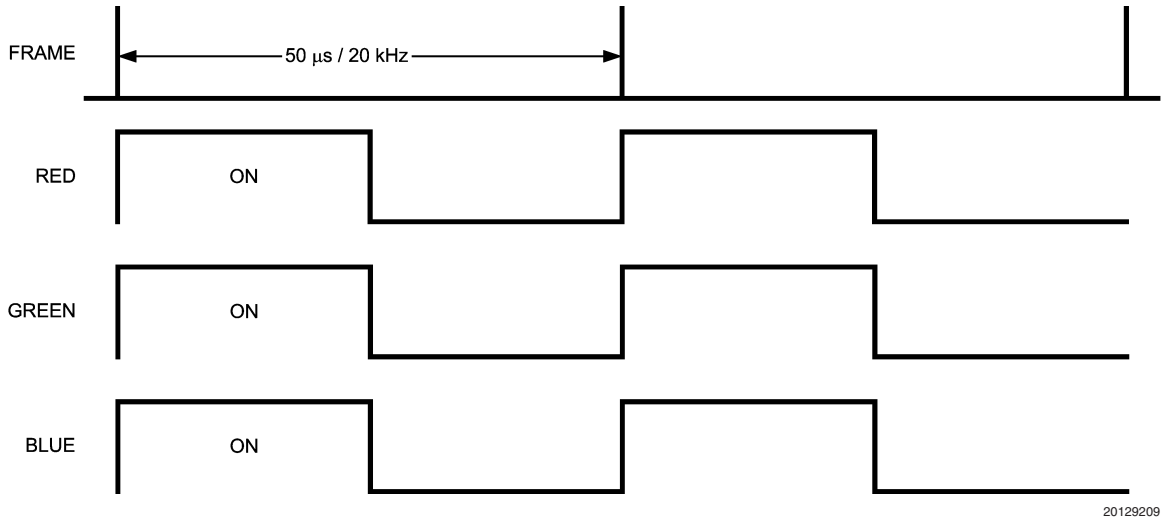
Since RGB outputs are on simultaneously, the maximum load peak current is

$$I_{MAX} = I(R1)_{MAX} + I(G1)_{MAX} + I(B1)_{MAX} + I(R2)_{MAX} + I(G2)_{MAX} + I(B2)_{MAX} .$$

Overlapping Mode Timing Diagram

The brightness is controlled using PWM duty cycle based control method as the following figure shows.

RGB Functionality (Continued)



RGB Framing with 50% Intensity

The brightness control is logarithmic and is programmed as follows.

Bright [2:0]	Color Brightness [%]	Ratio to Max Brightness
000	0	0
001	1.56	1/64
010	3.12	1/32
011	6.25	1/16
100	12.5	1/8
101	25.0	1/4
110	50.0	1/2
111	100	1/1

Non-Overlapping Mode

The non-overlapping mode has 16-programmed colors (different R, G and B ratio → different color). Since the R, G and B are split in to non-overlapping slots the output current through the RGB LED can be calculated by following equation:

$$I_{AVG} = (C_R * I_R + C_G * I_G + C_B * I_B) * B,$$

C = Color [%] (see table below)

B = Brightness [%] (see table below)

The 16 colors can be selected as follows. Please note that exact color depends on LED current and type.

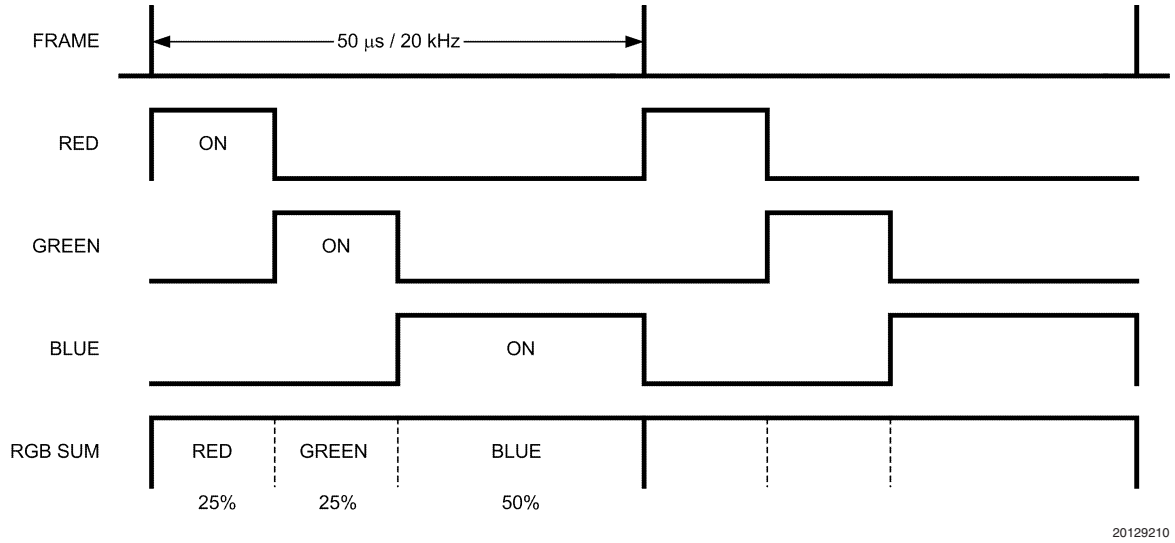
Color[3:0]	Red active/cycle [%]	Green active/cycle [%]	Blue active/cycle [%]	RGB Color (depends on RGB LED type)
0000	100	0	0	red
0001	0	100	0	green
0010	0	0	100	blue
0011	50	50	0	yellow
0100	0	50	50	green/blue
0101	50	0	50	maroon
0110	33	33	33	white
0111	50	25	25	dark pink
1000	25	50	25	dark green
1001	25	25	50	lt blue
1010	75	25	0	lt orange
1011	75	0	25	orange
1100	0	75	25	lt green
1101	25	75	0	med green
1110	0	25	75	blue/green
1111	25	0	75	purple

RGB Functionality (Continued)

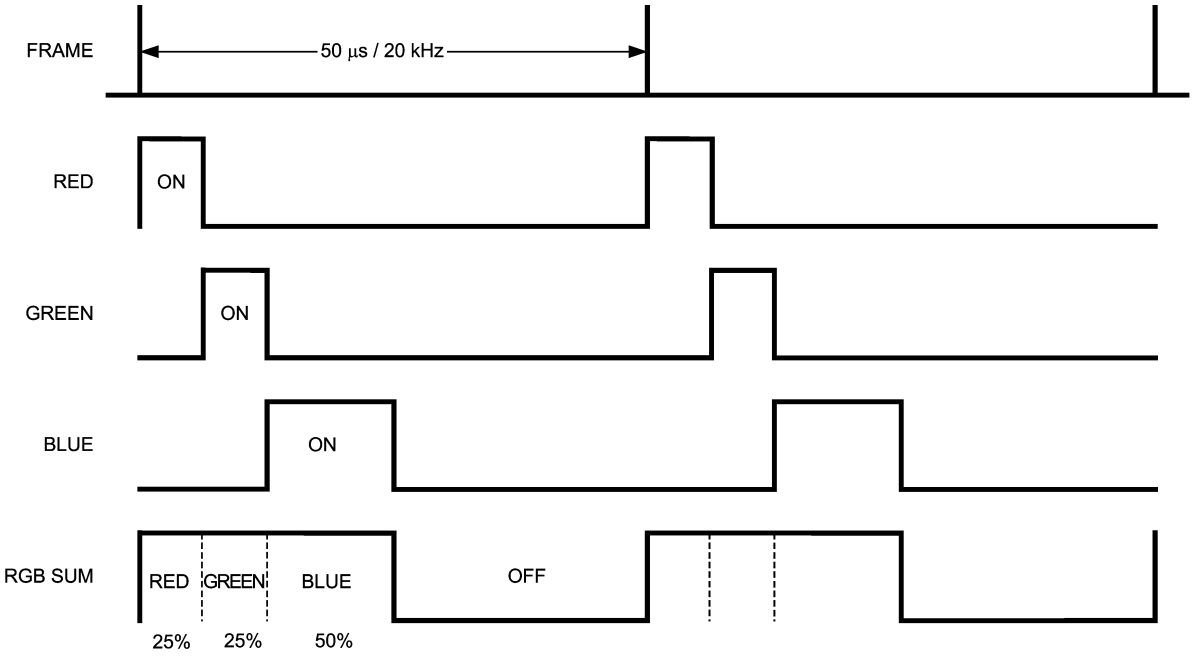
The same logarithmic brightness control is used in both modes.

Non-Overlapping Timing Diagram

The timing diagram shows the splitted R, G and B and brightness control effect to splitted parts.



RGB Framing with Full Intensity



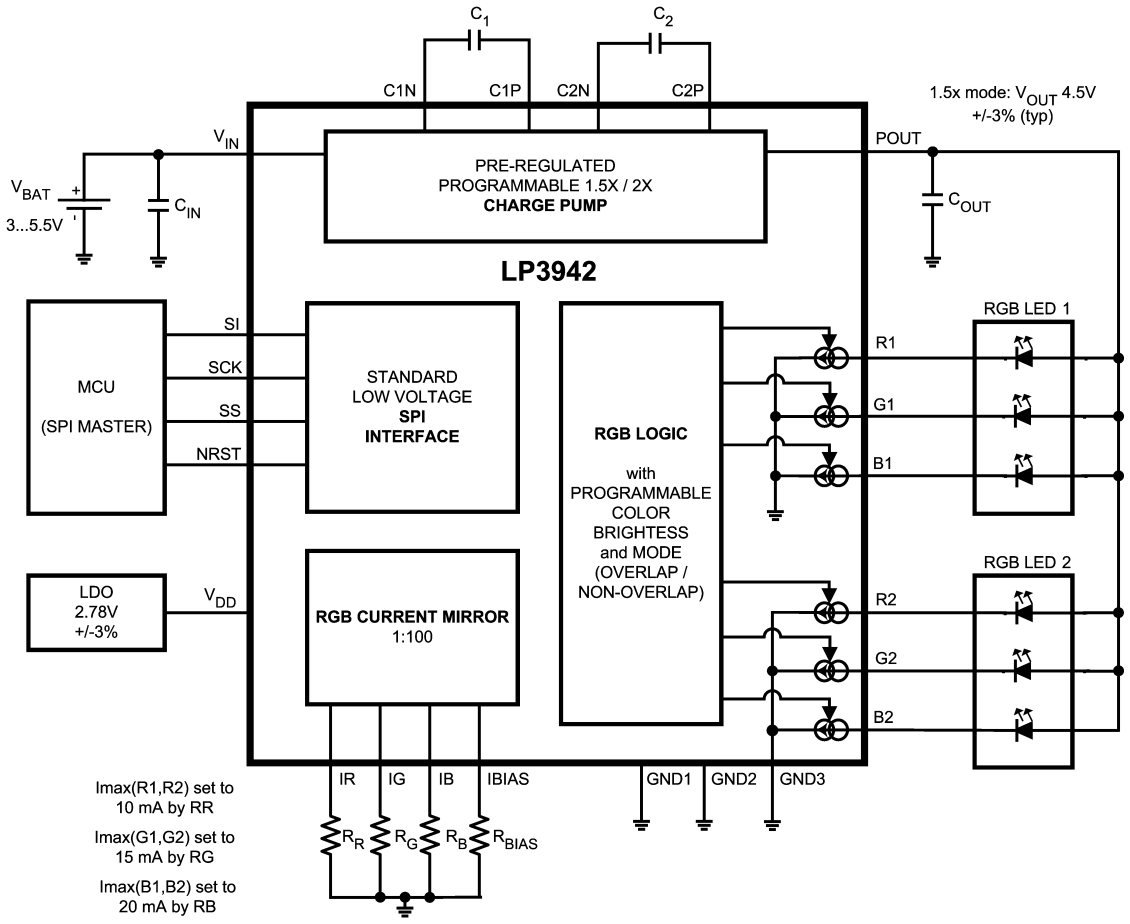
RGB Framing with 50% Intensity

Application Information

The following examples describe 4 different ways to use LP3942 to drive different LEDs (2 RGBs, 4 RGBs, 6 Blue LEDs)

Example 1: Normal Use – 2 RGBs

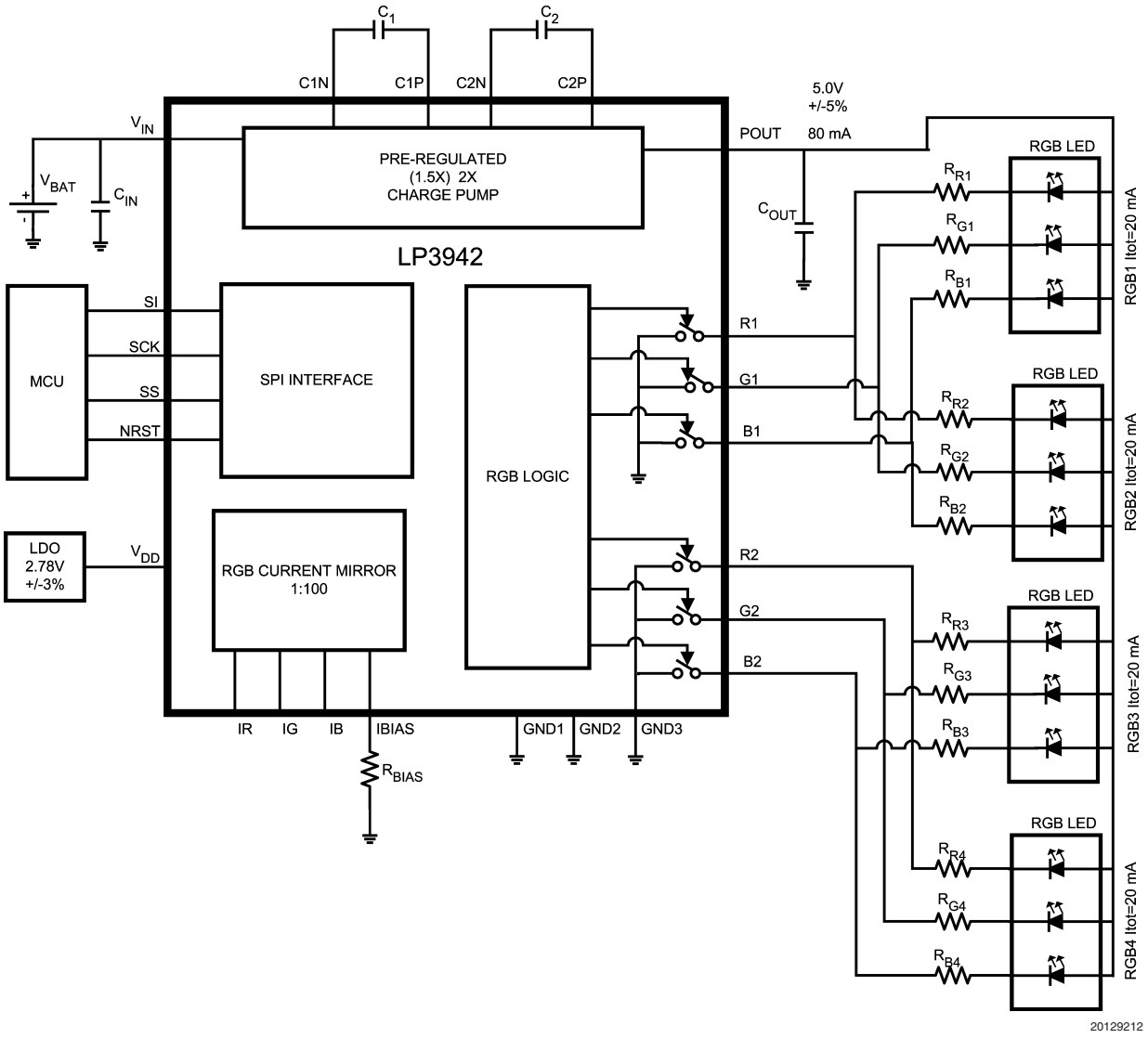
- Charge pump in 1.5x mode, V_{OUT} = 4.5V
- Non overlapping constant current mode in use
- RGB1 and RGB2 have different control
- Imax(R1, R2) limited to 10 mA by RR
- Imax(G1, G2) limited to 15 mA by RG
- Imax(B1, B2) limited to 20 mA by RB
- Framing → I_{LOAD}(max) = 40 mA → low noise to input.
- See Electrical Characteristics for output voltage and current specifications in different conditions



Application Information (Continued)

Example 2: 2+2 RGB LEDs in parallel

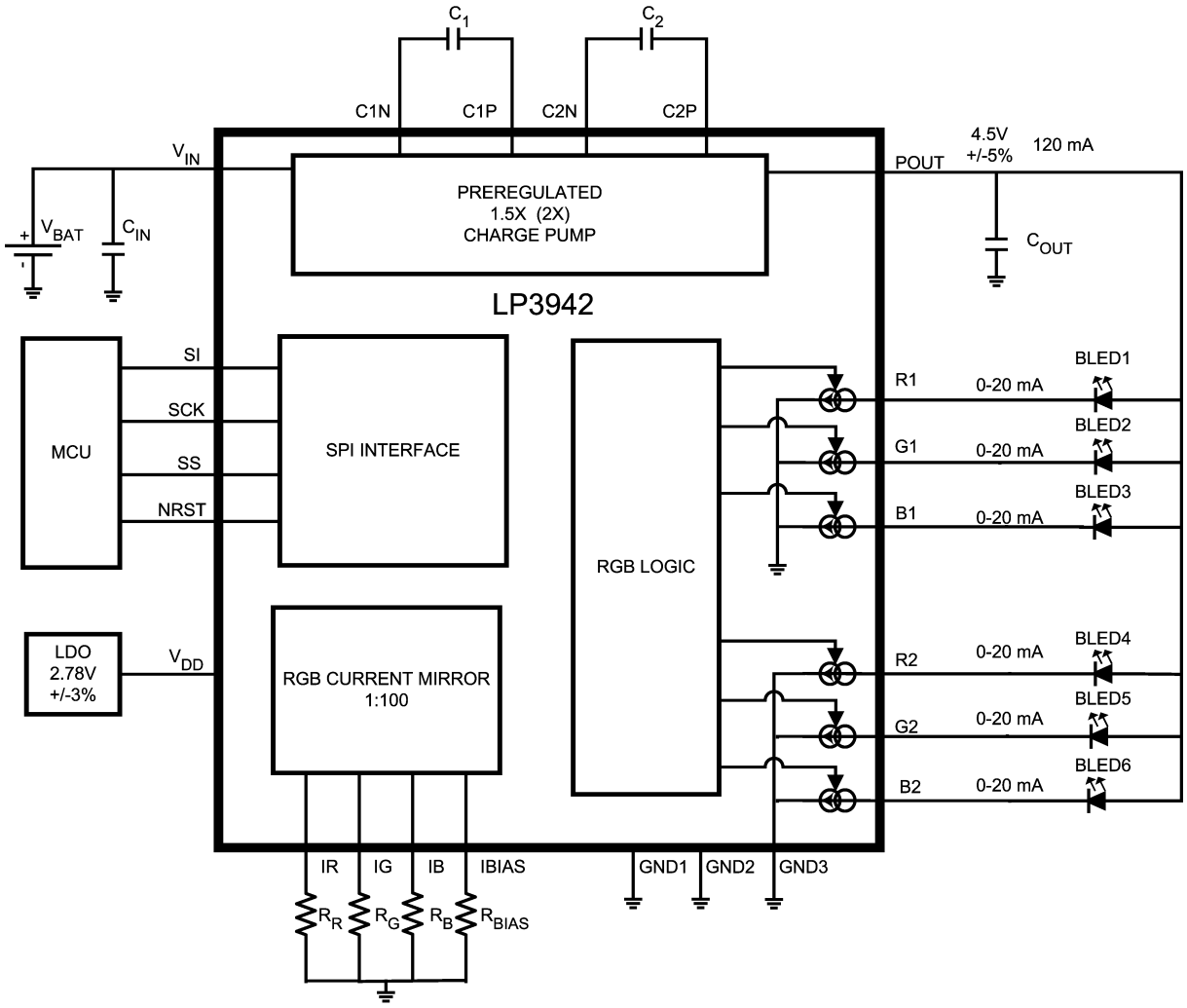
- Maximum current limited by ballast resistors
- I(LED) accuracy improved by using higher V_{OUT} voltage → Charge pump operates on 2x mode → V_{OUT} = 5.0V
- Non overlapping switch mode in use
- RGB1 and RGB2 have same control
- RGB3 and RGB4 have same control
- See Electrical Characteristics for output voltage and current specifications in different conditions



Application Information (Continued)

Example 3: 6 Blue LEDs in parallel (1), I(LED) ∿0-20 mA

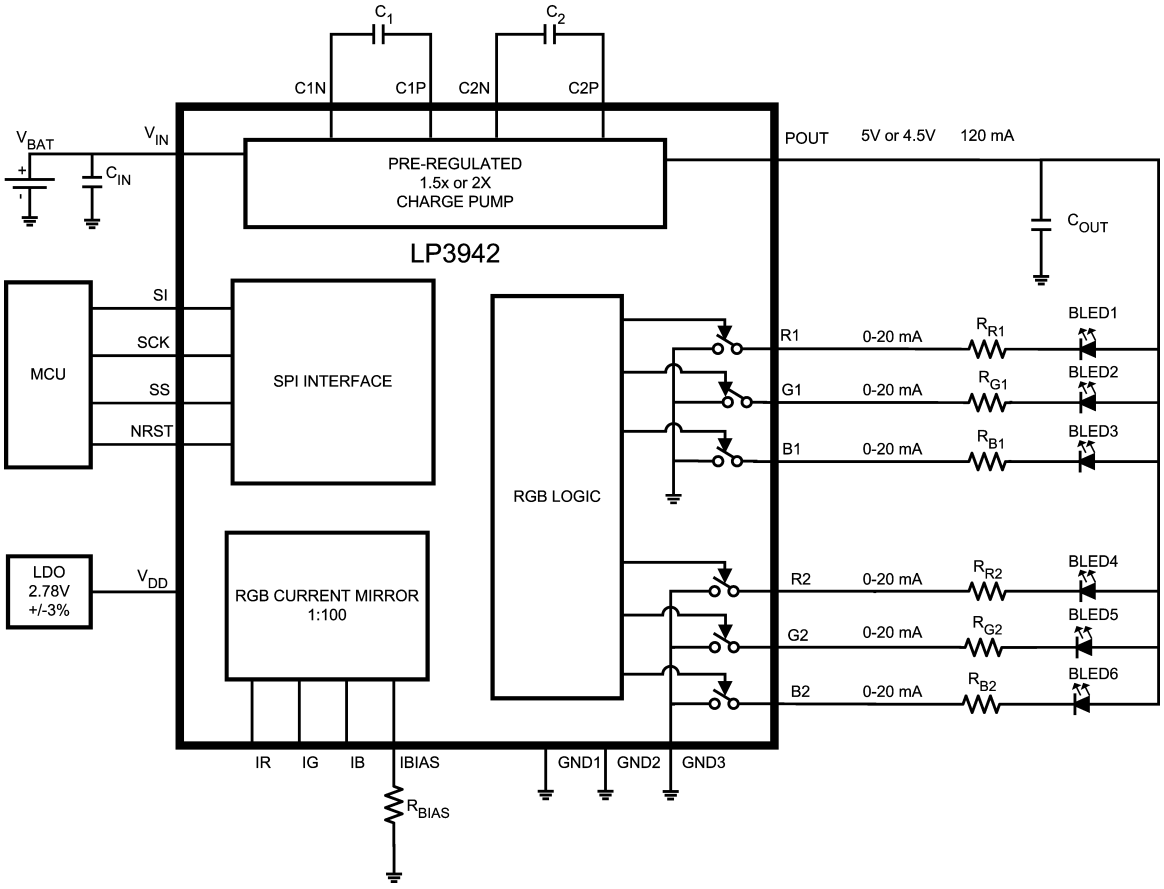
- Maximum current limited by constant current sinks and external resistor
- Charge pump in 1.5x mode. Brightness adjustment by programming (PWM type)
- 3 external resistors are required to set the current.
- Overlapping constant current mode in use
- See Electrical Characteristics for output voltage and current specifications in different conditions



Application Information (Continued)

Example 4: 6 Blue LEDs in parallel (2), I(LED) ∼0-20 mA

- Maximum current limited by ballast resistors (6)
- 1.5x or 2x mode can be used depending on application. If higher I(LED) accuracy is required then 2x mode is recommended.
- Brightness adjustment by programming
- Overlapping switch mode in use
- See Electrical Characteristics for output voltage and current specifications in different conditions



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Charge Pump Operational Description

OVERVIEW

The LP3942 includes a regulated switched-capacitor charge pump with two programmable voltage multiplications, 1.5 and 2.

On 1.5x mode by combining the principles of a switched-capacitor charge pump and a linear regulator, it generates a regulated 4.5V output from Li-Ion input voltage range. A two-phase internally generated non-overlapping clock controls the operation of the charge pump. During the charge phase (ø1), both flying capacitors (C1 and C2) are charged from input voltage. In the pump phase that follows (ø2), the flying capacitors are discharged to output. A traditional switched capacitor charge pump operating in this manner will use switches with very low on-resistance, ideally 0Ω, to generate an output voltage that is 1.5x the input voltage. The LP3942 regulates the output voltage by controlling the resistance of the input-connected pass-transistor switches in the charge pump. On 2x mode the output is regulated to 5.0V thus enabling the higher output voltage for driving parallel connected RGBs with lower current variation on RGB switch mode.

PRE-REGULATION

The low input current ripple of the LP3942, resulting from internal pre-regulation, adds very little noise to the input line. Regulation is achieved by modulating the on-resistance of the switches connected to the input pin. The regulation is done before the voltage multiplication, giving rise to the term "pre-regulation". It is pre-regulation that eliminates most of the input current ripple that is a typical and undesirable characteristic of a many switched capacitor converters. V_{DD} is used as the regulator reference voltage. Any change in V_{DD} value is reflected to V_{OUT}.

INPUT, OUTPUT, AND GROUND CONNECTIONS

Making good input, output, and ground connections is essential to achieve optimal LP3942 performance. It is strongly recommended that the input capacitor (C_{IN}) be placed as close as possible to the LP3942, so that the trace from the input pin (V_{IN}) is as short and straight as possible. It is recommended that the input capacitor (C_{IN}) is placed on the same side of the PCB as LP3942, and that traces remain on this side of the board as well (vias to traces on other PCB layers are not recommended between the input capacitor and LP3942 input pad). It is recommended that the output capacitor (C_{OUT}) be placed as close to the LP3942 output pad (P_{OUT}) as possible. It is best if routing of output pad trace follows guidelines similar to those presented for the input pad (V_{IN}) and capacitor (C_{IN}). The flying capacitors (C1 and C2) should also be placed as close to the LP3942 as possible to minimize PCB trace length between the capacitor and the IC.

The following pads of the LP3942 are ground connections and must be connected externally: pads GND1, GND2, GND3 and the die-attach pad (DAP). Large, low impedance copper fills and via connections to an internal ground plane are the preferred way of connecting together the ground pads of the LP3942, the input capacitor, and the output capacitor, as well as connecting this circuit ground to the system ground of the PCB.

RESET AND STANDBY

When the voltage on the NRST pin is high, the LP3942 will be in reset mode. After NRST goes low, the LP3942 goes to default mode, which is Standby. All internal registers in LP3942 are set to default state in reset mode. There is a 1 MΩ pull-down resistor tied between the NRST pin and ground that pulls the NRST pin voltage low if the pin is not driven by a voltage source. When pulling the part out of reset mode, the voltage source connected to the NRST pin must be able to drive the current required by the 1 MΩ resistor.

SOFT START

The LP3942 employs soft start circuitry to prevent excessive input inrush currents during startup. The output voltage is programmed to rise from 0V to the nominal output voltage (4.5V or 5.0V) in 200 µs (typ). Soft-start is engaged after the specified start-up delay (0.8 ms typically) after a part, with input voltage established, is taken out of standby by writing NSTBY and CP_ON bits to '1'. Start-up delay and soft-start will also engage always when CP_ON bit is written to '1' or when device recovers from thermal shutdown mode.

OUTPUT CURRENT CAPABILITY

In 1.5x mode the LP3942 is guaranteed to provide 120 mA of output current at specified output voltage when the input voltage is within 3.4V-to-5.0V. LP3942 can provide 120 mA current also from lower input voltage (down to 3.0V) but then output voltage will be degraded due to effective output resistance (R_{OUT}) of the charge pump. The expected voltage drop can be calculated by using a simple model for the charge pump depicted in *Figure 1*.

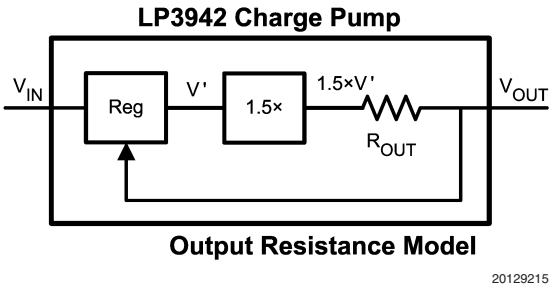


FIGURE 1. Charge Pump Output Resistance Model

The model shows a linear pre-regulation block (Reg), a voltage multiplier (1.5x), and an output resistance (R_{OUT}). Output resistance models the output voltage droop that is inherent to switched capacitor converters. The output resistance of the LP3942 is 5Ω (typ), and is function of switching frequency, flying capacitors, internal resistances of switches and ESR of capacitors. When the output voltage is in regulation, the regulator in the model controls the voltage V' to keep the output voltage equal to 4.5V (typ). With increased output current, the voltage drop across R_{OUT} increases. To prevent droop in output voltage, the voltage drop across the regulator is reduced, V' increases, and V_{OUT} remains at 4.5V. When the output current increases to the point that there is zero voltage drop across the regulator, V' equals the input voltage, and the output voltage is "on the edge" of regulation. Additional output current causes the output voltage to fall out of regulation, and the LP3942 operation is similar to a basic open-loop 1.5x charge pump. In this mode, output current results in output voltage drop proportional to the output resistance of the charge pump. The out-of-

Charge Pump Operational Description (Continued)

regulation LP3942 output voltage can be approximated by: V_{OUT}= 1.5 x V_{IN} – I_{OUT} x R_{OUT}. Again, this equation only applies at low input voltage and high output current where the LP3942 is not regulating. See *Output Current vs. Output Voltage* curves in the **Typical Performance Characteristics** section for more details.

On 2x mode the functionality is similar, only the output voltage is set to 5.0V and out-of-regulation output voltage can be estimated by: V_{OUT} = 2.0 x V_{IN} – I_{OUT} x R_{OUT}. Output resistance is approximately same as in 1.5x mode.

THERMAL SHUTDOWN

The LP3942 implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 160˚C (typ), the part switches into Startup mode. The LP3942 releases thermal shutdown when the junction temperature of the part is reduced to 140˚C (typ). Thermal shutdown is most-often triggered by self-heating, which occurs when there is excessive power dissipation in the device and/or insufficient thermal dissipation. LP3942 power dissipation increases with increased output current and input voltage (see **Power Efficiency and Power Dissipation** section). Because of automatic recovery from thermal shutdown function, thermal cycling is the typical result. Thermal cycling is the repeating process where the part self-heats, enters thermal shutdown, cools, turns-on, and then heats up again to the thermal shutdown threshold. Thermal cycling is recognized by a pulsing output voltage and can be stopped be reducing the internal power dissipation (reduce input voltage and/or output current) or the ambient temperature.

If thermal cycling occurs under desired operating conditions, thermal dissipation performance must be improved to accommodate the power dissipation of the LP3942. Fortunately, the LLP package has excellent thermal properties that, when soldered to a PCB designed to aid thermal dissipation, allows the LP3942 to operate under very demanding power dissipation conditions.

OUTPUT CURRENT LIMITING

The LP3942 contains current limit circuitry that protects the device in the event of excessive output current and/or output shorts to ground. Current is limited to 300 mA (typ) when the output is shorted directly to ground. When the LP3942 is current limiting, power dissipation in the device is likely to be quite high. In this event, thermal cycling should be expected (See **Thermal Shutdown** section).

Charge Pump Application Information

OUTPUT VOLTAGE RIPPLE

The amount of voltage ripple on the output of the LP3942 is highly dependent on the application conditions: output current and the output capacitor, specifically. A simple approximation of output ripple is determined by calculating the amount of voltage droop that occurs when the output of the LP3942 is not being driven. This occurs during the charge phase (Φ1). During this time, the load is driven solely by the charge on the output capacitor. The magnitude of the ripple thus follows the basic discharge equation for a capacitor (I = C x dV/dt), where discharge time is one-half the switching period, or 0.5/FSW. Put simply,

$$RIPPLE_{Peak\text{-}Peak} = \frac{I_{OUT}}{C_{OUT}} \times \frac{0.5}{F_{SW}}$$

A more thorough and accurate examination of factors that affect ripple requires including effects of phase non-overlap times and output capacitor equivalent series resistance (ESR). In order for the LP3942 to operate properly, the two phases of operation must never coincide. (If this were to happen all switches would be closed simultaneously, shorting input, output, and ground). Thus, non-overlap time is built into the clocks that control the phases. Since the output is not being driven during the non-overlap time, this time should be accounted for in calculating ripple. Actual output capacitor discharge time is approximately 60% of a switching period, or 0.6/FSW.

The ESR of the output capacitor also contributes to the output voltage ripple, as there is effectively an AC voltage drop across the ESR due to current switching in and out of the capacitor. The following equation is a more complete calculation of output ripple than presented previously, taking into account phase non-overlap time and capacitor ESR.

$$RIPPLE_{Peak-Peak} = \left(\frac{I_{OUT}}{C_{OUT}} \times \frac{0.6}{F_{SW}}\right) + \left(2 \times I_{OUT} \times ESR_{COUT}\right)$$

A low-ESR ceramic capacitor is recommended on the output to keep output voltage ripple low. Placing multiple capacitors in parallel can reduce ripple significantly, both by increasing capacitance and reducing ESR. When capacitors are in parallel, ESR is in parallel as well. The effective net ESR is determined according to the properties of parallel resistance. Two identical capacitors in parallel have twice the capacitance and half the ESR as compared to a single capacitor of the same make. On a similar note, if a large-value, high-ESR capacitor (tantalum, for example) is to be used as the primary output capacitor, the net output ESR can be significantly reduced by placing a low-ESR ceramic capacitor in parallel with this primary output capacitor.

CAPACITORS

The LP3942 requires 4 external capacitors for proper operation. Surface-mount multi-layer ceramic capacitors are highly recommended. These capacitors are small, inexpensive and have very low equivalent series resistance (≤ 10 mΩ. typ.). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors generally are *not* recommended for use with the LP3942 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LP3942. These capacitors have tight capacitance tolerance (as good as ±10%), hold their value over temperature (X7R: ±15% over –55˚C to +125˚C; X5R: ±15% over –55˚C to +85˚C), and typically have little voltage coefficient. Capacitors with Y5V and/or Z5U temperature characteristic are generally not recommended. These types of capacitors typically have wide capacitance tolerance (+80%, –20%), varies significantly over temperature (Y5V: +22%, –82% over –30˚C to +85˚C range; Z5U: +22%, –56% over +10˚C to +85˚C range), and has poor voltage coefficients. Under some conditions, a nominal 1 µF Y5V or Z5U capacitor could

Charge Pump Application Information (Continued)

have a capacitance of only 0.1 µF. Such detrimental deviation is likely to cause these Y5V and Z5U of capacitors to fail to meet the minimum capacitance requirements of the LP3942. The table below lists some leading ceramic capacitor manufacturers.

Manufacturer	Contact Information
TDK	www.component.tdk.com
AVX	www.avx.com
Murata	www.murata.com
Taiyo-Yuden	www.t-yuden.com
Vishay-Vitramon	www.vishay.com

INPUT CAPACITORS

The input capacitor (CIN) is used as a reservoir of charge, helping to quickly transfer charge to the flying capacitor during the charge phase (Φ1) of operation. The input capacitor helps to keep the input voltage from drooping at the start of the charge phase, when the flying capacitor is first connected to the input, and helps to filter noise on the input pin that could adversely affect sensitive internal analog circuitry biased off the input line. As mentioned above, an X7R/X5R ceramic capacitor is recommended for use.

For applications where the maximum load current required is between 60 mA and 120 mA, a minimum input capacitor of 2.2 µF is required. For applications where the maximum load current is 60 mA or less, 1.0 µF of input capacitor is sufficient. Failure to provide enough capacitance on the LP3942 input can result in poor part performance, often consisting of output voltage droop, excessive output voltage ripple and/or excessive input voltage ripple.

FLYING CAPACITOR (C1 and C2)

The flying capacitor (CFLY) transfers charge from the input to the output, providing the voltage boost of the charge pump. A polarized capacitor (tantalum, aluminum electrolytic, etc.) must not be used here, as the capacitor will be reverse-biased upon start-up of the LP3942. The size of the flying capacitor and its ESR affect output current capability when the input voltage of the LP3942 is low, most notable for input voltages below 3.4V. These issues were discussed previously in the **Output Current Capability** section. For most applications, a 1 µF X7R/X5R ceramic capacitor is recommended for the flying capacitor. When considering also voltage roll-off, minimum capacitance value of 700 nF should be available in all voltage conditions.

OUTPUT CAPACITOR

The output capacitor of the LP3942 plays an important part in determining the characteristics of the output signal of the LP3942, many of which have already been discussed. The ESR of the output capacitor affects charge pump output resistance, which plays a role in determining output current capability. Both output capacitance and ESR affect output voltage ripple. For these reasons, a low-ESR X7R/X5R ceramic capacitor is the capacitor of choice for the LP3942 output. In addition to these issues previously discussed, the output capacitor of the LP3942 also affects control-loop stability of the part. Instability typically results in the switching frequency effectively reducing by a factor of two, giving excessive output voltage droop and/or increased voltage ripple on the output and the input. Minimum output capacitance of 3.0 µF is required.

POWER EFFICIENCY AND POWER DISSIPATION ON 1.5x MODE

Efficiency of the LP3942 mirrors that of an unregulated switched capacitor converter followed by a linear regulator. The simplified power model of the LP3942, in *Figure 2*, will be used to discuss power efficiency and power dissipation. In calculating power efficiency, output power (P_{OUT}) is easily determined as the product of the output current and the 4.5V output voltage. Like output current, input voltage is an application-dependent variable. The input current can be calculated using the principles of linear regulation and switched capacitor conversion. In an ideal linear regulator, the current into the circuit is equal to the current out of the circuit. The principles of power conservation mandate the ideal input current of a 3/2-multiplier must be 1.5 times the output current. Adding a correction factor for operating quiescent current (IQ, 1.2 mA typ) gives an approximation for total input current which, when combined with the other input and output parameter(s), yields the following equation for efficiency:

$$E = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times (2 \cdot I_{OUT} + I_Q)}$$

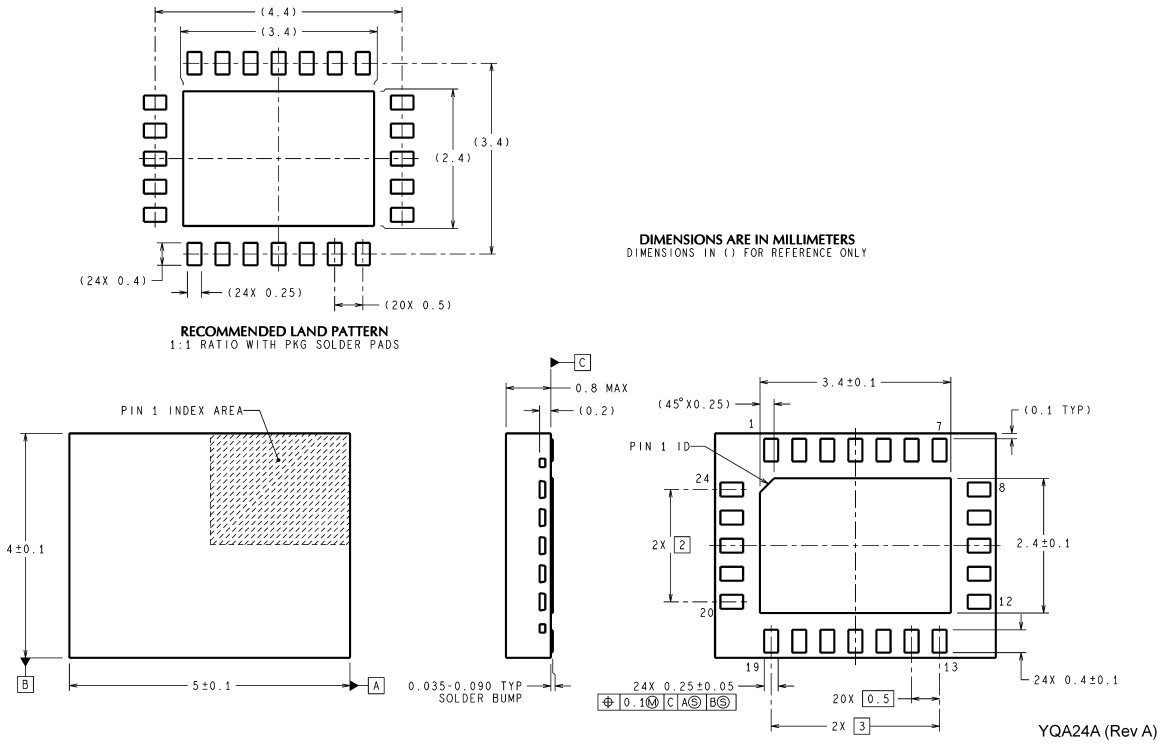
Because efficiency is inversely proportional to input voltage, it is highest when the input voltage is low. In fact, for an input voltage of 3.4V, efficiency of the LP3942 is greater than 80% ($I_{OUT} \geq 40$ mA). The average efficiency for an input voltage range spanning the input voltage range (3.4V-to-4.2V) is 75% (I_{out} = 120 mA). At higher input voltages, efficiency drops dramatically. In Li-Ion powered applications, this is typically not a major concern, as the circuit will be powered off a charger in these circumstances. Low efficiency equates to high power dissipation, however, which could become an issue worthy of attention.

LP3942's charge pump power dissipation (PD) is calculated simply by subtracting output power from input power:

$$P_D = P_{IN} - P_{OUT} = [V_{IN} \times (1.5 \cdot I_{OUT} + I_Q)] - [V_{OUT} \times I_{OUT}]$$

Power dissipation increases with increased input voltage and output current, up to 450 mW at the ends of the operating ratings (V_{IN} = 5.5V, I_{OUT} = 120 mA). Internal power dissipation self-heats the device. Dissipating this amount power/ heat so the LP3942 does not overheat is a demanding thermal requirement for a small surface-mount package. When soldered to a PCB with layout conducive to power dissipation, the excellent thermal properties of the LLP package enable this power to be dissipated from the LP3942 with little or no derating, even when the circuit is placed in elevated ambient temperatures.

Physical Dimensions inches (millimeters) unless otherwise noted



24–Lead LLP Package (5 mm*4 mm*0.8 mm), Bumped
NS Package Number YQA24A

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