MIC2559

PCMCIA Dual Card Socket V_{PP} Switching Matrix

Not Recommended for New Designs

General Description

The MIC2559 Dual V_{PP} Matrix switches the four voltages required by PCMCIA (Personal Computer Memory Card International Association) card V_{PP1} and V_{PP2} Pins. The MIC2559 provides selectable 0V, 3.3V, 5.0V, or 12.0V (±5%) from the system power supply to V_{PP1} and V_{PP2}. Output voltage is selected by two digital inputs per V_{PP} pin. Output current ranges up to 120mA. Four output states, V_{PP}, V_{CC}, high impedance, and active logic low are available, and V_{PP1} is independent of V_{PP2}. An auxiliary control input determines whether the high impedance (open) state or low logic state is asserted.

In standby mode or full operation, the device draws very little quiescent current, typically less than 1µA.

The MIC2559 is available in a 14-pin SOIC.

Applications

- PCMCIA V_{PP} Pin Voltage Switch
- Power Supply Management

Features

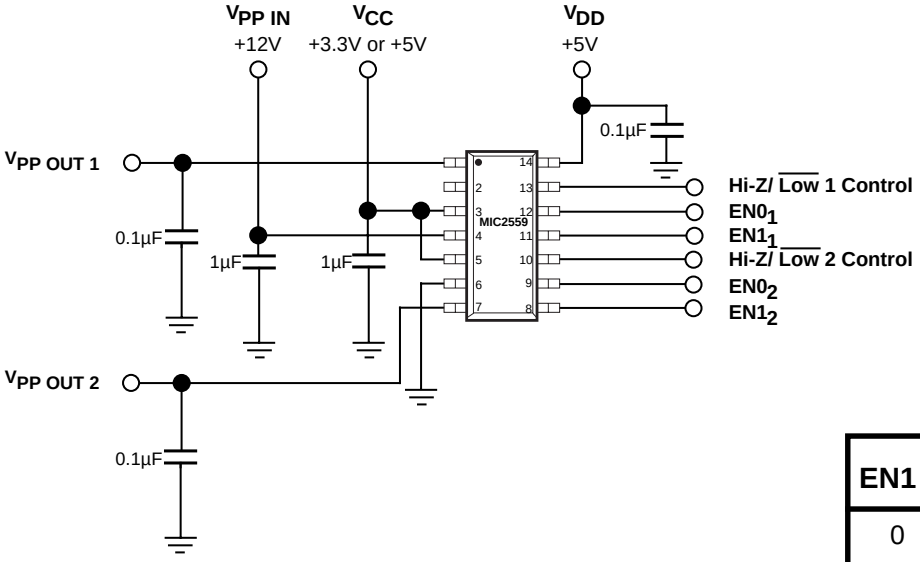
- Complete PCMCIA V_{PP} Switch Matrix in a Single IC
- Dual Matrix allows independent V_{PP1} and V_{PP2}
- Digital Selection of 0V, V_{CC}, V_{PP}, or High Imped–ance Output
- No V_{PPOUT} Overshoot or Switching Transients
- Break-Before-Make Switching
- Ultra Low Power Consumption
- 120mA V_{PP} (12V) Output Current
- Optional Active Source Clamp for Zero Volt Condition
- 3.3V or 5V Supply Operation
- 14-Pin SOIC Package

Ordering Information

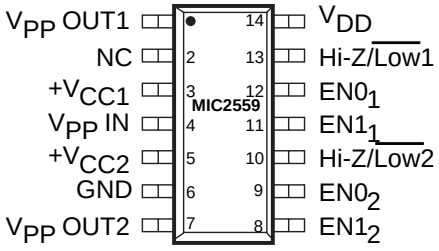
Part Number	Temperature Range	Package
MIC2559BM	–40°C to +85°C	14-pin SOIC
MIC2559BM T&R	–40°C to +85°C	14-SO Tape & Reel*

* 2,500 Parts per reel.

Typical Application



Pin Configuration



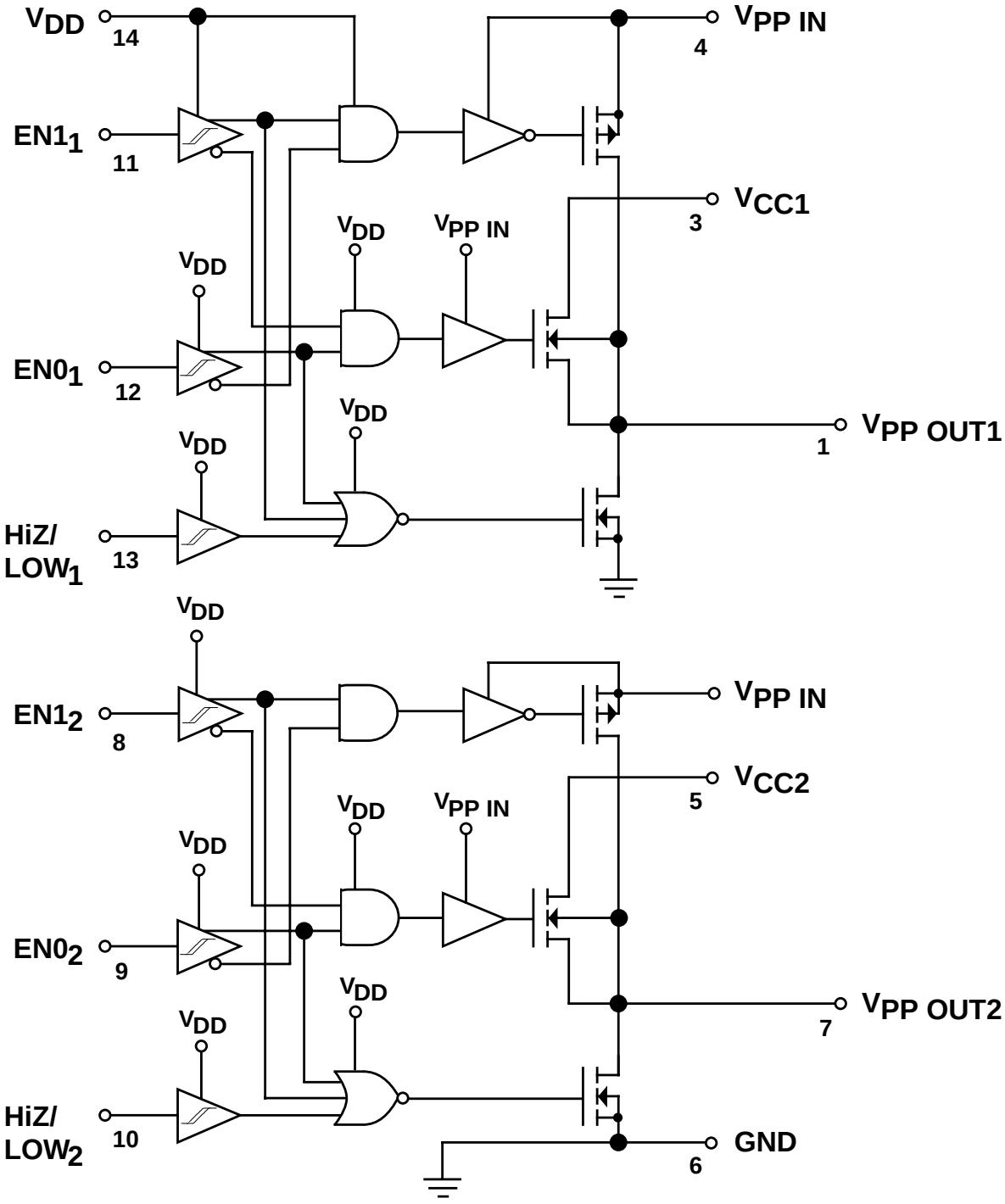
EN1	EN0	Hi-Z/Low	$V_{PP\ OUT}$
0	0	0	0V, (Sink current)
0	0	1	Hi-Z (No Connect)
0	1	x	V_{CC} (3.3V or 5.0V)
1	0	x	V_{PP}
1	1	x	Hi-Z (No Connect)

Absolute Maximum Ratings (Notes 1 and 2)

Power Dissipation, $T_{AMBIENT} \leq 25°C$	800 mW
Derating Factors (To Ambient)	4 mW/°C
Storage Temperature	–65°C to +150°C
Operating Temperature (Die)	125°C
Operating Temperature (Ambient)	–40°C to +85°C
Lead Temperature (5 sec)	260°C

Supply Voltage, $V_{PP\ IN}$	15V
V_{CC}	7.5V
V_{DD}	7.5V
Logic Input Voltages	–5V to V_{DD}
Output Current (each Output)	
$V_{PP\ OUT} = 12V$	600mA
$V_{PP\ OUT} = V_{CC}$	250mA

Logic Block Diagram



Electrical Characteristics: (Over operating temperature range with V_{DD} = V_{CC}= 5V, $V_{PP\ IN}$ = 12 V unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.2			V
V_{IL}	Logic 0 Input Voltage				0.8	V
V_{IN} (Max)	Input Voltage Range		–5		V_{DD}	V
I_{IN}	Input Current	0 V < V_{IN} < V_{DD}			±1	µA
EACH OUTPUT						
V_{OL}	Clamp Low Output Voltage	EN0 = EN1 = HiZ = 0, I_{SINK} = 1.6mA			0.4	V
I_{OUT}, Hi-Z	High Impedance Output Leakage Current	EN0 = EN1 = 0, HiZ = 1. 0 ≤ $V_{PP\ OUT}$ ≤ 12V		1	10	µA
R_{OC}	Clamp Low Output Resistance	Resistance to Ground. I_{SINK} = 2mA EN0 = EN1 = 0, HiZ = 0.		130	250	Ω
R_O	Switch Resistance, $V_{PP\ OUT}$ = V_{CC}	$I_{PP\ OUT}$ = –100 mA (Sourcing) T_A = –40°C to +60°C		0.8	1.5	Ω
R_O	Switch Resistance, $V_{PP\ OUT}$ = $V_{PP\ IN}$	$I_{PP\ OUT}$ = –100 mA (Sourcing)		0.5	1	Ω
SWITCHING TIME (See Figure 1)						
t_1	Delay + Rise Time	$V_{PP\ OUT}$ = 0V to 5V (Notes 3, 5)		15	50	µs
t_2	Delay + Rise Time	$V_{PP\ OUT}$ = 5V to 12V (Notes 3, 5)		12	50	µs
t_3	Delay + Fall Time	$V_{PP\ OUT}$ = 12V to 5V (Notes 3, 5)		25	75	µs
t_4	Delay + Fall Time	$V_{PP\ OUT}$ = 5V to 0V (Notes 3, 5)		45	100	µs
t_5	Output Turn-On Delay	$V_{PP\ OUT}$ = Hi-Z to 5V (Notes 4, 5)		10	50	µs
t_6	Output Turn-Off Delay	$V_{PP\ OUT}$ = 5V to Hi-Z (Notes 4, 5)		75	200	ns
POWER SUPPLY						
I_{DD}	V_{DD} Supply Current			–	1	µA
I_{CC}	V_{CC} Supply Current	$I_{PP\ OUT}$ = 0		–	1	µA
I_{PP}	I_{PP} Supply Current	$V_{PP\ OUT1}$ = V_{PPOUT2} = 0 V or V_{PP} . I_{PPOUT} = 0.		–	10	µA
		$V_{PP\ OUT1}$ = V_{PPOUT2} = V_{CC}		20	80	µA

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY, continued						
V_{CC}	Operating Input Voltage				6	V
V_{DD}	Operating Input Voltage		2.8		6	V
$V_{PP\ IN}$	Operating Input Voltage		8.0		14.5	V

NOTE 1: Functional operation above the absolute maximum stress ratings is not implied.
NOTE 2: Static-sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent damage from static discharge.
NOTE 3: With R_L = 2.9kΩ and C_{OUT} = 0.1µF on $V_{PP\ OUT}$.
NOTE 4: R_L = 2.9kΩ. R_L is connected to V_{CC} during t_5, and is connected to ground during t_6.
NOTE 5: Rise and fall times are measured to 90% of the difference of initial and final values.

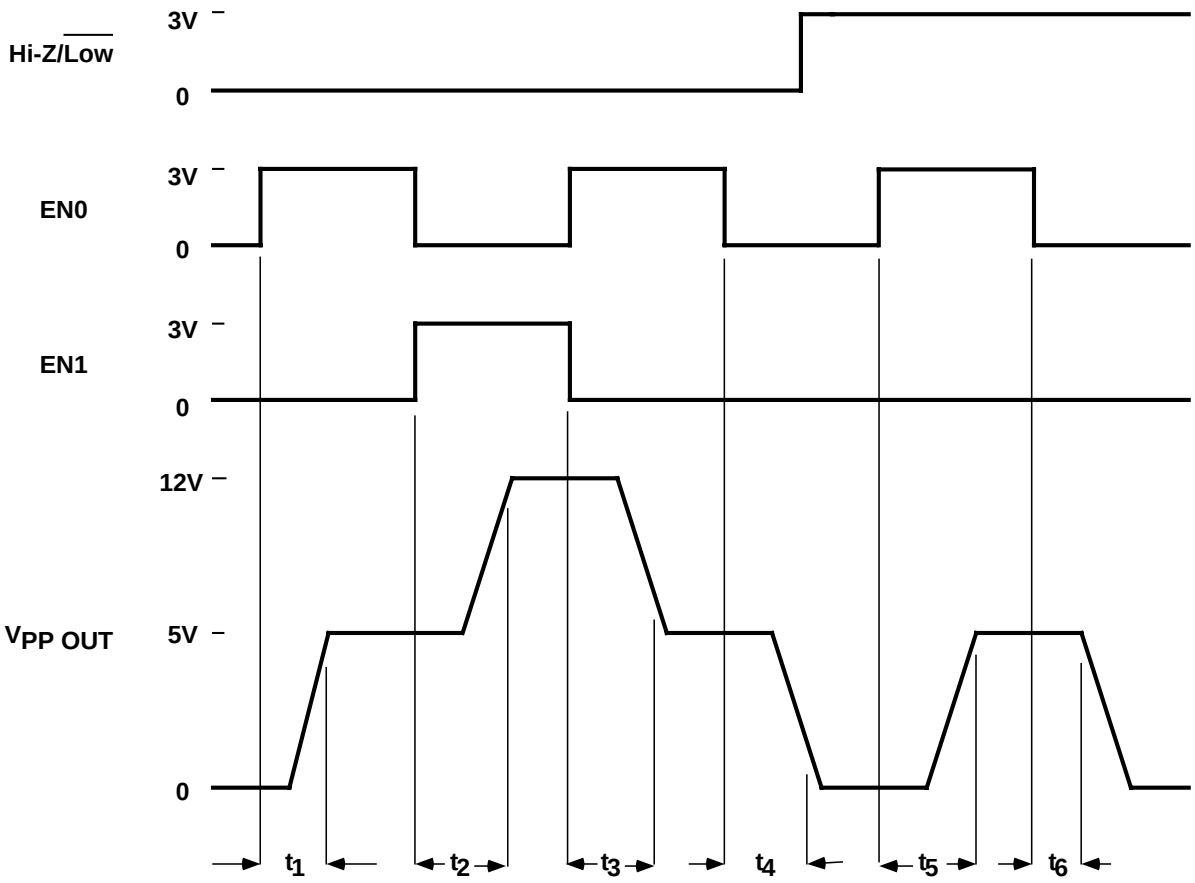


Figure 1. Timing Diagram.

Applications Information

PCMCIA V_{PP1} and V_{PP2} control is easily accomplished using the MIC2559 voltage selector/switch IC. Two control bits per $V_{PP\ OUT}$ pin determine output voltage and standby/operate mode condition. Output voltages of 0V (defined as less than 0.4V), V_{CC} (3.3V or 5V), V_{PP}, or a high impedance state, are available. When either the high impedance or low voltage conditions are selected, the device switches into "sleep" mode and draws only nanoamperes of leakage current.

The MIC2559 is a dual low-resistance power MOSFET switching matrix that operates from the computer system main power supply. Device power is obtained from V_{DD}, which may be either 3.3V or 5V, and FET drive is obtained from $V_{PP\ IN}$ (usually +12V). Internal break-before-make switches determine the output voltage and device mode. V_{PP1} and V_{PP2} are completely indepenent from each other.

Supply Bypassing

For best results, bypass V_{CC} and $V_{PP\ IN}$ inputs with 1µF capacitors. Both $V_{PP\ OUT}$ pins should have a 0.01µF to 0.1µF capacitor for noise reduction and electrostatic discharge (ESD) damage prevention. Larger values of output capacitor will create large current spikes during transitions, requiring larger bypass capacitors on the V_{CC} and $V_{PP\ IN}$ pins.

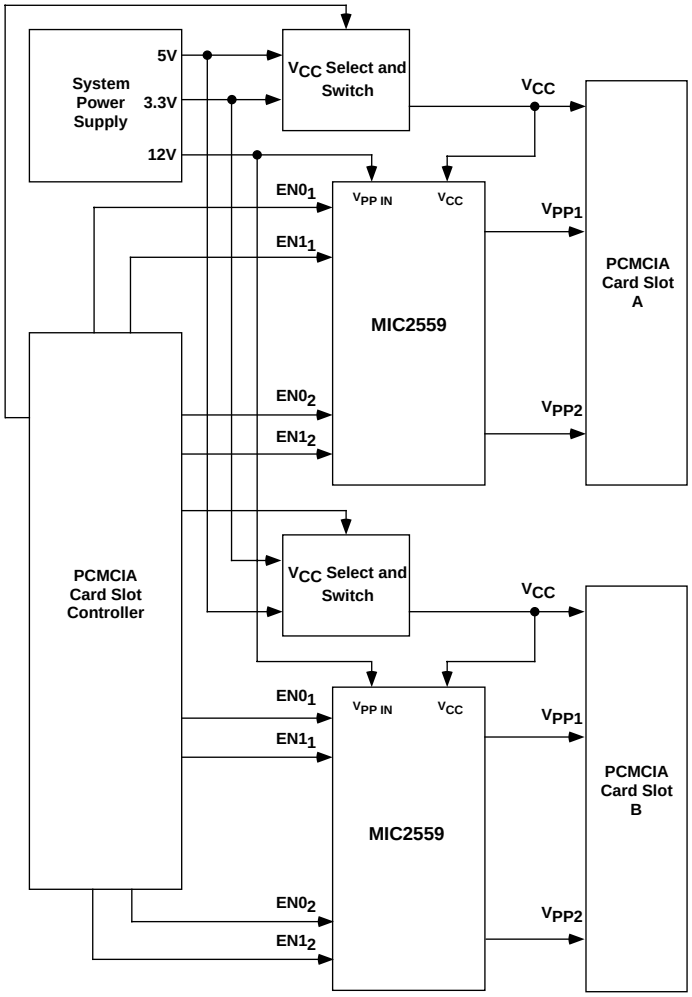


Figure 2. MIC2559 Typical two slot PCMCIA application with dual V_{CC} (5.0V or 3.3V).

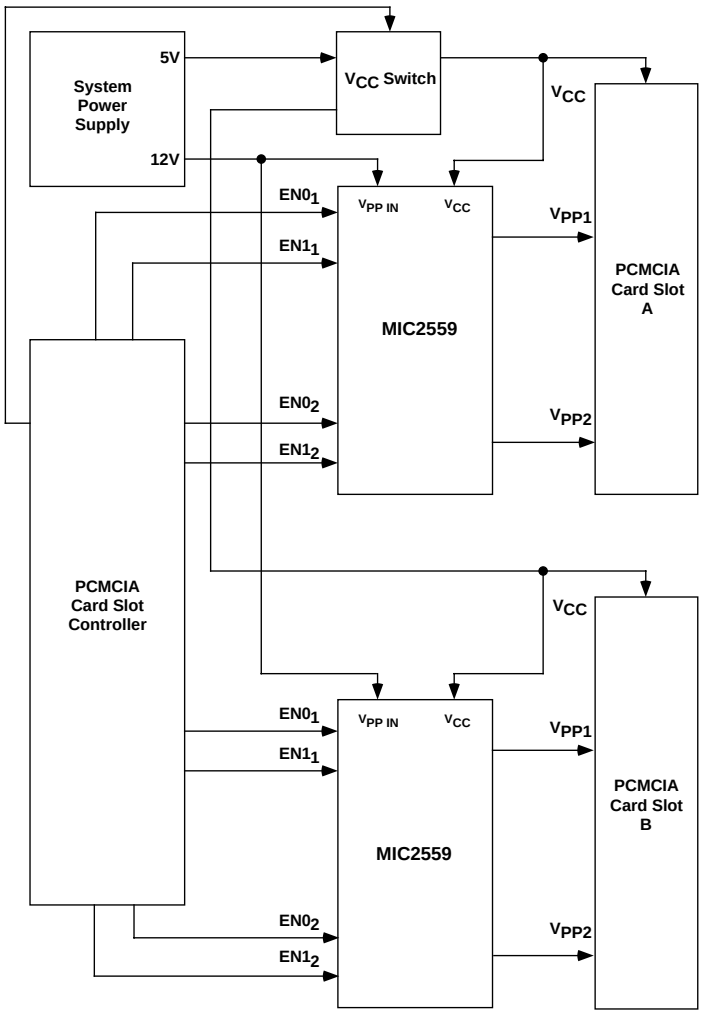


Figure 3. MIC2559 Typical two slot PCMCIA application with single 5.0V V_{CC}.

PCMCIA Implementation

The Personal Computer Memory Card International Association (PCMCIA) specification, version 2.0 (September, 1991), requires two V_{PP} supply pins per PCMCIA slot. V_{PP} is primarily used for programming Flash (EEPROM) memory cards. The two V_{PP} supply pins may be programmed to different voltages. Fully implementing PCMCIA specifications requires a MIC2559 and a controller. Figure 2 shows this full configuration, supporting both 5.0V and 3.3V V_{CC} operation. Figure 3 is a simplified design with fixed V_{CC} = 5V.

When a memory card is initially inserted, it should receive V_{CC} — usually 5.0V ±5%. The card sends a handshaking data stream to the controller, which then determines whether or not this card requires V_{PP} and if the card is designed for 5.0V or 3.3V V_{CC}. If the card uses 3.3V V_{CC}, the controller commands this change, which is reflected on the V_{CC} pins of both the PCMCIA slot and the MIC2559.

During Flash memory programming, the PCMCIA controller outputs a (1,0) to one or both halves of the MIC2559, which connects $V_{PP\ IN}$ to $V_{PP\ OUT1}$ and/or $V_{PP\ OUT2}$. The low ON resistance of the MIC2559 switch requires only a small bypass capacitor on the $V_{PP\ OUT}$ pins, with the main filtering

action performed by a large filter capacitor on $V_{PP\ IN}$. The $V_{PP\ OUT}$ transition from V_{CC} to 12.0V typically takes 25µS. After programming is completed, the controller outputs a (0,1) to the MIC2559, which then reduces $V_{PP\ OUT}$ to the V_{CC} level. Break-before-make switching action reduces switching transients and lowers maximum current spikes through the switch from the output capacitor.

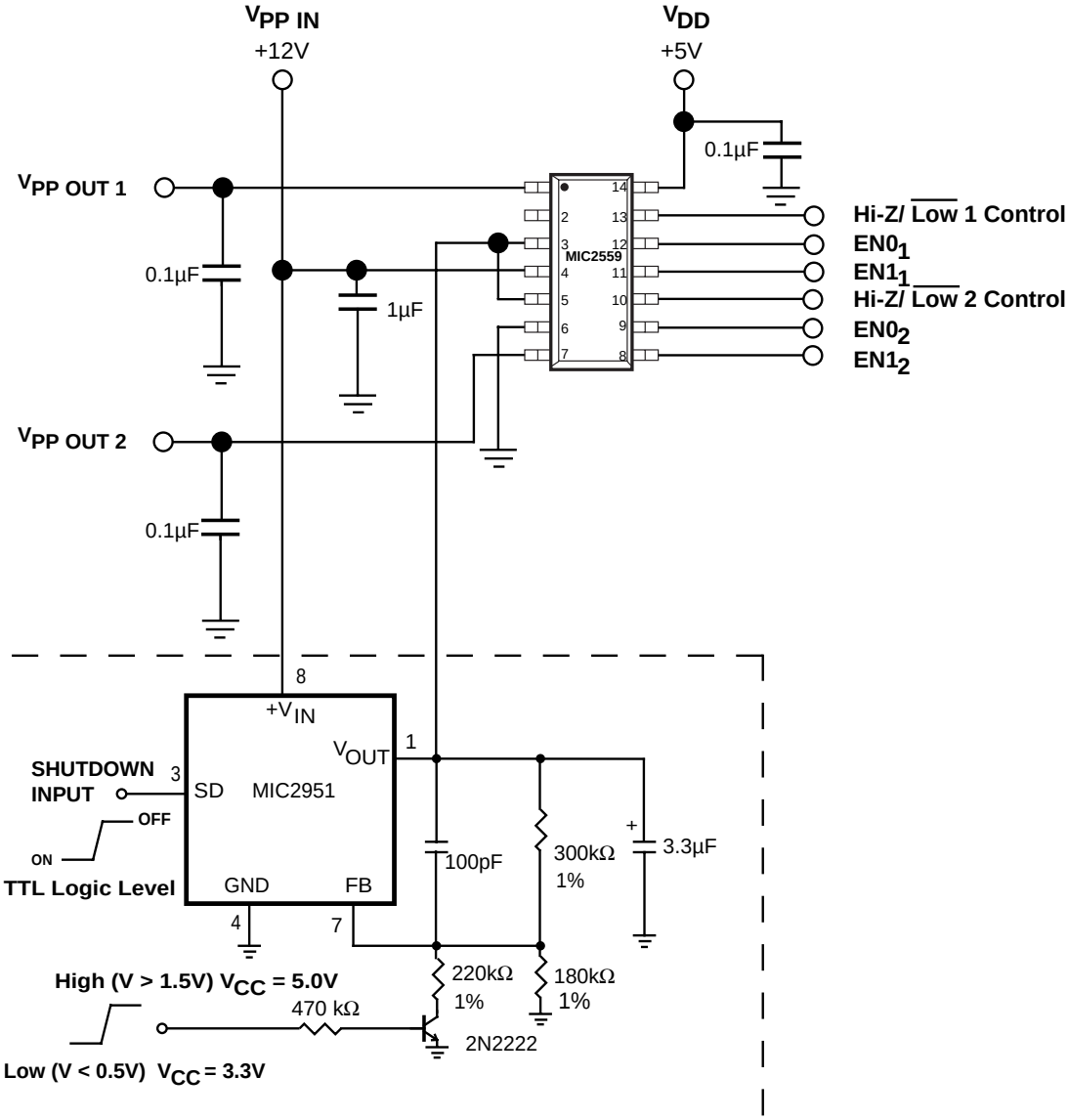
If no card is inserted, or the system is in sleep mode, the controller outputs either a (0,0) or a (1,1) to the MIC2559. Either input places the switch into shutdown mode, where current consumption drops even further.

The HiZ/Low input controls the optional logic low output clamp. With HiZ/Low in the high state and EN0 = EN1 = 0, $V_{PP\ OUT}$ enters a high impedance (open) state. With HiZ/Low in the low state and EN0 = EN1 = 0, $V_{PP\ OUT}$ is clamped to ground, providing a logic low signal. The clamp does not require any DC bias current for operation.

MOSFET drive and bias voltage is derived from $V_{PP\ IN}$. Internal device control logic is powered from V_{DD}, which should be connected to the same supply voltage as the PCMCIA controller (normally either 3.3V or 5V).

Output Current

MIC2559 output switches are capable of far more current than usually needed in PCMCIA applications. PCMCIA V_{PP} output current is limited primarily by switch resistance voltage drop (**I** x **R**) and the requirement that $V_{PP\ OUT}$ cannot drop more than 5% below nominal. $V_{PP\ OUT}$ will survive output short circuits to ground if $V_{PP\ IN}$ or V_{CC} are current limited by the regulator that supplies these voltages.



V_{CC} Switching and Control Block

Figure 3. Full PCMCIA Implementation of V_{PP} and V_{CC} switching using MIC2559 and MIC2951 voltage regulator.