



April 2000

QFET™

FQD3N60 / FQU3N60

600V N-Channel MOSFET

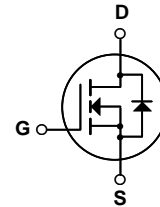
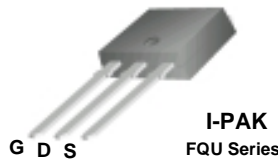
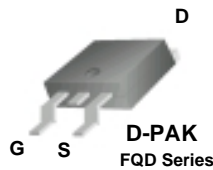
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply.

Features

- 2.4A, 600V, $R_{DS(on)} = 3.6\Omega @ V_{GS} = 10V$
- Low gate charge (typical 10 nC)
- Low Crss (typical 5.5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | FQD3N60 / FQU3N60 | Units |
|----------------|---|-------------------|---------------------|
| V_{DSS} | Drain-Source Voltage | 600 | V |
| I_D | Drain Current - Continuous ($T_C = 25^\circ\text{C}$) | 2.4 | A |
| | | 1.5 | A |
| I_{DM} | Drain Current - Pulsed (Note 1) | 9.6 | A |
| V_{GSS} | Gate-Source Voltage | ± 30 | V |
| E_{AS} | Single Pulsed Avalanche Energy (Note 2) | 200 | mJ |
| I_{AR} | Avalanche Current (Note 1) | 2.4 | A |
| E_{AR} | Repetitive Avalanche Energy (Note 1) | 5.0 | mJ |
| dv/dt | Peak Diode Recovery dv/dt (Note 3) | 4.5 | V/ns |
| P_D | Power Dissipation ($T_A = 25^\circ\text{C}$) * | 2.5 | W |
| | Power Dissipation ($T_C = 25^\circ\text{C}$) | 50 | W |
| | - Derate above 25°C | 0.4 | W/ $^\circ\text{C}$ |
| T_J, T_{STG} | Operating and Storage Temperature Range | -55 to +150 | $^\circ\text{C}$ |
| T_L | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | 300 | $^\circ\text{C}$ |

Thermal Characteristics

| Symbol | Parameter | Typ | Max | Units |
|-----------------|---|-----|-----|---------------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | -- | 2.5 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient * | -- | 50 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | -- | 110 | $^\circ\text{C}/\text{W}$ |

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics T_C = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

Off Characteristics

| | | | | | | |
|--------------------------------------|---|---|-----|-----|------|------|
| BV _{DSS} | Drain-Source Breakdown Voltage | V _{GS} = 0 V, I _D = 250 μA | 600 | -- | -- | V |
| ΔBV _{DSS} / ΔT _J | Breakdown Voltage Temperature Coefficient | I _D = 250 μA, Referenced to 25°C | -- | 0.6 | -- | V/°C |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} = 600 V, V _{GS} = 0 V | -- | -- | 10 | μA |
| | | V _{DS} = 480 V, T _C = 125°C | -- | -- | 100 | μA |
| I _{GSSF} | Gate-Body Leakage Current, Forward | V _{GS} = 30 V, V _{DS} = 0 V | -- | -- | 100 | nA |
| I _{GSSR} | Gate-Body Leakage Current, Reverse | V _{GS} = -30 V, V _{DS} = 0 V | -- | -- | -100 | nA |

On Characteristics

| | | | | | | |
|---------------------|-----------------------------------|---|-----|-----|-----|---|
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} = V _{GS} , I _D = 250 μA | 3.0 | -- | 5.0 | V |
| R _{DS(on)} | Static Drain-Source On-Resistance | V _{GS} = 10 V, I _D = 1.2 A | -- | 2.8 | 3.6 | Ω |
| g _{FS} | Forward Transconductance | V _{DS} = 50 V, I _D = 1.2 A (Note 4) | -- | 2.4 | -- | S |

Dynamic Characteristics

| | | | | | | |
|------------------|------------------------------|---|----|-----|-----|----|
| C _{iss} | Input Capacitance | V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz | -- | 350 | 450 | pF |
| C _{oss} | Output Capacitance | | -- | 50 | 65 | pF |
| C _{rss} | Reverse Transfer Capacitance | | -- | 5.5 | 7.5 | pF |

Switching Characteristics

| | | | | | | |
|---------------------|---------------------|---|----|-----|----|----|
| t _{d(on)} | Turn-On Delay Time | V _{DD} = 300 V, I _D = 3.0 A, R _G = 25 Ω (Note 4, 5) | -- | 10 | 30 | ns |
| t _r | Turn-On Rise Time | | -- | 30 | 70 | ns |
| t _{d(off)} | Turn-Off Delay Time | | -- | 20 | 50 | ns |
| t _f | Turn-Off Fall Time | | -- | 30 | 70 | ns |
| Q _g | Total Gate Charge | V _{DS} = 480 V, I _D = 3.0 A, V _{GS} = 10 V (Note 4, 5) | -- | 10 | 13 | nC |
| Q _{gs} | Gate-Source Charge | | -- | 2.7 | -- | nC |
| Q _{gd} | Gate-Drain Charge | | -- | 4.9 | -- | nC |

Drain-Source Diode Characteristics and Maximum Ratings

| | | | | | | |
|-----------------|---|--|----|-----|-----|----|
| I _S | Maximum Continuous Drain-Source Diode Forward Current | -- | -- | 2.4 | A | |
| I _{SM} | Maximum Pulsed Drain-Source Diode Forward Current | -- | -- | 9.6 | A | |
| V _{SD} | Drain-Source Diode Forward Voltage | V _{GS} = 0 V, I _S = 2.4 A | -- | -- | 1.4 | V |
| t _{rr} | Reverse Recovery Time | V _{GS} = 0 V, I _S = 3.0 A, | -- | 210 | -- | ns |
| Q _{rr} | Reverse Recovery Charge | di _F / dt = 100 A/μs (Note 4) | -- | 1.2 | -- | μC |

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 64mH, I_{AS} = 2.4A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 3.0A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

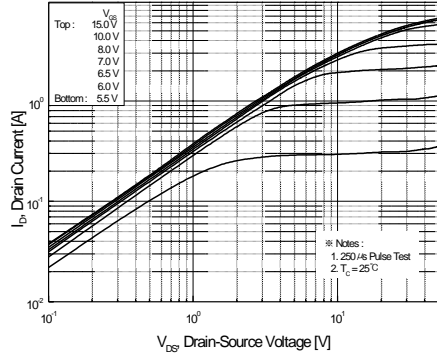


Figure 1. On-Region Characteristics

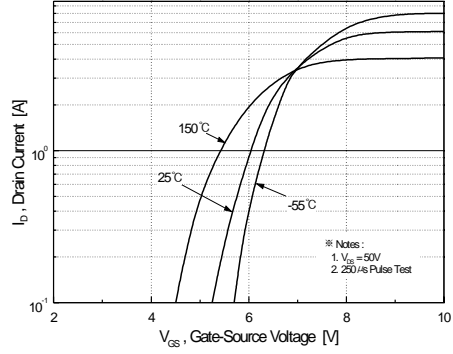


Figure 2. Transfer Characteristics

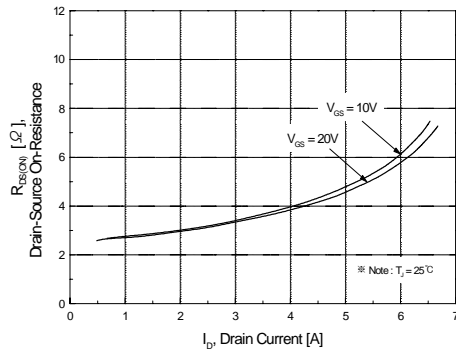


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

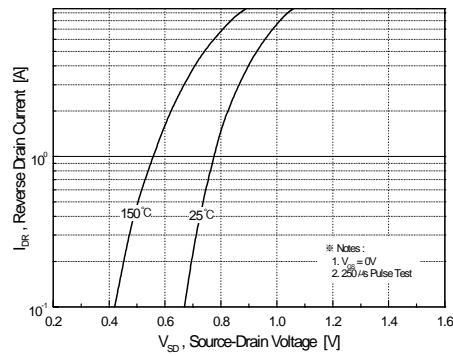


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

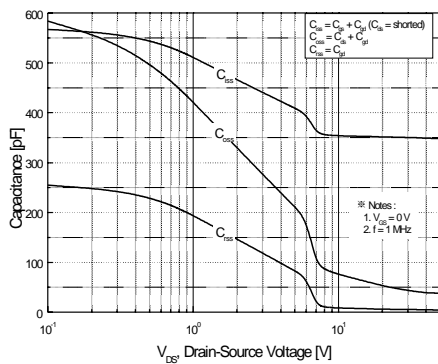


Figure 5. Capacitance Characteristics

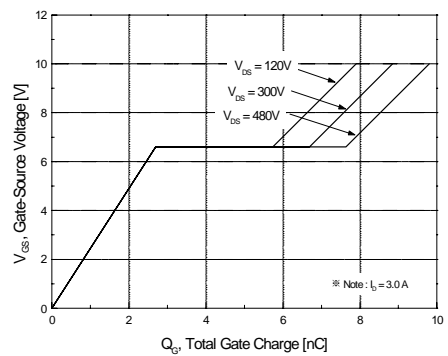


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

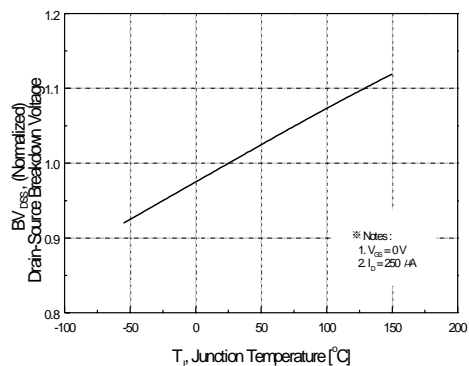


Figure 7. Breakdown Voltage Variation vs. Temperature

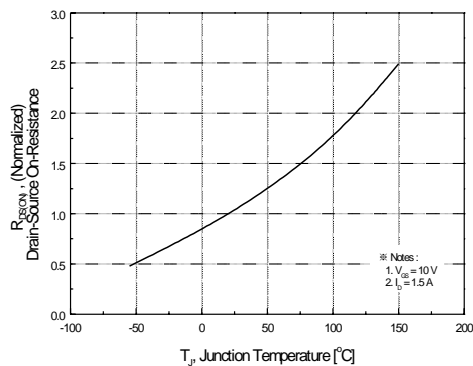


Figure 8. On-Resistance Variation vs. Temperature

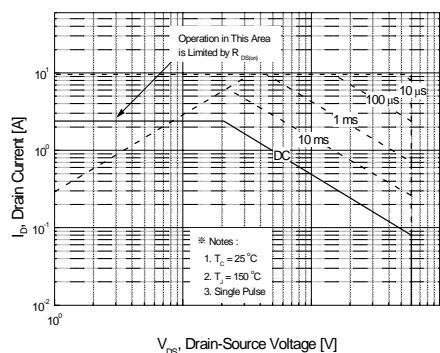


Figure 9. Maximum Safe Operating Area

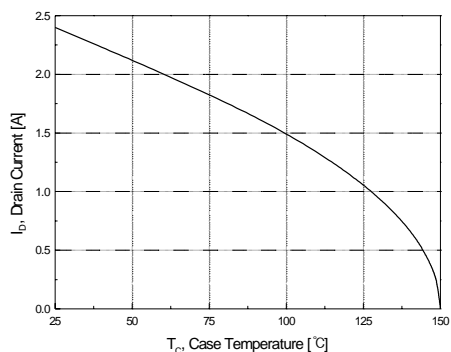


Figure 10. Maximum Drain Current vs. Case Temperature

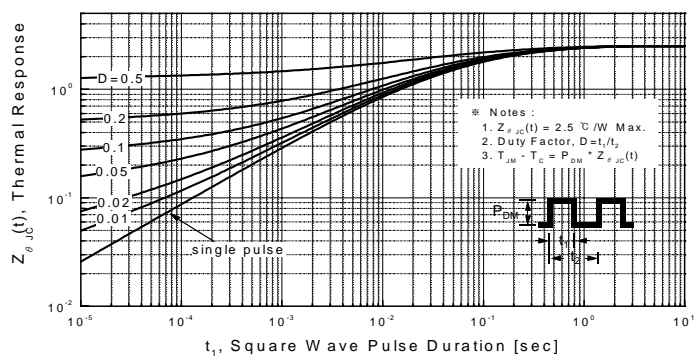
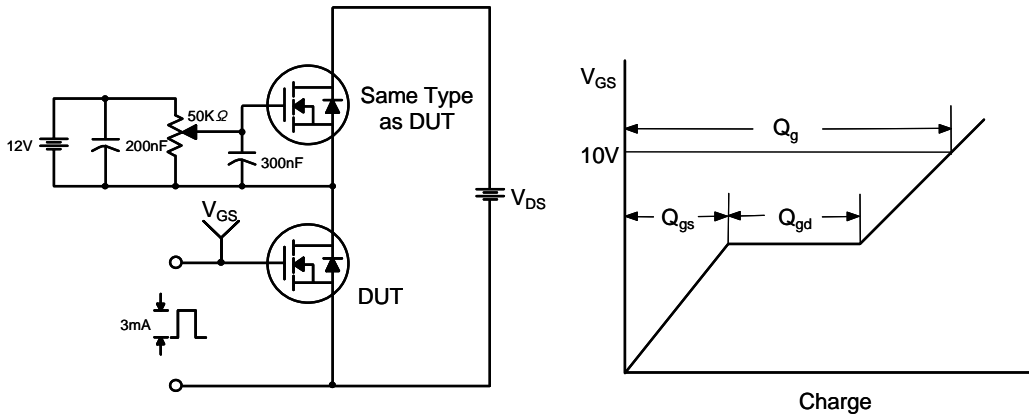
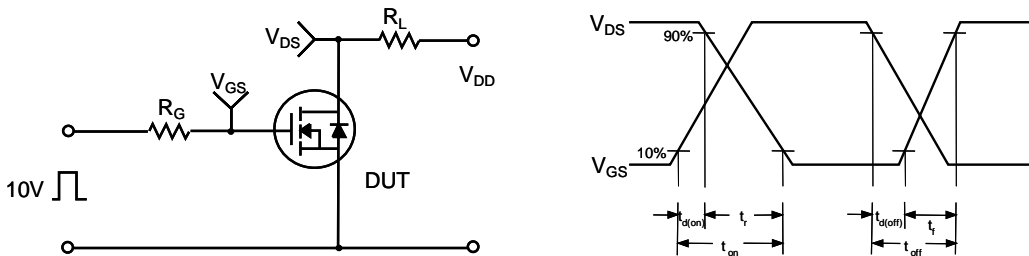


Figure 11. Transient Thermal Response Curve

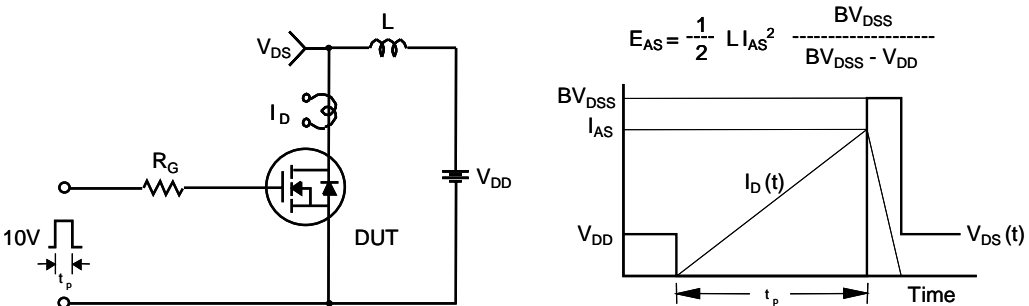
Gate Charge Test Circuit & Waveform



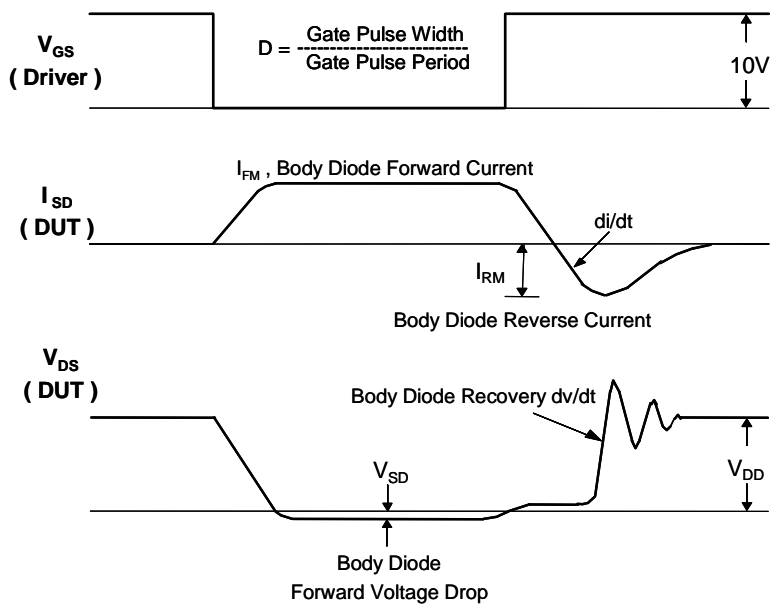
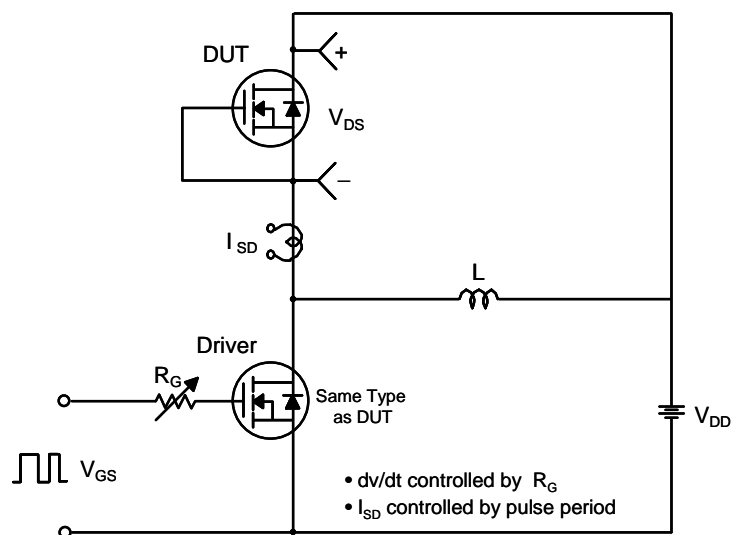
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

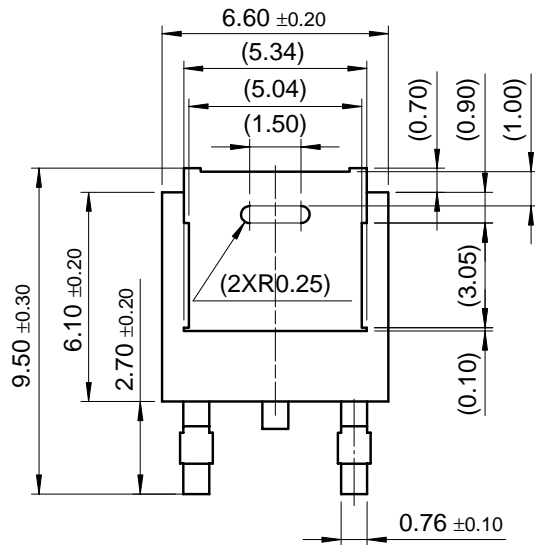
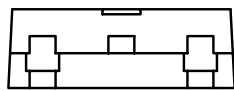
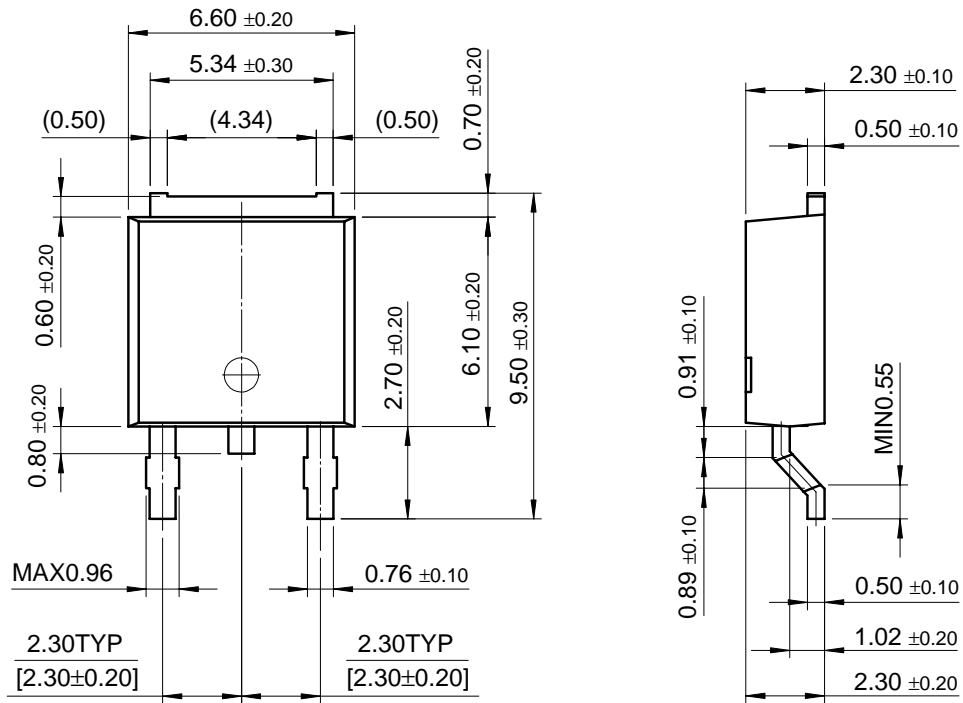


Peak Diode Recovery dv/dt Test Circuit & Waveforms



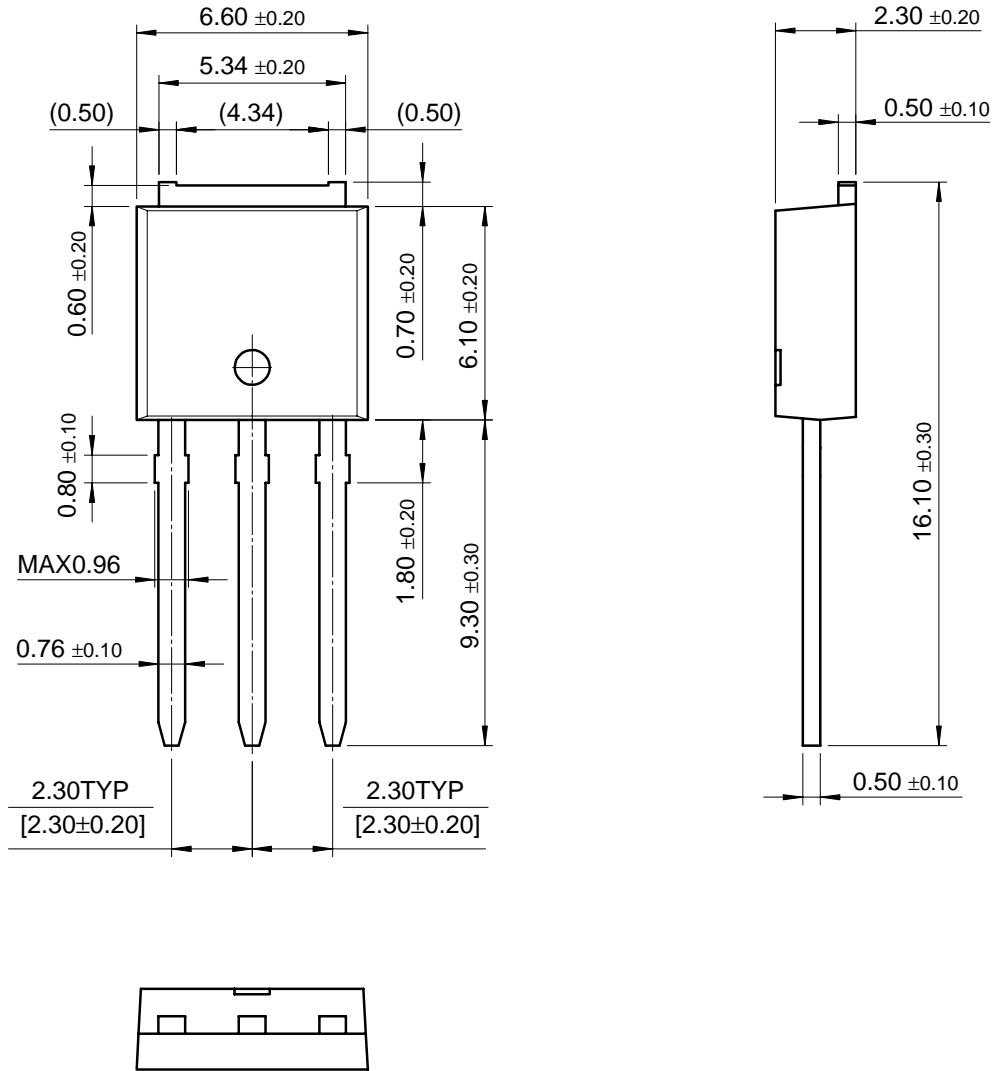
Package Dimensions

DPAK



Package Dimensions (Continued)

IPAK



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