Voltage Detector IC Series

Free Delay Time Setting CMOS Voltage Detector IC Series

BD52□□G, BD52□□FVE, BD53□□G, BD53□□FVE series

No.09006EBT03

● Description

ROHM's BD52□□G/FVE and BD53□□G/FVE series are highly accurate, low current consumption reset IC series with a built-in delay circuit. The lineup was established with tow output types (Nch open drain and CMOS output) and detection voltages range from 2.3V to 6.0V in increments of 0.1V, so that the series may be selected according the application at hand.

● Features

1) Detection voltage: 2.3V to 6.0V (Typ.), 0.1V steps
2) High accuracy detection voltage: ±1.0%
3) Ultra-low current consumption: 0.8µA (Typ.)
4) Nch open drain output (BD52□□G/FVE), CMOS output (BD53□□G/FVE)
5) Compact packages VSOF5: BD52□□FVE, BD53□□FVE
SSOP5: BD52□□G, BD53□□G

● Applications

All electronic devices that use micro controllers and logic circuits

● Selection Guide

Part Number : BD5 □ □□ □
① ② ③

No.	Specifications	Description
①	Output Circuit Format	2:Open Drain Output, 3:CMOS Output
②	Detection Voltage	Example: Displays VS over a 2.3V to 6.0V range in 0.1V increments.
③	Package	G:SSOP5 / FVE:VSOF5

● Lineup

Marking	Detection Voltage	Part Number	Marking	Detection Voltage	Part Number	Marking	Detection Voltage	Part Number	Marking	Detection Voltage	Part Number
PW	6.0V	BD5260	PB	4.1V	BD5241	RW	6.0V	BD5360	RB	4.1V	BD5341
PV	5.9V	BD5259	PA	4.0V	BD5240	RV	5.9V	BD5359	RA	4.0V	BD5340
PU	5.8V	BD5258	MV	3.9V	BD5239	RU	5.8V	BD5358	QV	3.9V	BD5339
PT	5.7V	BD5257	MU	3.8V	BD5238	RT	5.7V	BD5357	QU	3.8V	BD5338
PS	5.6V	BD5256	MT	3.7V	BD5237	RS	5.6V	BD5356	QT	3.7V	BD5337
PR	5.5V	BD5255	MS	3.6V	BD5236	RR	5.5V	BD5355	QS	3.6V	BD5336
PQ	5.4V	BD5254	MR	3.5V	BD5235	RQ	5.4V	BD5354	QR	3.5V	BD5335
PP	5.3V	BD5253	MQ	3.4V	BD5234	RP	5.3V	BD5353	QQ	3.4V	BD5334
PN	5.2V	BD5252	MP	3.3V	BD5233	RN	5.2V	BD5352	QP	3.3V	BD5333
PM	5.1V	BD5251	MN	3.2V	BD5232	RM	5.1V	BD5351	QN	3.2V	BD5332
PL	5.0V	BD5250	MM	3.1V	BD5231	RL	5.0V	BD5350	QM	3.1V	BD5331
PK	4.9V	BD5249	ML	3.0V	BD5230	RK	4.9V	BD5349	QL	3.0V	BD5330
PJ	4.8V	BD5248	MK	2.9V	BD5229	RJ	4.8V	BD5348	QK	2.9V	BD5329
PH	4.7V	BD5247	MJ	2.8V	BD5228	RH	4.7V	BD5347	QJ	2.8V	BD5328
PG	4.6V	BD5246	MH	2.7V	BD5227	RG	4.6V	BD5346	QH	2.7V	BD5327
PF	4.5V	BD5245	MG	2.6V	BD5226	RF	4.5V	BD5345	QG	2.6V	BD5326
PE	4.4V	BD5244	MF	2.5V	BD5225	RE	4.4V	BD5344	QF	2.5V	BD5325
PD	4.3V	BD5243	ME	2.4V	BD5224	RD	4.3V	BD5343	QE	2.4V	BD5324
PC	4.2V	BD5242	MD	2.3V	BD5223	RC	4.2V	BD5342	QD	2.3V	BD5323

● **Absolute maximum ratings (Ta=25°C)**

Parameter		Symbol	Limits	Unit
Power Supply Voltage		VDD-GND	-0.3 ~ +10	V
Output Voltage	Nch Open Drain Output	VOUT	GND-0.3 ~ +10	V
	CMOS Output		GND-0.3 ~ VDD+0.3	
Power Dissipation	SSOP5 *1*3	Pd	540	mW
	VSOF5 *2*3		210	
Operating Temperature		Topr	-40 ~ +105	°C
Ambient Storage Temperature		Tstg	-55 ~ +125	°C

*1 Use above Ta=25°C results in a 5.4mW loss per degree.
*2 Use above Ta=25°C results in a 2.1mW loss per degree.
*3 When a ROHM standard circuit board (70mm×70mm×1.6mm glass epoxy board) is mounted.

● **Electrical characteristics (Unless Otherwise Specified Ta=-40 to 105°C)**

Parameter	Symbol	Condition		Limit Min.	Limit Typ.	Limit Max.	Unit
Detection Voltage	V_{DET}	VDD=H→L, RL=470kΩ *1		VDET(T) ×0.99	VDET(T)	VDET(T) ×1.01	V
Circuit Current when ON	IDD1	VDD=VDET-0.2V	V_{DET} =2.3-3.1V	-	0.80	2.40	µA
			V_{DET} =3.2-4.2V	-	0.85	2.55	
			V_{DET} =4.3-5.2V	-	0.90	2.70	
			V_{DET} =5.3-6.0V	-	0.95	2.85	
Circuit Current when OFF	IDD2	VDD=VDET+2.0V	V_{DET} =2.3-3.1V	-	0.75	2.25	µA
			V_{DET} =3.2-4.2V	-	0.80	2.40	
			V_{DET} =4.3-5.2V	-	0.85	2.55	
			V_{DET} =5.3-6.0V	-	0.90	2.70	
Operating Voltage Range	VOPL	VOL≤0.4V, Ta=25~105°C, RL=470kΩ		0.95	-	-	V
		VOL≤0.4V, Ta=-40~25°C, RL=470kΩ		1.20	-	-	
'Low' Output Current (Nch)	IOL	VDS=0.5V VDD=1.2V		0.4	1.2	-	mA
		VDS=0.5V VDD=2.4V		2.0	5.0	-	
'High' Output Current (Pch)	IOH	VDS=0.5V VDD=4.8V VDET=2.3-4.2V		0.7	1.4	-	mA
		VDS=0.5V VDD=6.0V VDET=4.3-5.2V		0.9	1.8	-	
		VDS=0.5V VDD=8.0V VDET=5.3-6.0V		1.1	2.2	-	
Leak Current when OFF	Ileak	VDD=VDS=10V *1		-	-	0.1	µA
CT pin Threshold Voltage	VCTH	VDD=VDET×1.1, VDET=2.3-2.6V, RL=470kΩ		VDD ×0.30	VDD ×0.40	VDD ×0.60	V
		VDD=VDET×1.1, VDET=2.7-4.2V, RL=470kΩ		VDD ×0.30	VDD ×0.45	VDD ×0.60	
		VDD=VDET×1.1, VDET=4.3-5.2V, RL=470kΩ		VDD ×0.35	VDD ×0.50	VDD ×0.60	
		VDD=VDET×1.1, VDET=5.3-6.0V, RL=470kΩ		VDD ×0.40	VDD ×0.50	VDD ×0.60	
Output Delay Resistance	RCT	VDD=VDET×1.1 VCT=0.5V *1		5.5	9	12.5	MΩ
CT pin Output Current	ICT	VCT=0.1V VDD=0.95V *1		15	40	-	µA
		VCT=0.5V VDD=1.5V		150	240	-	
Detection Voltage Temperature coefficient	VDET/ΔT	Ta=-40°C to 105°C		-	±100	±360	ppm/°C
Hysteresis Voltage	ΔVs	VDD=L→H→L, RL=470kΩ		VDET ×0.03	VDET ×0.05	VDET ×0.08	V

V_S(T) : Standard Detection Voltage (2.3V to 6.0V, 0.1V step)
R_L: Pull-up resistor to be connected between VOUT and power supply.
Designed Guarantee. (Outgoing inspection is not done on all products.)
*1 Guarantee is Ta=25°C.

● Block Diagrams

BD52□□G/FVE

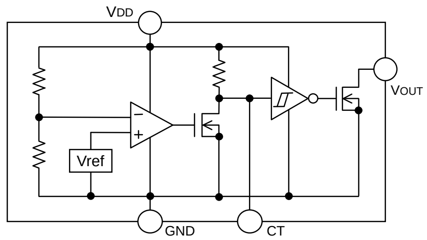


Fig.1

BD53□□G/FVE

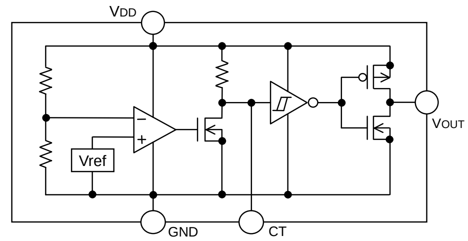
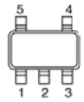


Fig.2

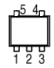
TOP VIEW



SSOP5

PIN No.	Symbol	Function
1	VOUT	Reset Output
2	VDD	Power Supply Voltage
3	GND	GND
4	N.C.	Unconnected Terminal
5	CT	Capacitor connection terminal for output delay time

TOP VIEW



VSOF5

PIN No.	Symbol	Function
1	VOUT	Reset Output
2	SUB	Substrate*
3	CT	Capacitor connection terminal for output delay time
4	GND	GND
5	VDD	Power Supply Voltage

*Connect the substrate to GND.

● **Reference Data (Unless specified otherwise, Ta=25°C)**

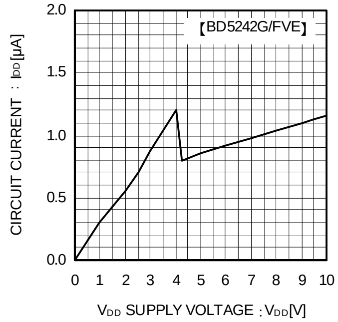


Fig.3 Circuit Current

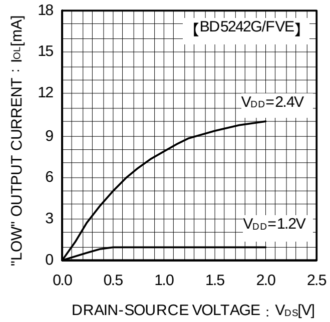


Fig.4 "Low" Output Current

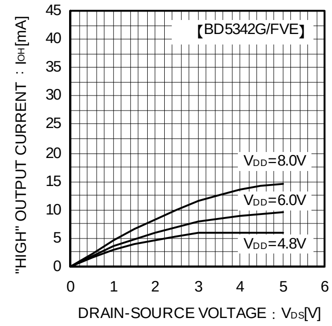


Fig.5 "High" Output Current

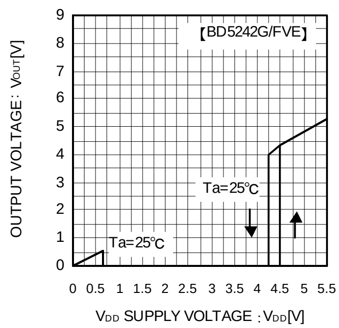


Fig.6 I/O Characteristics

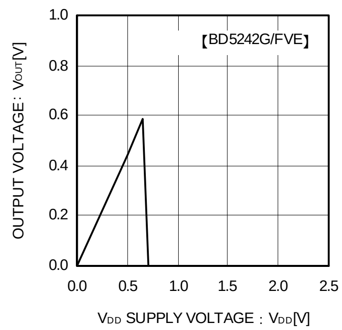


Fig.7 Operating Limit Voltage

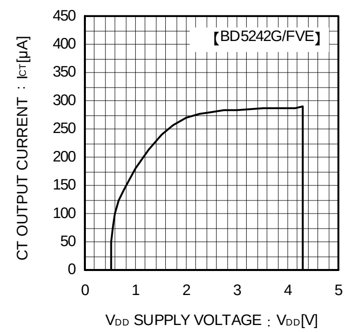


Fig.8 CT Terminal Current

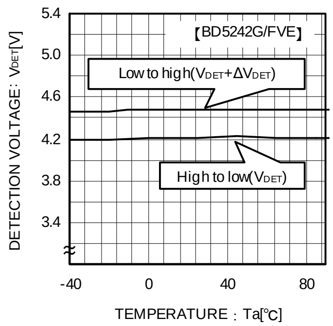


Fig.9 Detection Voltage
Release Voltage

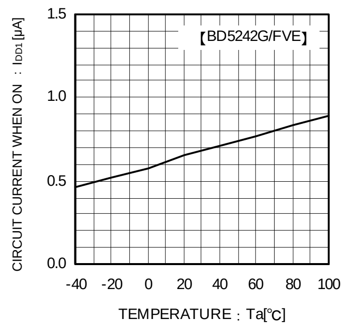


Fig.10 Circuit Current when ON

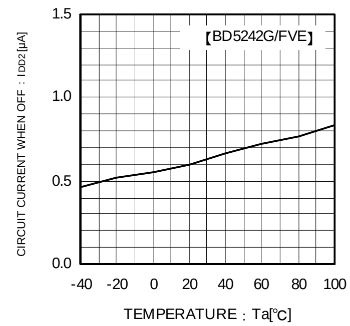


Fig.11 Circuit Current when OFF

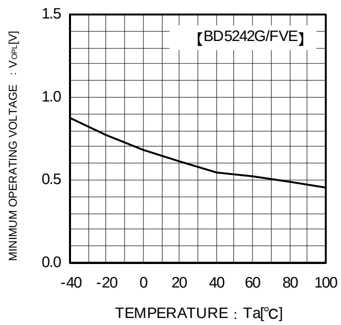


Fig.12 Operating Limit Voltage

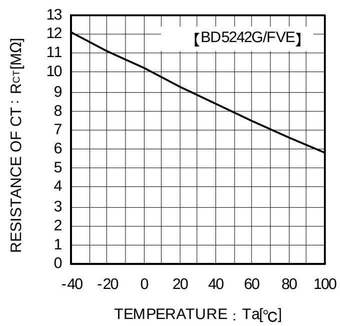


Fig.13 Ct Terminal Circuit Resistance

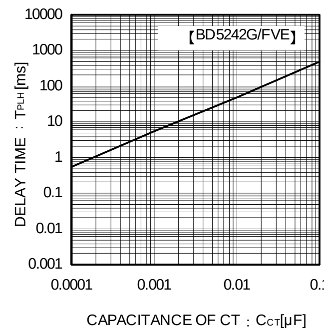


Fig.14 Delay Time (TPLH) and
CT Terminal External Capacitance

● Setting of Detector Delay Time

This detector IC can be set delay time at the rise of VDD by the capacitor connected to CT terminal.

Delay time at the rise of V_{DD} T_{PLH}: Time until when Vout rise to 1/2 of V_{DD} after V_{DD} rise up and beyond the release voltage($V_{DET}+\Delta V_{DET}$)

$$T_{PLH} = -C_{CT} \times R_{CT} \times \ln \left(\frac{V_{DD}-V_{CTH}}{V_{DD}} \right)$$

C_{CT}: CT pin Externally Attached Capacitance　　R_{CT}: CT pin Internal Impedance　(P.2 R_{CT} refer.)

V_{CTH}: CT pin Threshold Voltage (P.2 VCTH refer.)　　Ln : Natural Logarithm

● Reference Data of Falling Time (T_{PHL}) Output

Examples of Falling Time (T_{PHL}) Output

Part Number	tPHL[µs] -40°C	tPHL[µs] ,+25°C	tPHL[µs],+105°C
BD5227G	30.8	30	28.8
BD5327G	26.8	26	24.8

*This data is for reference only.

The figures will vary with the application, so please confirm actual operating conditions before use.

● Explanation of Operation

For both the open drain type (Fig.15) and the CMOS output type (Fig.16), the detection and release voltages are used as threshold voltages. When the voltage applied to the VDD pins reaches the applicable threshold voltage, the VOUT terminal voltage switches from either "High" to "Low" or from "Low" to "High". Because the BD52□□G/FVE series uses an open drain output type, it is possible to connect a pull-up resistor to VDD or another power supply [The output "High" voltage (VOUT) in this case becomes VDD or the voltage of the other power supply].

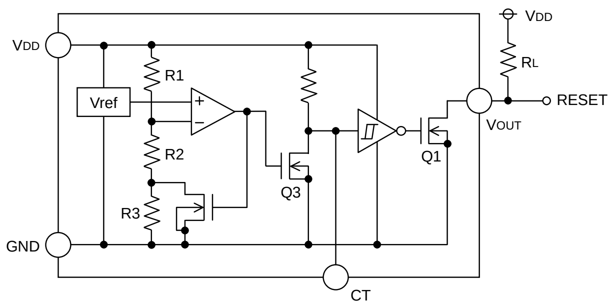


Fig.15 (BD52□□Type Internal Block Diagram)

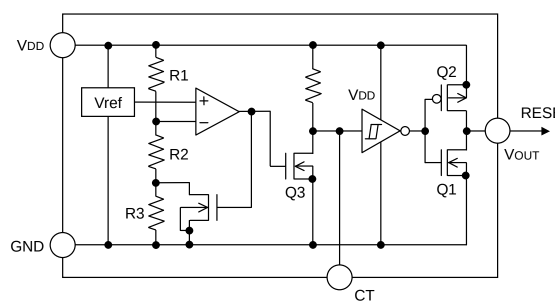


Fig.16 (BD53□□Type Internal Block Diagram)

● Timing Waveforms

Example: the following shows the relationship between the input voltage VDD, the CT Terminal Voltage VCT and the output voltage VOUT when the input power supply voltage VDD is made to sweep up and sweep down (The circuits are those in Fig.15 and 16).

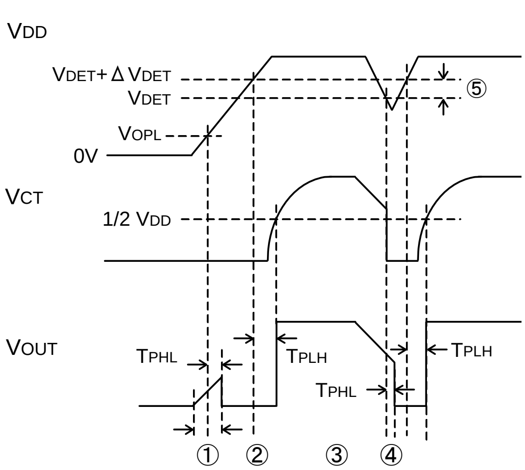


Fig.17

① When the power supply is turned on, the output is unsettled from after over the operating limit voltage (VOPL) until TPHL. There fore it is possible that the reset signal is not outputted when the rise time of VDD is faster than TPHL.

② When VDD is greater than VOPL but less than the reset release voltage (VDET+ΔVDET), the CT terminal (VCT) and output (VOUT) voltages will switch to L.

③ If VDD exceeds the reset release voltage (VDET+ΔVDET), then VOUT switches from L to H (with a delay to the CT terminal).

④ If VDD drops below the detection voltage (VDET) when the power supply is powered down or when there is a power supply fluctuation, VOUT switches to L (with a delay of TPHL).

⑤ The potential difference between the detection voltage and the release voltage is known as the hysteresis width (ΔVDET). The system is designed such that the output does not flip-flop with power supply fluctuations within this hysteresis width, preventing malfunctions due to noise.

● **Circuit Applications**

1) Examples of a common power supply detection reset circuit

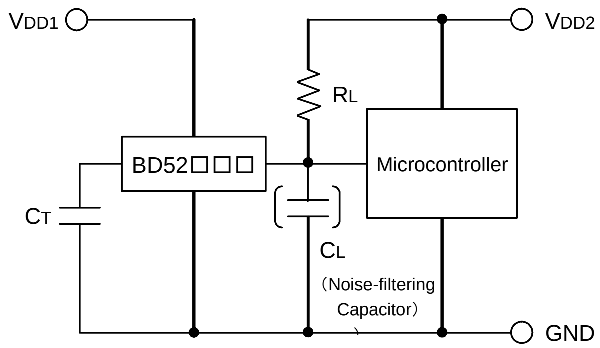


Fig.18 Open Collector Output Type

Application examples of BD52□□G/FVE series (Open Drain output type) and BD53□□G/FVE series (CMOS output type) are shown below.

CASE1: the power supply of the microcontroller (VDD2) differs from the power supply of the reset detection (VDD1).
Use the open drain output type (BD52□□G/FVE) attached a load resistance (RL) between the output and VDD2. (As shown Fig.15)

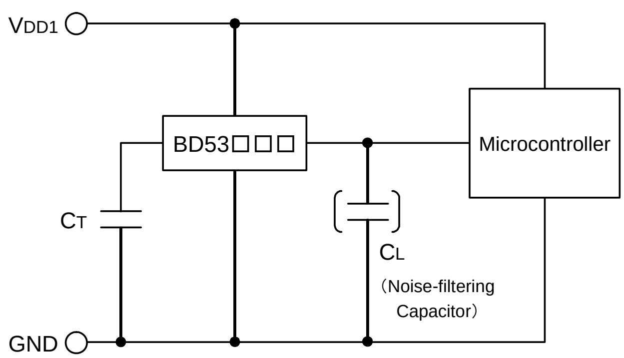


Fig.19 CMOS Output Type

CASE2: the power supply of the microcontroller (VDD1) is same as the power supply of the reset detection (VDD1).
Use CMOS output type (BD53□□G/FVE) or open drain output type (BD52□□G/FVE) attached a load resistance (RL) between the output and Vdd1. (As shown Fig.16)

When a capacitance CL for noise filtering is connected to the VOUT pin (the reset signal input terminal of the microcontroller), please take into account the waveform of the rise and fall of the output voltage (VOUT).

2) The following is an example of a circuit application in which an OR connection between two types of detection voltages resets the microcontroller.

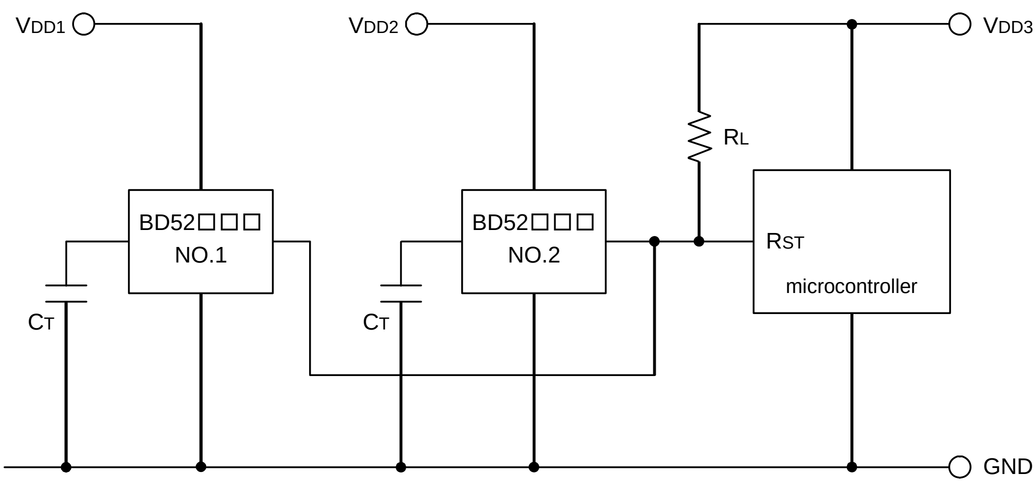


Fig.20

When there are many power supplies of the system, power supplies VDD1 and VDD2 are being monitored separately, and it is necessary to reset the microcomputer, it is possible to use an OR connection on the open drain output type BD52□□G/FVE series to pull-up to the desired voltage (VDD3) as shown in Fig.17 and make the output “High” voltage matches the power supply voltage VDD3 of the microcontroller.

3) Examples of the power supply with resistor dividers

In applications where the power supply input terminal (VDD) of an IC with resistor dividers, it is possible that a through current will momentarily flow into the circuit when the output logic switches, resulting in malfunctions (such as output oscillatory state).

(Through-current is a current that momentarily flows from the power supply (VDD) to ground (GND) when the output level switches from “High” to “Low” or vice versa.)

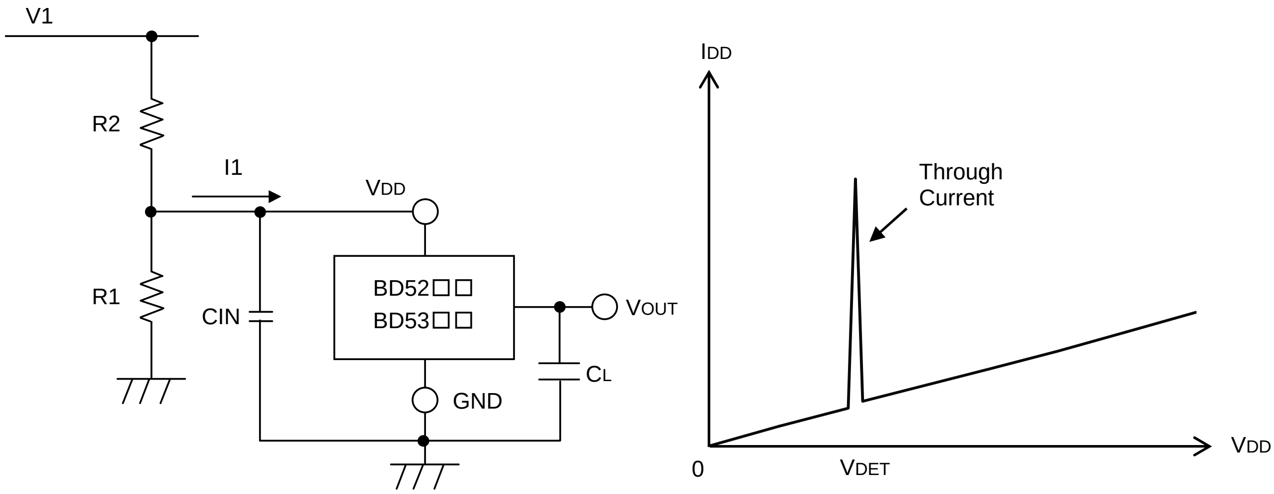


Fig.21

A voltage drop of [the through-current (I1)] × [input resistor (R2)] is caused by the through current, and the input voltage to descends, when the output switches from “Low” to “High”. When the input voltage decreases and falls below the detection voltage, the output voltage switches from “High” to “Low”. At this time, the through-current stops flowing through output “Low”, and the voltage drop is eliminated. As a result, the output switches from “Low” to “High”, which again causes the through current to flow and the voltage drop. This process is repeated, resulting in oscillation.

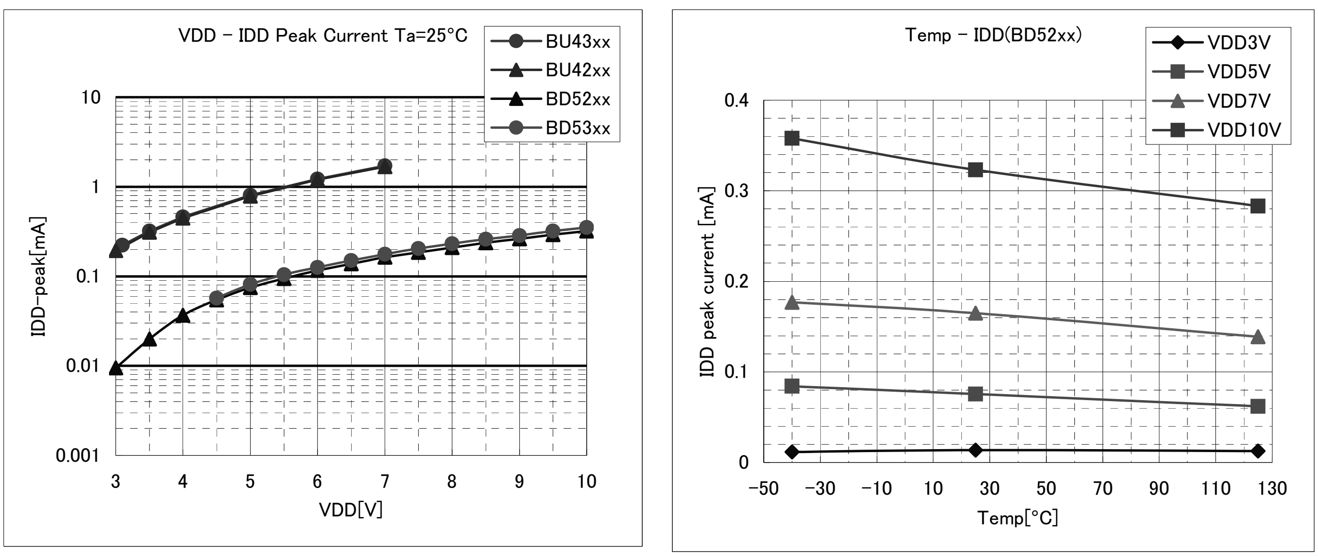


Fig.22 Current Consumption vs. Power Supply Voltage

*This data is for reference only.

The figures will vary with the application, so please confirm actual operating conditions before use.

● **Operation Notes**

1．Absolute maximum range
Absolute Maximum Ratings are those values beyond which the life of a device may be destroyed. We cannot be defined the failure mode, such as short mode or open mode. Therefore a physical security countermeasure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.

2．GND potential
GND terminal should be a lowest voltage potential every state.
Please make sure all pins, which are over ground even if, include transient feature.

3．Electrical Characteristics
Be sure to check the electrical characteristics that are one the tentative specification will be changed by temperature, supply voltage, and external circuit.

4．Bypass Capacitor for Noise Rejection
Please put into the capacitor of 1µF or more between VDD pin and GND, and the capacitor of about 1000pF between VOUT pin and GND, to reject noise. If extremely big capacitor is used, transient response might be late. Please confirm sufficiently for the point.

5．Short Circuit between Terminal and Soldering
Don’t short-circuit between Output pin and VDD pin, Output pin and GND pin, or VDD pin and GND pin. When soldering the IC on circuit board, please be unusually cautious about the orientation and the position of the IC. When the orientation is mistaken the IC may be destroyed.

6．Electromagnetic Field
Mal-function may happen when the device is used in the strong electromagnetic field.

7． The VDD line inpedance might cause oscillation because of the detection current.

8． A VDD -GND capacitor (as close connection as possible) should be used in high V_{DD} line impedance condition.

9． Lower than the mininum input voltage makes the V_{OUT} high impedance, and it must be V_{DD} in pull up (V_{DD}) condition.

10. This IC has extremely high impedance terminals. Small leak current due to the uncleanness of PCB surface might cause unexpected operations. Application values in these conditions should be selected carefully. If the leakage is assumed between the VOUT terminal and the GND terminal, the pull-up resistor should be less than 1/10 of the assumed leak resistance. If 10MΩ leakage is assumed between the CT terminal and the GND terminal, 1MΩ connection between the CT terminal and the V_{DD} terminal would be recommended. The value of R_{CT} depends on the external resistor that is connected to CT terminal, so please consider the delay time that is decided by τ×RCT×CCT changes.

11. External parameters
The recommended parameter range for C_T is 100pF~0.1µF and RL is 50kΩ~1MΩ. There are many factors (board layout, etc) that can affect characteristics. Please verify and confirm using practical applications.

12. Power on reset operation
Please note that the power on reset output varies with the VDD rise up time. Please verify the actual operation.

13. Precautions for board inspection
Connecting low-impedance capacitors to run inspections with the board may produce stress on the IC. Therefore, be certain to use proper discharge procedure before each process of the test operation.
To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handing, transfer and storage operations. Before attempting to connect components to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing any component connected to the test setup.

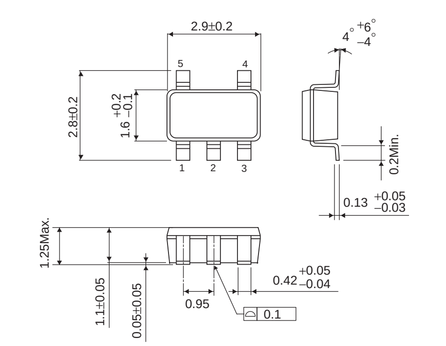
14. When the power supply, is turned on because of in certain cases, momentary Rash-current flow into the IC at the logic unsettled, the couple capacitance, GND pattern of width and leading line must be considered.

● **Part Number Selection**

B	D	5	2		2	3		G	–	T	R

- BD52: Adjustable Delay Time CMOS Reset IC Open Drain Type
  BD53: Adjustable Delay Time CMOS Reset IC CMOS Output Type
- Reset Voltage Value
  23: 2.3V to (0.1V step)
  60: 6.0V
- Package
  G: SSOP5
  FVE: VSOF5
- Taping Specifications
  Embossed Taping

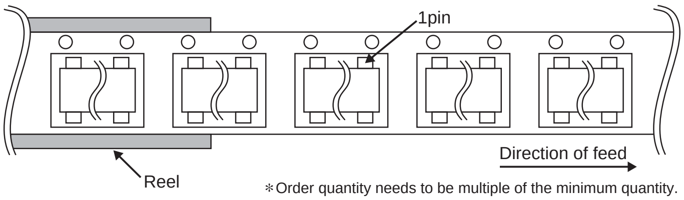
SSOP5



(Unit : mm)

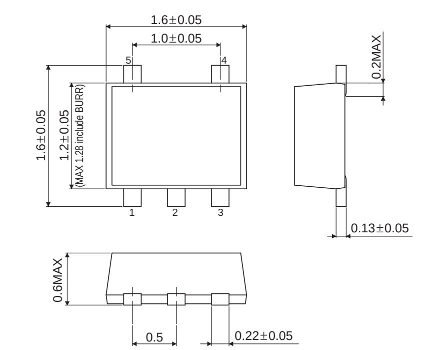
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

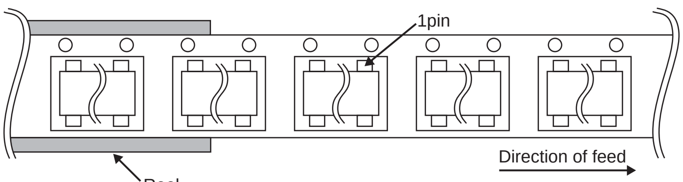
VSOF5



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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