Power Management Switch ICs for PCs and Digital Consumer Products

# Power Switch IC for ExpressCard™

**BD4154FV**

No.10029EBT09

## ●Description

BD4154FV is a power management switch IC for the next generation PC card (ExpressCard™) developed by the PCMCIA. It conforms to the PCMCIA ExpressCard™ Standard, ExpressCard™ Compliance Checklist, and ExpressCard™ Implementation Guideline, and obtains the Compliance ID "EC100040" from PCMCIA. The power switch offers a number of functions - card detector, and system status detector - which are ideally suited for laptop and desktop computers.

## ●Features

1) Incorporates three low on-resistance FETs for ExpressCard™.
2) Incorporates an FET for output discharge.
3) Incorporates an enabler.
4) Incorporates under voltage lockout (UVLO) protection.
5) Employs an SSOP-B20 package.
6) Built-in thermal shutdown protector (TSD).
7) Built-in soft start function.
8) Incorporates an overcurrent protection (OCP).
9) Built-in enable signal for PLL
10) Built-in Pull up resistance for detecting ExpressCard™
11) Conforms to the ExpressCard™ Standard.
12) Conforms to the ExpressCard™ Compliance Checklist.
13) Conforms to the ExpressCard™ Implementation Guideline.

## ●Applications

Laptop and desktop computers, and other ExpressCard™ equipped digital devices.

## ●Product Lineup

| Parameter | BD4154FV |
|---|---|
| Package | SSOP-B20 |

"ExpressCard™" is a registered trademark registered of the PCMCIA (Personal Computer Memory Card International Association).

●**Absolute Maximum Ratings**

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Input Voltage | V3AUX_IN, V3_IN, V15_IN | -0.3～5.0 *1 | V |
| Logic Input Voltage 1 | EN,CPPE#,CPUSB#,SYSR, PERST_IN#,RCLKEN | -0.3～V3AUX_IN+0.3 *1 | V |
| Logic Output Voltage 1 | RCLKEN | -0.3～V3AUX_IN+0.3 *1 | V |
| Logic Output Voltage 2 | PERST# | -0.3～V3AUX_IN+0.3 | V |
| Output Voltage | V3AUX,V3, V15 | -0.3～5.0 *1 | V |
| Output Current 1 | IOV3AUX | 1.0 | A |
| Output Current 2 | IOV3 | 2.0 | A |
| Output Current 3 | IOV15 | 2.0 | A |
| Power Dissipation 1 | Pd1 | 500.0 *2 | mW |
| Power Dissipation 2 | Pd2 | 812.5 *3 | mW |
| Operating Temperature Range | Topr | -40～+100 | ℃ |
| Storage Temperature Range | Tstg | -55～+150 | ℃ |
| Maximum Junction Temperature | Tjmax | +150 | ℃ |

*1 Not to exceed Pd.
*2 Reduced by 4.0mW for each increase in Ta of 1℃ over 25℃
*3 Reduced by 6.5mW for each increase in Ta of 1℃ over 25℃(When mounted on a board 70mmx70mmx1.6mm Glass-epoxy PCB)

●**Operating Conditions** (Ta=25℃)

| Parameter | Symbol | MIN | MAX | Unit |
|---|---|---|---|---|
| Input Voltage 1 | V3AUX_IN | 3.0 | 3.6 | V |
| Input Voltage 2 | V3_IN | 3.0 | 3.6 | V |
| Input Voltage 3 | V15_IN | 1.35 | 1.65 | V |
| Logic Input Voltage 1 | EN | -0.3 | 3.6 | V |
| Logic Input Voltage 2 | CPPE#,CPUSB#,SYSR, PERST_IN#,RCLKEN | 0 | V3AUX_IN | V |
| Logic Output Voltage 1 | RCLKEN | 0 | V3AUX_IN | V |
| Logic Output Voltage 2 | PERST# | 0 | V3AUX_IN | V |
| Output Current 1 | IOV3AUX | 0 | 275 | mA |
| Output Current 2 | IOV3 | 0 | 1.3 | A |
| Output Current 3 | IOV15 | 0 | 650 | mA |

* This product is not designed to offer protection against radioactive rays.

●**Electrical Characteristics (unless otherwise noted, Ta=25℃ VEN=3.3V V3AUX_IN =V3_IN=3.3V,V15_IN=1.5V)**

| Parameter | Symbol | Standard Value | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| Standby Current | IST | - | 40 | 80 | μA | VEN=0V (Include IEN, IRCLKEN) |
| Bias Current 1 | Icc1 | - | 120 | 250 | μA | VSYSR=0V |
| Bias Current 2 | Icc2 | - | 250 | 500 | μA | VSYSR=3.3V |
| [Enable] | | | | | | |
| High Level Enable Input Voltage | VENHI | 2.0 | - | 5.5 | V | |
| Low Level Enable Input Voltage | VENLOW | -0.2 | - | 0.8 | V | |
| Enable Pin Input Current | IEN | 10 | - | 30 | μA | VEN=0V |
| [Logic] | | | | | | |
| High Level Logic Input Voltage | VLHI | 2.0 | - | - | V | |
| Low Level Logic Input Voltage | VLLOW | - | - | 0.8 | V | |
| Logic Pin Input Current | ICPPE# | - | 0 | 1 | μA | CPPE#=3.6V |
| | | 10 | - | 30 | μA | CPPE#=0V |
| | ICPUSB# | - | 0 | 1 | μA | CPUSB#=3.6V |
| | | 10 | - | 30 | μA | CPUSB#=0V |
| | ISYSR | - | 0 | 1 | μA | SYSR=3.6V |
| | | 10 | - | 30 | μA | SYSR=0V |
| | IPRT_IN# | - | 0 | 1 | μA | PERST_IN#=3.6V |
| | | 10 | - | 30 | μA | PERST_IN#=0V |
| | IRCLKEN | - | 0 | 1 | μA | RCLKEN=3.6V |
| | | 10 | - | 30 | μA | RCLKEN=0V |
| RCLKEN Low Voltage | VRCLKEN | - | 0.1 | 0.3 | V | IRCLKEN=0.5mA |
| RCLKEN Leak Current | IRCLKEN | - | - | 1 | μA | VRCLKEN=3.65V |
| [Switch V3AUX] | | | | | | |
| On Resistance | $R_{V3AUX}$ | - | 120 | 220 | mΩ | Tj=-10～100℃ * |
| Discharge On Resistance | $R_{V3AUX}$ Dis | - | 60 | 150 | Ω | |
| [Switch V3] | | | | | | |
| On Resistance | $R_{V3}$ | - | 42 | 90 | mΩ | Tj=-10～100℃ * |
| Discharge On Resistance | $R_{V3}$Dis | - | 60 | 150 | Ω | |
| [Switch V15] | | | | | | |
| On Resistance | $R_{V15}$ | - | 45 | 90 | mΩ | Tj=-10～100℃ * |
| Discharge On Resistance | $R_{V15}$Dis | - | 60 | 150 | Ω | |
| [Over Current Protection] | | | | | | |
| V3 Over Current | $OCP_{V3}$ | 1.3 | - | - | A | |
| V3AUX Over Current | $OCP_{V3AUX}$ | 0.275 | - | - | A | |
| V15 Over Current | $OCP_{V15}$ | 0.65 | - | - | A | |
| [Under Voltage Lockout] | | | | | | |
| V3_IN UVLO OFF Voltage | $VUVLO_{V3\_IN}$ | 2.70 | 2.80 | 2.90 | V | sweep up |
| V3_IN Hysteresis Voltage | $\Delta VUVLO_{V3\_IN}$ | 50 | 100 | 150 | mV | sweep down |
| V3AUX_IN UVLO OFF Voltage | $VUVLO_{V3AUX\_IN}$ | 2.70 | 2.80 | 2.90 | V | sweep up |
| V3AUX_IN Hysteresis Voltage | $\Delta VUVLO_{V3AUX\_IN}$ | 50 | 100 | 150 | mV | sweep down |
| V15_IN UVLO OFF Voltage | $VUVLO_{V15\_IN}$ | 1.15 | 1.20 | 1.25 | V | sweep up |
| V15_IN Hysteresis Voltage | $\Delta VUVLO_{V15\_IN}$ | 50 | 100 | 150 | mV | sweep down |
| [POWER GOOD] | | | | | | |
| V3 POWER GOOD Voltage | $PG_{V3}$ | 2.700 | 2.850 | 3.000 | V | |
| V3AUX POWER GOOD Voltage | $PG_{V3AUX}$ | 2.700 | 2.850 | 3.000 | V | |
| V15 POWER GOOD Voltage | $PG_{V15}$ | 1.200 | 1.275 | 1.350 | V | |
| PERST# LOW Voltage | $VPERST\#_{Low}$ | - | 0.1 | 0.3 | V | $I_{PERST}$=0.5mA |
| PERST# HIGH Voltage | $VPERST\#_{HIGH}$ | 3.0 | - | - | V | |
| PERST# Delay Time | $T_{PERST\#}$ | 4 | - | 20 | ms | |
| PERST# assertion time | Tast | - | - | 500 | ns | |
| [OUTPUT RISE TIME] | | | | | | |
| V3_IN to V3 | $T_{V3}$ | 0.1 | - | 3 | ms | |
| V3AUX_IN to V3AUX | $T_{V3AUX}$ | 0.1 | - | 3 | ms | |
| V15_IN to V15 | $T_{V15}$ | 0.1 | - | 3 | ms | |

* Design target

●Reference data

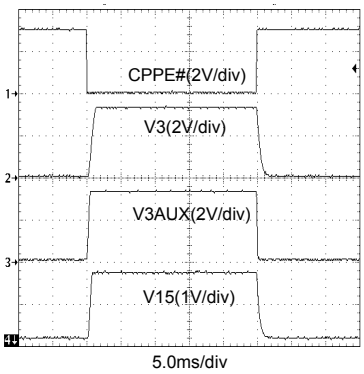



Fig.1 Card Assert/ De-assert (Active)

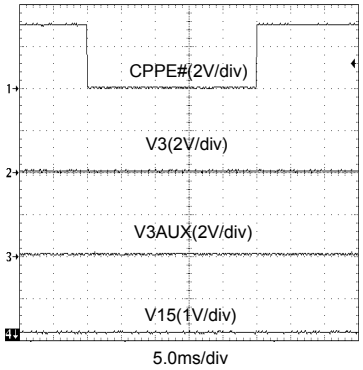



Fig.2 Card Assert/De-assert (Standby)

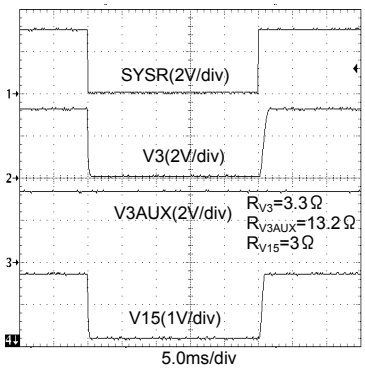



Fig.3 System Active⇔Standby ( Card Present)

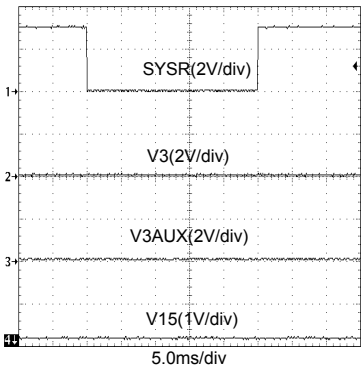



Fig.4 System Active⇔Standby (No Card)

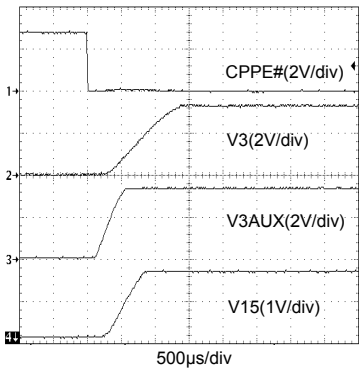



Fig.5 Wakeup Wave Form (Card Assert)

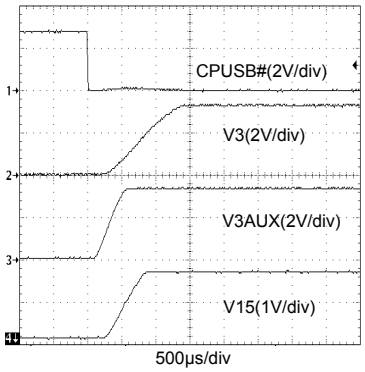



Fig.6 Wakeup Wave Form (USB2.0 Assert)

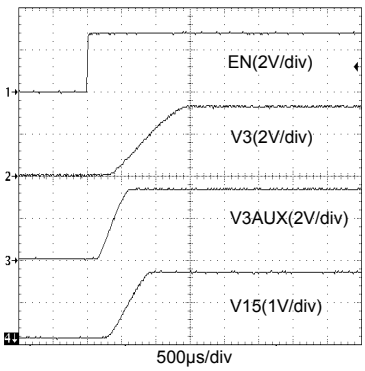



Fig.7 Wakeup Wave Form (Shut Down→Active)

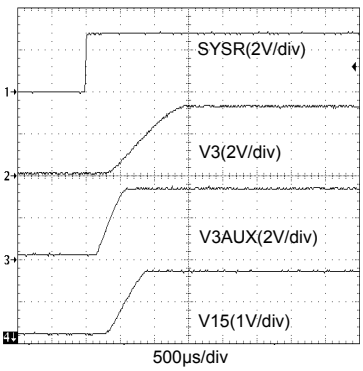



Fig.8 Wakeup Wave Form (Standby→Active)

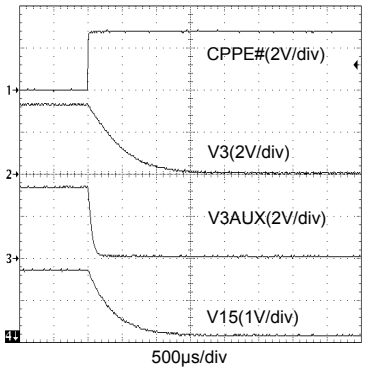



Fig.9 Power Down Wave Form (Card De-assert)

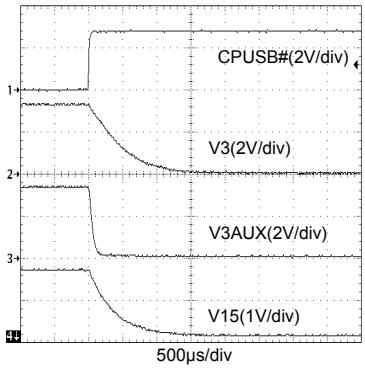



Fig.10 Power Down Wave Form (USB2.0 De-assert)

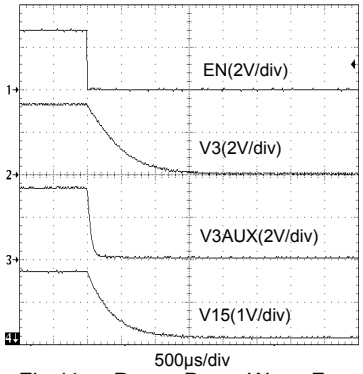



Fig.11 Power Down Wave Form (Active→Shut Down)

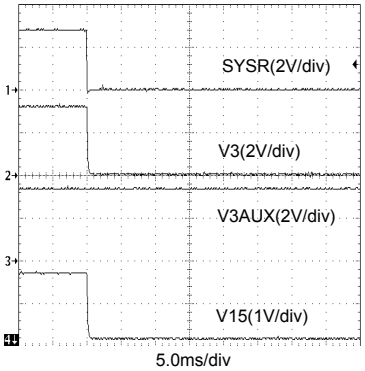



Fig.12 Power Down Wave Form (Active→Standby)

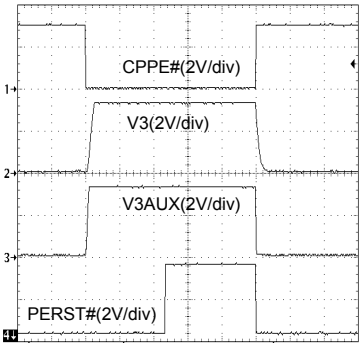



Fig.13 PERST# Wave Form
(Card Assert/ De-assert)

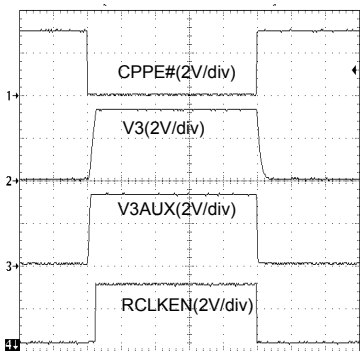



Fig.14 RCLKEN Wave Form
(Card Assert/ De-assert)

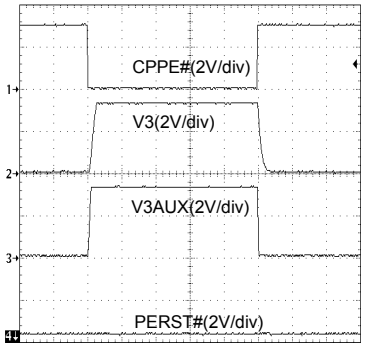



Fig.15 PERST# Wave Form
(USB2.0 Assert/ De-assert)

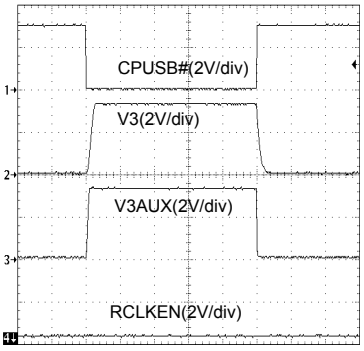



Fig.16 RCLKEN Wave Form
(USB2.0 Assert/ De-assert)

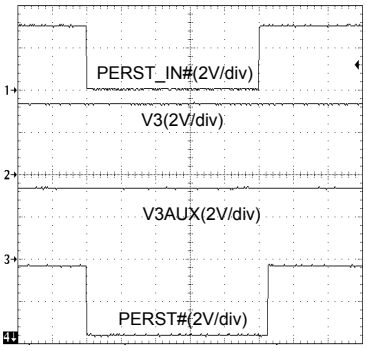



Fig.17 PERST# Wave Form
(PERST_IN# Input)

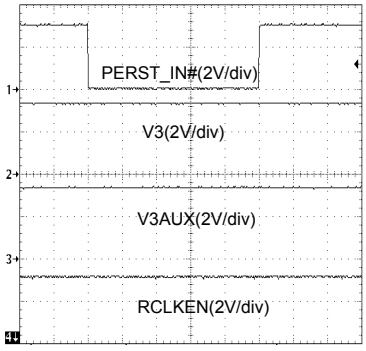



Fig.18 RCLKEN Wave Form
(PERST_IN# Input)

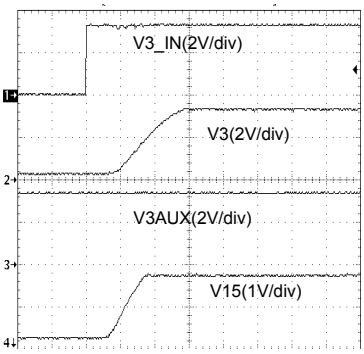



Fig.19 Output Voltage
(V3_IN:OFF→ON)

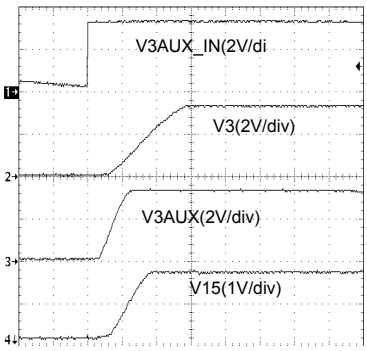



Fig.20 Output Voltage
(V3AUX_IN:OFF→ON)

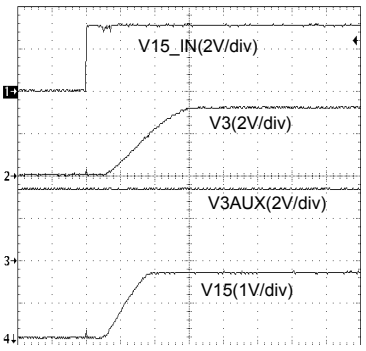



Fig.21 Output Voltage
(V15_IN:OFF→ON)

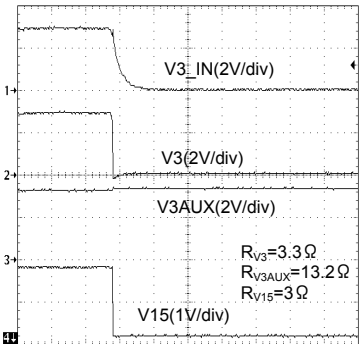



Fig.22 Output Voltage
(V3_IN:ON→OFF)

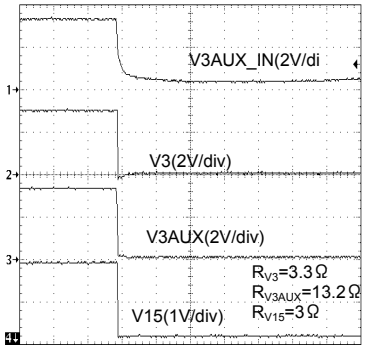



Fig.23 Output Voltage
(V3AUX_IN:ON→OFF)

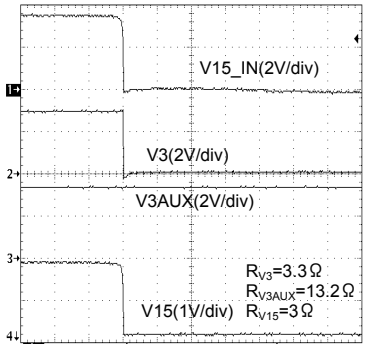
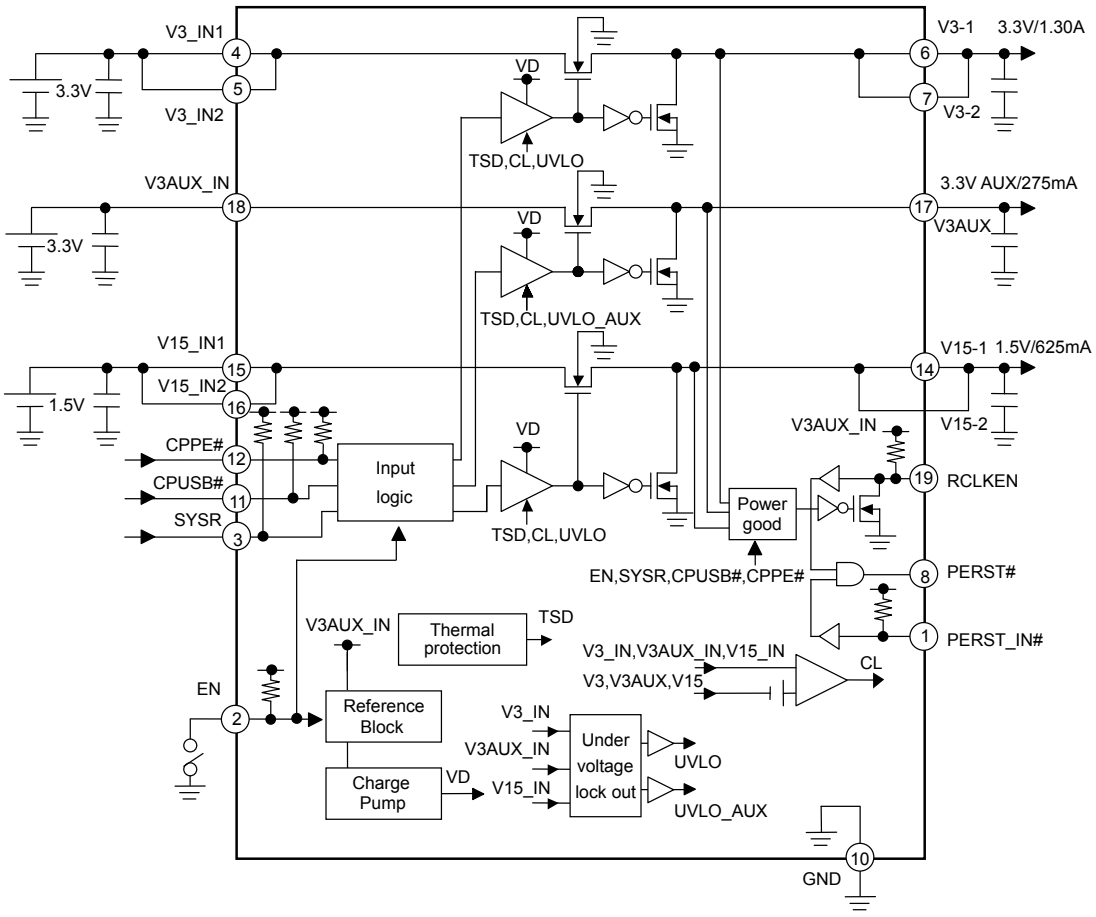
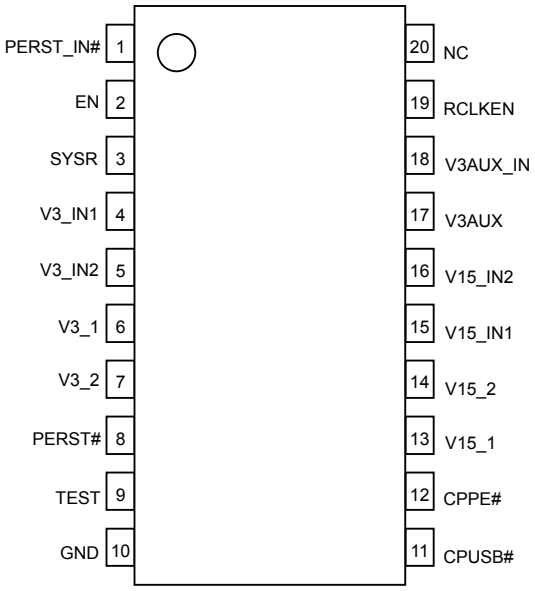



Fig.24 Output Voltage
(V15_IN:ON→OFF)

## ●Block Diagram




## ●PIN CONFIGRATION




SSOP-B20 Package

## ●PIN FUNCTION

| PIN No | PIN NAME | PIN FUNCTION |
|---|---|---|
| 1 | PERST_IN# | PERST# control input pin (SysReset#) |
| 2 | EN | Enable input pin |
| 3 | SYSR | Logic input pin |
| 4 | V3_IN1 | V3 input pin 1 |
| 5 | V3_IN2 | V3 input pin 2 |
| 6 | V3_1 | V3 output pin 1 |
| 7 | V3_2 | V3 output pin 2 |
| 8 | PERST# | Logic output pin |
| 9 | TEST | Test pin |
| 10 | GND | GND pin |
| 11 | CPUSB# | Logic input pin |
| 12 | CPPE# | Logic input pin |
| 13 | V15_1 | V15 output pin 1 |
| 14 | V15_2 | V15 output pin 2 |
| 15 | V15_IN1 | V15 input pin 1 |
| 16 | V15_IN2 | V15 input pin 2 |
| 17 | V3AUX | V3AUX output pin |
| 18 | V3AUX_IN | V3AUX input pin 1 |
| 19 | RCLKEN | Reference clock enable signal/ Power good signal (No delay) |
| 20 | NC | Non connection |

## ●Description of block operation

**EN**

With an input of 2.0 volts or higher, this terminal goes HIGH to activate the circuit, and goes LOW to deactivate the circuit (with the standby circuit current of 40 μA), It discharges each output and lowers output voltage when the input falls to 0.8 volts or less.

**V3_IN, V15_IN, and V3AUX_IN**

These are the input terminals for each channel of a 3ch switch. V3_IN and V15_IN terminals have two pins each, which should be short-circuited on the pc board with a thick conductor. A large current runs through these three terminals : (V3_IN: 1.35A; V3AUX_IN: 0.275 A; and V15_IN: 0.625 A). In order to lower the output impedance of the connected power supply, it is recommended that ceramic capacitors (with B-type characteristics or better) be provided between these terminals and the ground. Specifically, the capacitors should be on the order of 1 μF between V3_IN and GND, and between V15_IN and GND; and on the order of 0.1 μF between V3AUX_IN and GND.

**V3, V15, and V3AUX**

These are the output terminals for each switch. The V3 and V15 terminals have two pins each, which should be short-circuited on the PC board and connected to an ExpressCard connector with a thick conductor, as short as possible. In order to stabilize the output, it is recommended that ceramic capacitors (with B-type characteristics or better) be provided between these terminals and the ground. Specifically, the capacitors should be on the order of 10 μF between V3 and GND, and between V15 and GND; and on the order of 1 μF between V3AUX and GND.

**CPPE#**

This pin is used to find whether or not a PCI-Express signal compatible card is present. Turns to “High” level with an input of 2.0 volts or higher, which means that no card is provided, while it turns to “Low” level when the input is lowered to 0.8 volts or less, which means that a card is provided. Controls the ON/OFF, switch selecting the proper mode based on the status of the system.
Pull up resistance (100kΩ～200kΩ) is built into, so the number of components is reduced.

**CPUSB#**

This pin is used to find whether or not a USB2.0 signal compatible card is present. Turns to “High” level with an input of 2.0 volts or higher, which means that no card is provided, while it turns to “Low” level when the input is lowered to 0.8 volts or less, which means that a card is provided. Controls the ON/OFF switch, selecting the proper mode based on the system status.
Pull up resistance (100kΩ～200kΩ) is built into, so the number of components is reduced.

**SYSR**

This pin is used to detect the system status. Turns to “High” level with an input of 2.0 volts or higher, which means that the system is activated, while it turns to “Low” level when the input is lowered to 0.8 volts or less, which means that the system is on standby.

**PERST_IN#**

This pin is used to control the reset signal (PERST#) to a card from the system side. (Also referred to as “SysReset#” by PCMCIA.) Turns to “High” level with an input of 2.0 volts or higher, and sets PERST# to “High” AND with a “Power Good” output. Turns to “Low” level and sets PERST# to “Low” when the input falls to 0.8 volts or less.

**PERST#**

This pin is used to send a reset signal to a PCI-Express compatible card. Reset status is determined by the outputs, PERST_IN#, CPPE# system status, and EN on/off status. Turns to “High” level and activates the PCI-Express compatible card only if each output is within the “Power Good” threshold, with the card inserted and PERST_IN# turned to “High” level.

**RCLKEN**

This pin is used to send an enable signal to the reference clock. Activation status is determined by the outputs, CPPE# system status, and EN on/off status. Turns to “High” level and activates the reference clock PLL only if each output is within the “Power Good” threshold, with the card kept inserted.

**TEST**

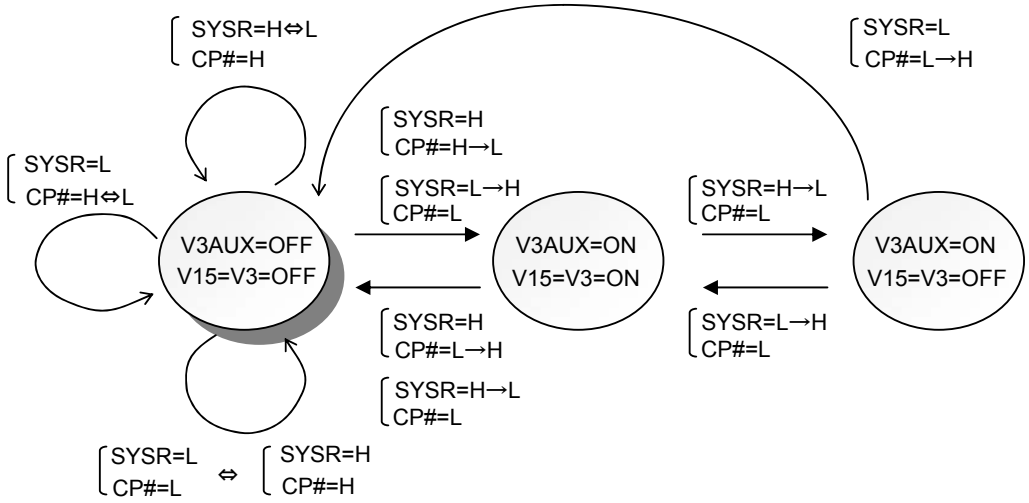
This pin is used to test, which should be short-circuited to the GND. When it is short-circuited to V3AUX_IN, UVLO (V3_IN, V15_IN) turns OFF.

●**Timing Chart**

Power ON/OFF Status of ExpressCard™

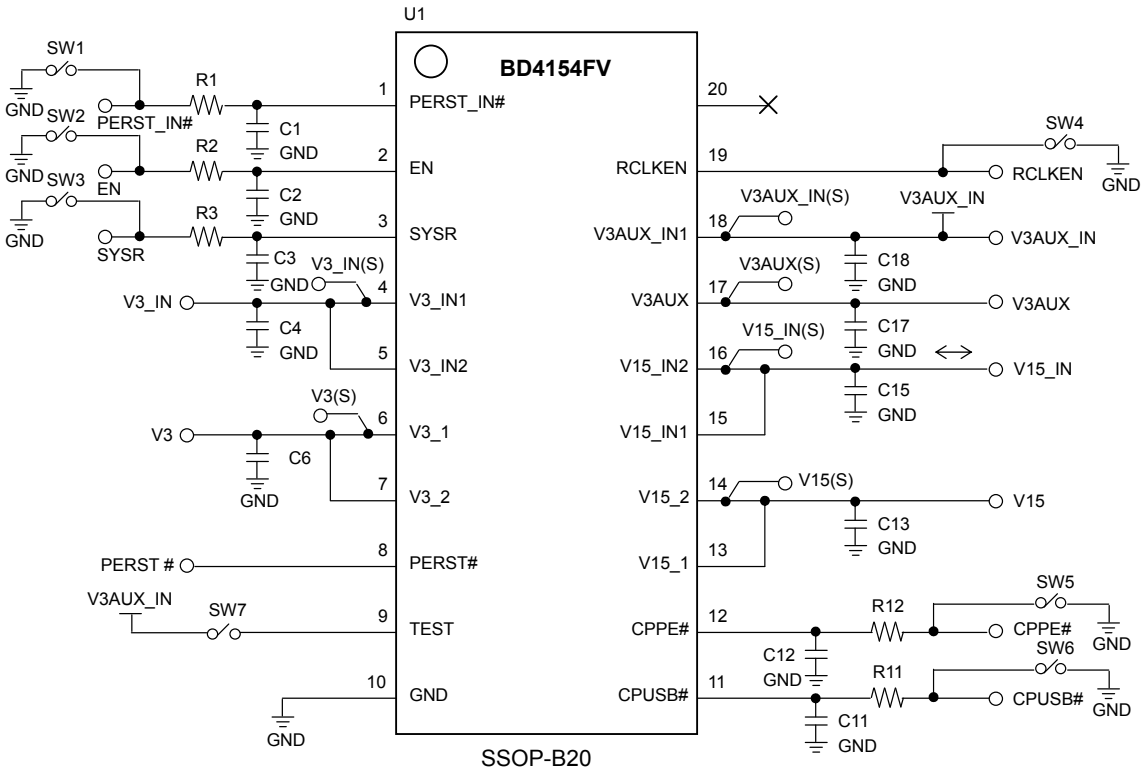
| System Status | | ExpressCard™ Module Status | Power Switch Status | |
|---|---|---|---|---|
| Primary | Auxiliary | | Primary(+3.3V and +1.5V) | Auxiliary(3.3V Aux) |
| OFF | OFF | Don't care | OFF | OFF |
| ON | ON | De-asserted | OFF | OFF |
| | | Asserted | ON | ON |
| ON | ON | De-asserted | OFF | OFF |
| | | Asserted Before This | OFF | ON |
| | | Asserted After This | OFF | OFF |

ExpressCard™ States Transition Diagram




| System Status | | Card Status | |
|---|---|---|---|
| Stand-by Status | :SYSR=L | Card Asserted Status | :CP#=L |
| ON Status | :SYSR=H | Card De-asserted Status | :CP#=H |
| From ON to Stand-by Status | :SYSR=H→L | From De-asserted to Asserted Status | :CP#=H→L |
| From Stand-by to ON Status | :SYSR=L→H | From Asserted to De-asserted Status | :CP#=L→H |

## BD4154FV Evaluation Board

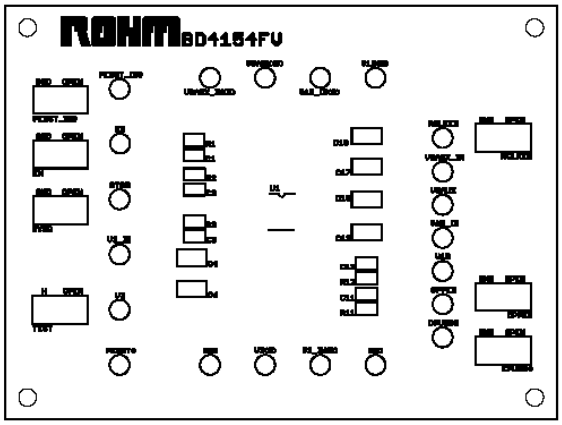



## BD4154FV Evaluation Board Application Components

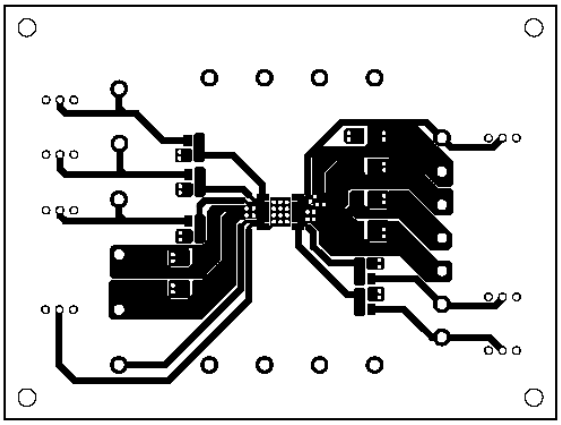
| Part No | Value | Company | Part Name |
|---|---|---|---|
| R1 | 0Ω | ROHM | MCR03series |
| R2 | 0Ω | ROHM | MCR03series |
| R3 | 0Ω | ROHM | MCR03series |
| R11 | 0Ω | ROHM | MCR03series |
| R12 | 0Ω | ROHM | MCR03series |
| C1 | - | - | - |
| C2 | - | - | - |
| C3 | - | - | - |
| C4 | 1μF | murata | GMR21 series |
| C6 | 10μF | murata | GMR21 series |
| C11 | - | - | - |
| C12 | - | - | - |
| C13 | 10μF | murata | GMR21 series |
| C15 | 1μF | murata | GMR21 series |
| C17 | 1μF | murata | GMR21 series |
| C18 | 0.1μF | murata | GMR18 series |

## BD4154FV Evaluation Board Layout

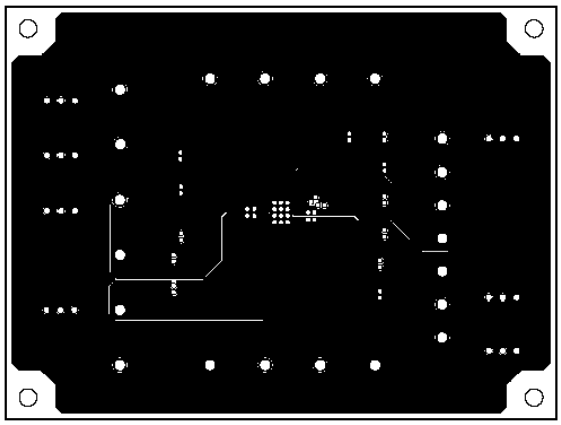
Silk Screen



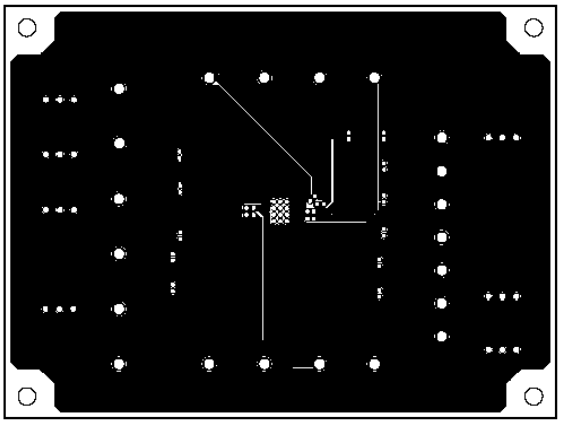

TOP Layer



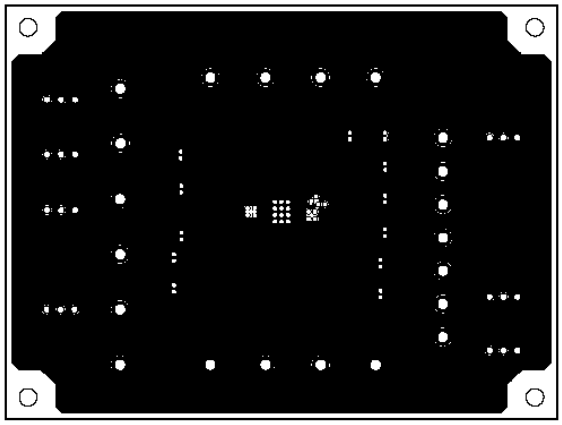
Mid Layer 1



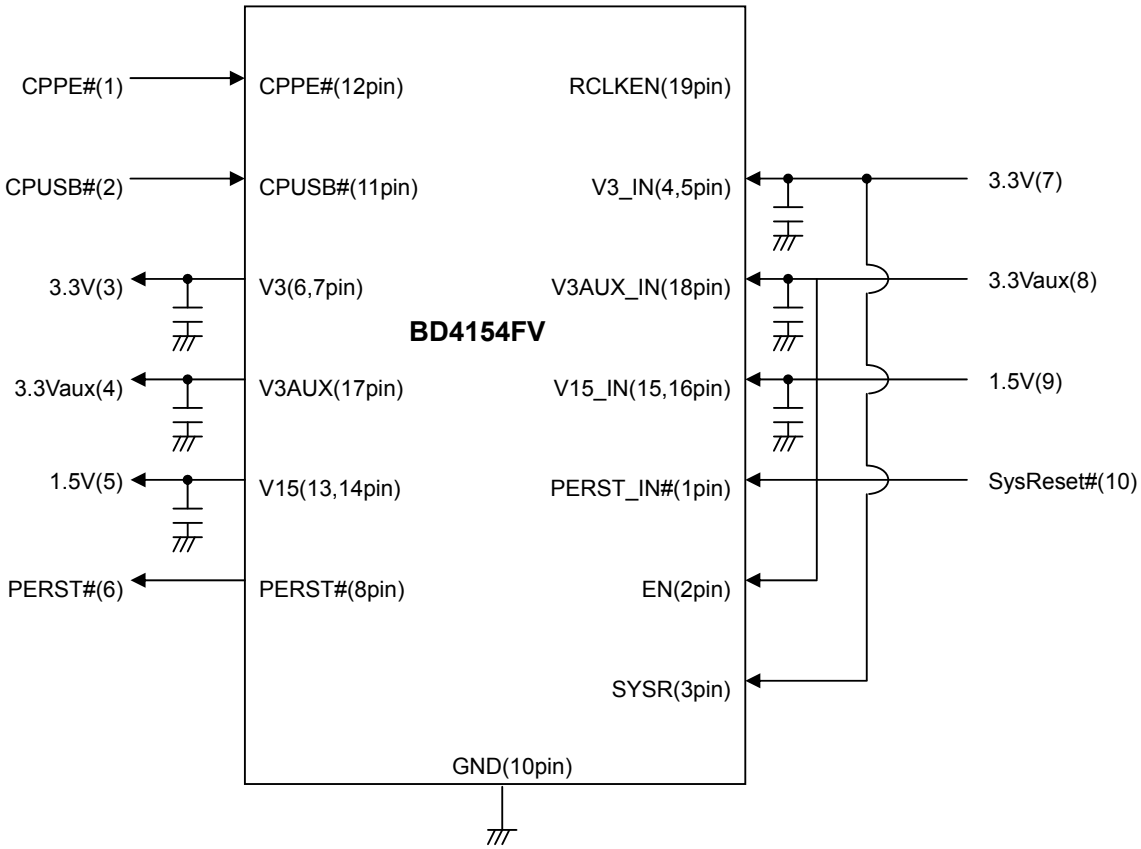
Mid Layer 2



Bottom Layer



●**Application Circuit (Circuit for ExpressCard™ Compliance Checklist)**




●**Heat loss**

Thermal design should allow the device to operate within the following conditions. Note that the temperatures listed are the allowed temperature limits. Thermal design should allow sufficient margin from these limits.

1. Ambient temperature Ta can be no higher than 100°C.
2. Chip junction temperature Tj can be no higher more than 150°C.

Chip junction temperature Tj can be determined as follows:

①Chip junction temperature Tj is calculated from IC surface temperature TC under actual application conditions:

Tj=TC+θj-cxW

＜Reference value＞

θj-c:SSOP-B20 35□/W

②Chip junction temperature Tj is calculated from ambient temperature Ta:

Tj=TC+ *θ* j-axW

＜Reference value＞

*θ* j-a:SSOP-B20 250℃/W (IC only)

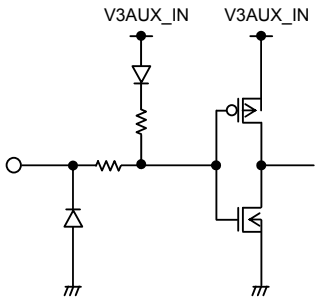
153.8℃/W Single-layer substrate

(substrate surface copper foil area: less than 3%)

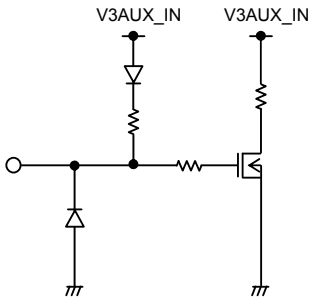
Most of heat loss in the BD4154FV occurs at the output switch. The power lost is determined by multiplying the on-resistance by the square of output current of each switch.

●**Equivalent Circuit**

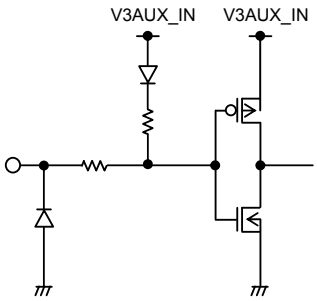
1pin<PERST_IN#>



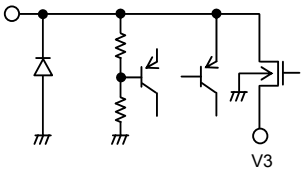

2pin<EN>



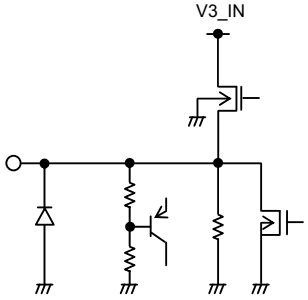

3pin<SYSR>



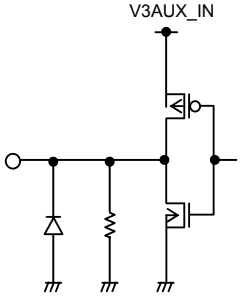

4,5pin<V3_IN1,V3_IN2>



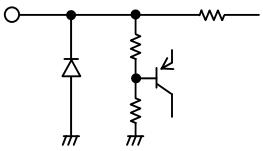

6,7pin<V3_1,V3_2>



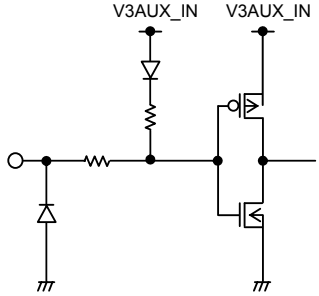

8pin<PERST#>



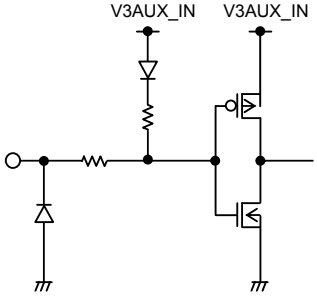

9pin<TEST>



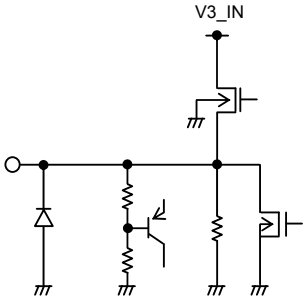
11pin<CPUSB#>



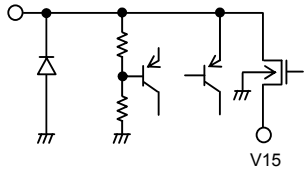

12pin<CPPE#>



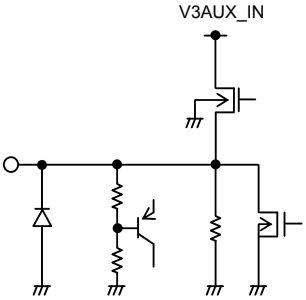

13,14pin<V15_1,V15_2>



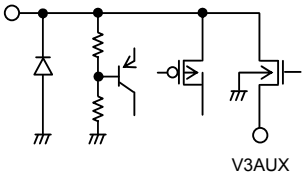

15,16pin<V15_IN1,V15_IN2>



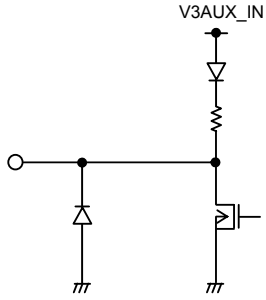

17pin<V3AUX>




18pin<V3AUX_IN>




19pin<RCLKEN >



**●Notes for Use**

1.Absolute maximum ratings

Although quality is rigorously controlled, the device may be destroyed when applied voltage, operating temperature, etc. exceeds its absolute maximum rating. Because the source (short mode or open mode) cannot be identified once the IC is destroyed, it is important to take physical safety measures such as fusing when implementing any special mode that operates in excess of absolute rating limits.

2.Thermal design

Consider allowable loss (Pd) under actual operating conditions and provide sufficient margin in the thermal design.

3.Terminal-to-terminal short-circuit and mis-mounting

When the mounting the IC to a printed circuit board, take utmost care to assure the position and orientation of the IC are correct. In the event that the IC is mounted erroneously, it may be destroyed. The IC may also be destroyed when a short-circuit is caused by foreign matter introduced into the clearance between outputs, or between an output and power-GND.

4.Operation in strong electromagnetic fields

Using the IC in strong electromagnetic fields may cause malfunctions. Exercise caution in respect to electromagnetic fields.

5.Built-in thermal shutdown protection circuit

This IC incorporates a thermal shutdown protection circuit (TSD circuit). The working temperature is 175°C (standard value) with a -15°C (standard value) hysteresis width. When the IC chip temperature rises the TSD circuit is activated, while the output terminal is brought to the OFF state. The built-in TSD circuit is intended exclusively to shut down the IC in a thermal runaway event, and is not intended to protect the IC or guarantee performance in these conditions. Therefore, do not operate the IC after with the expectation of continued use or subsequent operation once this circuit is activated.

6.Capacitor across output and GND

When a large capacitor is connected across the output and GND, and the V3AUX_IN is short-circuited with 0V or GND for any reason, current charged in the capacitor flows into the output and may destroy the IC. Therefore, use a capacitor smaller than 1000 µF between the output and GND.

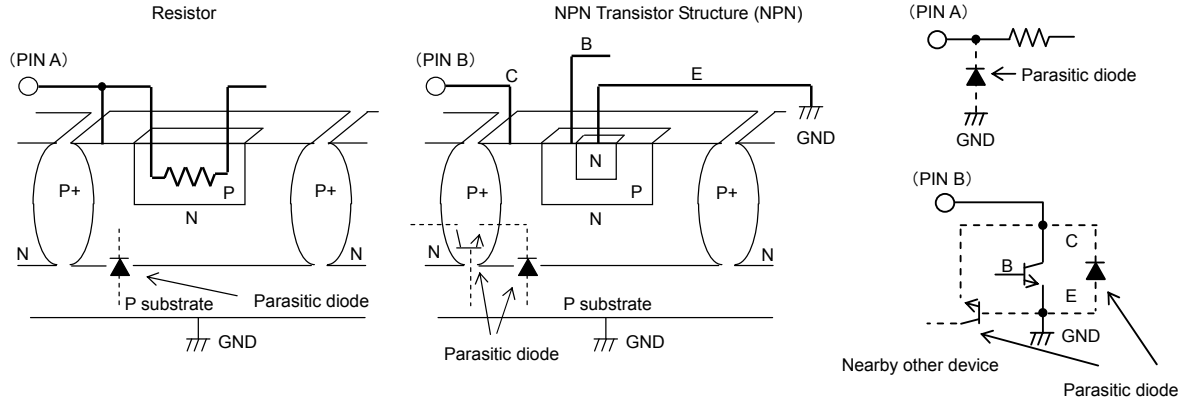
7.Set substrate inspection

Connecting a low-impedance capacitor to a pin when running an inspection with a set substrate may produce stress on the IC. Therefore, be certain to discharge electricity at each process of the operation. To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handling, transfer and storage operations. Before attempting to connect the set substrate to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing the substrate from the test setup.

8.IC terminal input

This integrated circuit is a monolithic IC, with P substrate and $P^+$ isolation between elements.

The P layer and N layer of each element form a, PN junction. When the potential relation is GND>terminal A>terminal B, the PN junction works as a diode, and when terminal B>GND terminal A, the PN junction operates as a parasitic transistor. Parasitic elements inevitably form, due to the nature of the IC construction. The operation of the parasitic element gives rise to mutual interference between circuits and results in malfunction, and eventually, breakdown. Consequently, take utmost care not to use the IC in a way that would cause the parasitic element to actively operate, such as applying voltage lower than GND (P substrate) to the input terminal.

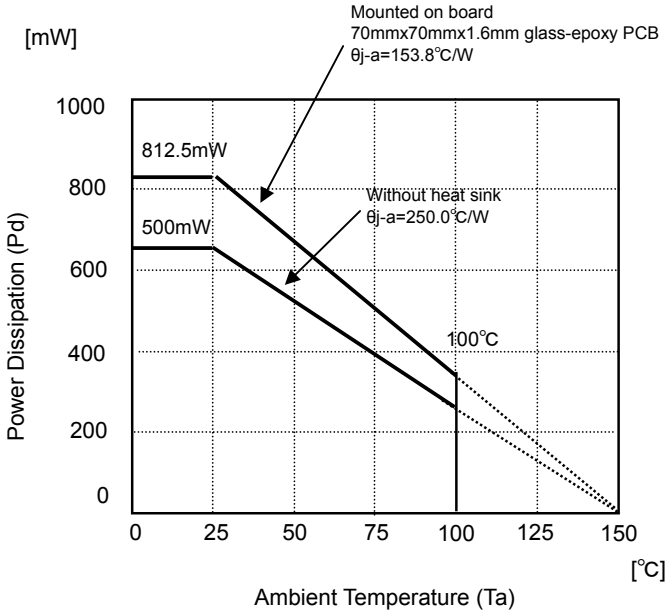



9. GND wiring pattern

If both a small signal GND and a high current GND are present, it is recommended that the patterns for the high current GND and the small signal GND be separated. Proper grounding to the reference point of the set should also be provided. In this way, the small signal GND voltage will by unaffected by the change in voltage stemming from the pattern wiring resistance and the high current. Also, pay special attention to avoid undesirable wiring pattern fluctuations in any externally connected GND component.

10. Electrical characteristics
    The electrical characteristics in the Specifications may vary, depending on ambient temperature, power supply voltage, circuit(s) externally applied, and/or other conditions. Therefore, please check all such factors, including transient characteristics, that could affect the electrical characteristics.
11. Capacitors applied to input terminals
    The capacitors applied to the input terminals (V3_IN, V3AUX_IN and V15_IN) are used to lower the output impedance of the connected power supply. An increase in the output impedance of the power supply may result in destabilization of input voltages (V3_IN, V3AUX_IN and V15_IN). It is recommended that a low-ESR capacitor be used, with a lower temperature coefficient (change in capacitance vs. change in temperature), Recommended capacitors are on the order of 0.1 μF for V3AUX_IN, and1 μF for V3_IN and V15_IN. However, they must be thoroughly checked at the temperature and with the load range expected in actual use, because capacitor selection depends to a significant degree on the characteristics of the input power supply to be used and the conductor pattern of the PC board.
12. Capacitors applied to output terminals
    Capacitors for the output terminals (V3, V3_AUX, and V15), should be connected between each of the output terminals and GND. A low-ESR, low temperature coefficient output capacitor is recommended-on the order of 1 μF for V3 and V15 terminals, and 1μF less for V3_AUX. However, they must be thoroughly checked at the temperature and with the load range expected in actual use, because capacitor selection depends to a significant degree on the temperature and the load conditions.
13. Not of a radiation-resistant design.
14. Allowable loss (Pd)
    With respect to the allowable loss, please refer to the thermal derating characteristics shown in the Exhibit, which serves as a rule of thumb. When the system design causes the IC to operate in excess of the allowable loss, chip temperature will rise, reducing the current capacity and decreasing other basic IC functionality. Therefore, design should always enable IC operation within the allowable loss only.
15. Operating range
    Basic circuit functions and operations are warranted within the specified operating range the working ambient temperature range. Although reference values for electrical characteristics are not warranted, no rapid or extraordinary changes in these characteristics are expected, provided operation is within the normal operating and temperature range.
16. The applied circuit example diagrams presented here are recommended configurations. However, actual design depends on IC characteristics, which should be confirmed before operation. Also, note that modifying external circuits may impact static, noise and other IC characteristics, including transient characteristics. Be sure to allow sufficient margin in the design to accommodate these factors.
17. Wiring to the input terminals (V3 IN, V3AUX IN, and V15 IN) and output terminals (V3, V3AUX and V15) of the built-in FET should be carried out with special care. Using unnecessarily long and/or thin conductors may decrease output voltage and degrade other characteristics.
18. Heatsink
    The heatsink is connected to the SUB, which should be short-circuited to the GND. Proper heatsink soldering to the PC board should enable lower thermal resistance.

**●Power Dissipation**



●**Ordering part number**

| B | D | 4 | 1 | 5 | 4 | F | V | - | E | 2 |
|---|---|---|---|---|---|---|---|---|---|---|

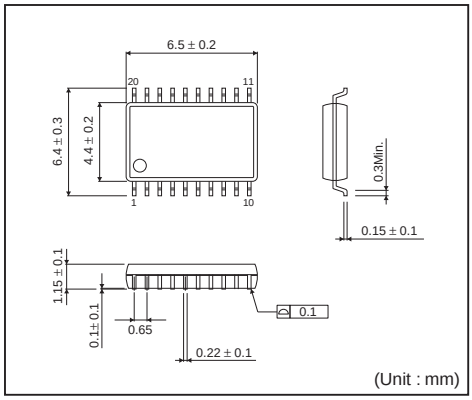
Part Number: BD

Part Number: 4154

Package: FV : SSOP-B20

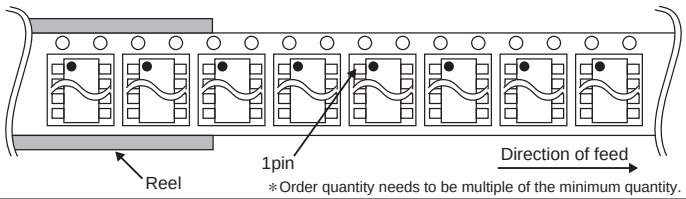
Packaging and forming specification: E2: Embossed tape and reel (SSOP-B20)

**SSOP-B20**




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.

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ROHM SEMICONDUCTOR

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