

### General Description

The MIC23250 is a high efficiency 4MHz dual 400mA synchronous buck regulator with Hyper Light Load™. Hyper Light Load™ provides all the advantages of standard light load modes, such as low quiescent current and high efficiency but also allows the use of very small output capacitors to maintain low output ripple voltage throughout the entire load range. This benefit is not possible with other light load mode types as they trade off control speed for low standby currents. With Hyper Light Load™, the output capacitor can be reduced by up to a factor of 20 saving cost and valuable board space. The tiny package (2mm x 2mm Thin MLF®) of MIC23250 also saves crucial board space by using only six external components while regulating two independent outputs up to 400mA each.

The device is designed for use with a 1µH inductor and a 4.7µF output capacitor that enables a sub-1mm height.

The MIC23250 has a very low quiescent current of 35µA and can achieve over 85% efficiency at 1mA. At higher loads the MIC23250 provides a constant switching frequency around 4MHz while providing peak efficiencies up to 94%.

The MIC23250 fixed output voltage option is available in a 10-pin 2mm x 2mm Thin MLF® with a junction operating range from -40°C to +125°C. The adjustable output voltage option will soon be available in Q2/Q3 2008.

Data sheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

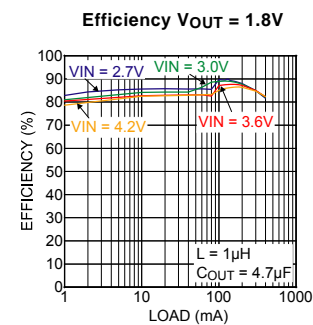
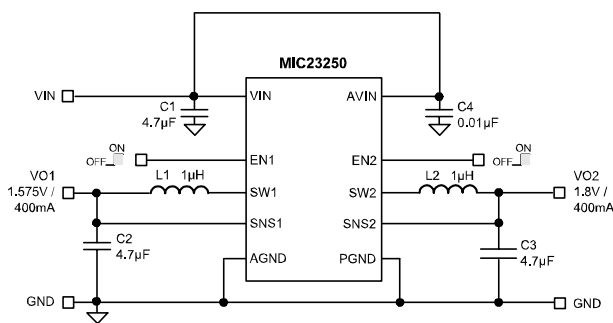
### Features

- Input voltage range: 2.7V to 5.5V
- Dual output current 400mA/400mA
- Hyper Light Load™ mode
  - 35µA dual quiescent current
  - 1µH inductor with a 4.7µF capacitor
- 4MHz in PWM operation
- Ultra fast transient response
- Low voltage output ripple
  - 20mVpp in Hyper Light Load™ mode
  - 3mV output voltage ripple in full PWM mode
- Up to 94% peak efficiency and 85% efficiency at 1mA
- Fully integrated MOSFET switches
- Micropower shutdown
- Thermal shutdown and current limit protection
- Fixed output: 10-pin 2mm x 2mm Thin MLF®
- Adjustable output: 12-pin 2.5mm x 2.5mm Thin MLF® (Available in Q2/Q3 2008)
- -40°C to +125°C junction temperature range

### Applications

- Mobile handsets
- Portable media players
- Portable navigation devices (GPS)
- WiFi/WiMax/WiBro modules
- Digital cameras
- Wireless LAN cards
- USB Powered Devices

### Typical Application



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MLF and MicroLeadFrame are registered trademarks of Amkor Technology, Inc.

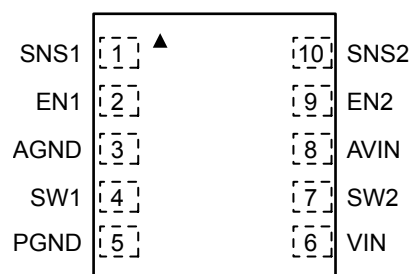
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## Ordering Information

Part Number	Marking	Nominal Output Voltage 1	Nominal Output Voltage 2	Junction Temp. Range	Package	Lead Finish
MIC23250-GFHMT	WV1	1.575V	1.8V	-40° to +125°C	10-Pin 2mm x 2mm Thin MLF <sup>®</sup>	Pb-Free
MIC23250-G4YMT	WV5	1.8V	1.2V	-40° to +125°C	10-Pin 2mm x 2mm Thin MLF <sup>®</sup>	Pb-Free
MIC23250-C4YMT	WV2	1.0V	1.2V	-40° to +125°C	10-Pin 2mm x 2mm Thin MLF <sup>®</sup>	Pb-Free
MIC23250-3BYMT	WV3	1.1V	0.9V	-40° to +125°C	10-Pin 2mm x 2mm Thin MLF <sup>®</sup>	Pb-Free
MIC23250-W4YMT	WV4	1.6V	1.2V	-40° to +125°C	10-Pin 2mm x 2mm Thin MLF <sup>®</sup>	Pb-Free
MIC23250-Adj*	TBD	ADJ	ADJ	-40° to +125°C	12-Pin 2.5mm x 2.5mm Thin MLF <sup>®</sup>	Pb-Free

Note: \* Available Q2/Q3 2008

## Pin Configuration



10-Pin 2mm x 2mm Thin MLF<sup>®</sup> (MT)  
(Top View)

## Pin Description

Pin Number	Pin Name	Pin Name
1	SNS1	Sense 1 (Input): Error amplifier input. Connect to feedback resistor network to set output 1 voltage.
2	EN1	Enable 1 (Input): Logic low will shut down output 1. Logic high powers up output 1. Do not leave unconnected.
3	AGND	Analog Ground. Must be connected externally to PGND.
4	SW1	Switch Node 1 (Output): Internal power MOSFET output.
5	PGND	Power Ground.
6	VIN	Supply Voltage (Power Input): Requires close bypass capacitor to PGND.
7	SW2	Switch Node 2 (Output): Internal power MOSFET output.
8	AVIN	Supply Voltage (Power Input): Analog control circuitry. Connect to VIN.
9	EN2	Enable 2 (Input): Logic low will shut down output 2. Logic high powers up output 2. Do not leave unconnected.
10	SNS2	Sense 2 (Input): Error amplifier input. Connect to feedback resistor network to set output 2 voltage.

**Absolute Maximum Ratings<sup>(1)</sup>**

Supply Voltage ( $V_{IN}$ ).....	6V
Output Switch Voltage ( $V_{SW}$ ).....	6V
Logic Input Voltage ( $V_{EN}$ ) .....	-0.3V to $V_{IN}$
Storage Temperature Range ( $T_s$ ).....	-65°C to +150°C
ESD Rating <sup>(3)</sup> .....	2kV

**Operating Ratings<sup>(2)</sup>**

Supply Voltage ( $V_{IN}$ ).....	2.7V to 5.5V
Logic Input Voltage ( $V_{EN}$ ) .....	-0.3V to $V_{IN}$
Junction Temperature ( $T_J$ ) .....	-40°C ≤ $T_J$ ≤ +125°C
Thermal Resistance	
2mm x 2mm Thin MLF <sup>®</sup> -10 ( $\theta_{JA}$ ).....	70°C/W

**Electrical Characteristics<sup>(4)</sup>**

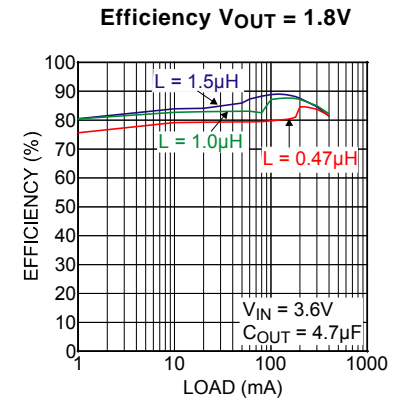
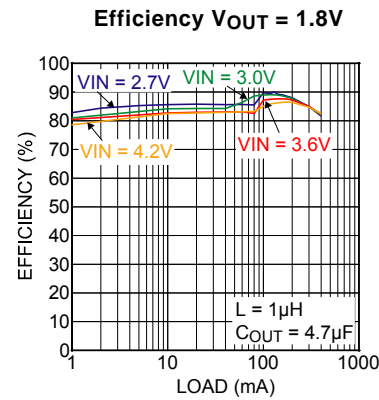
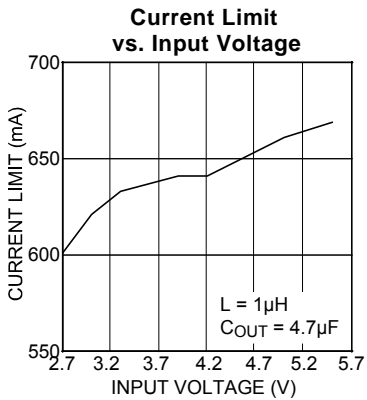
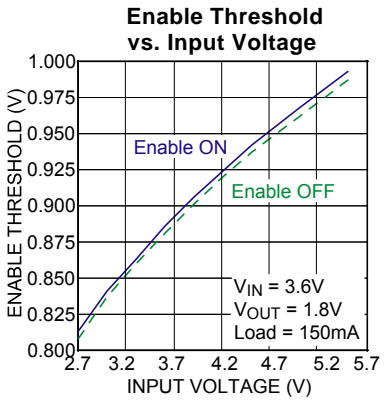
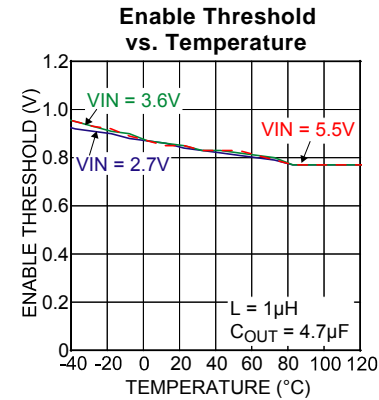
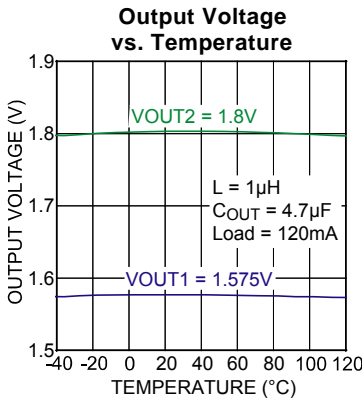
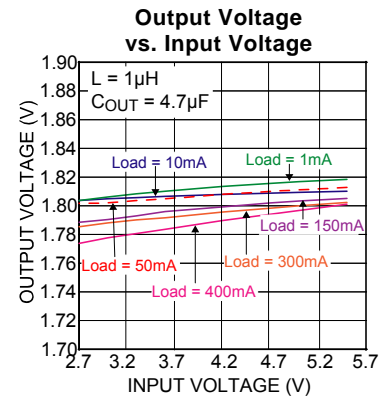
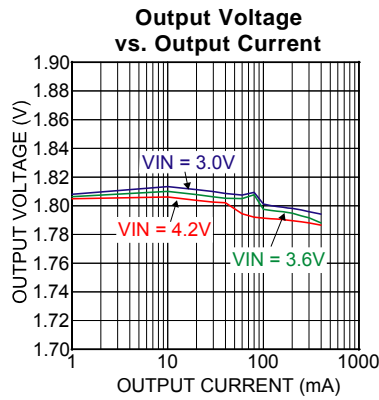
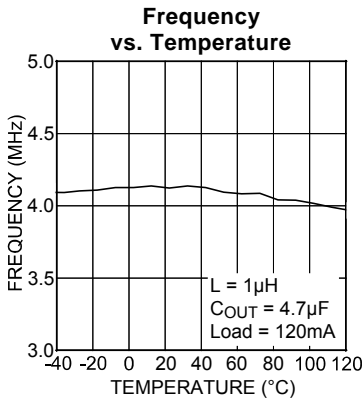
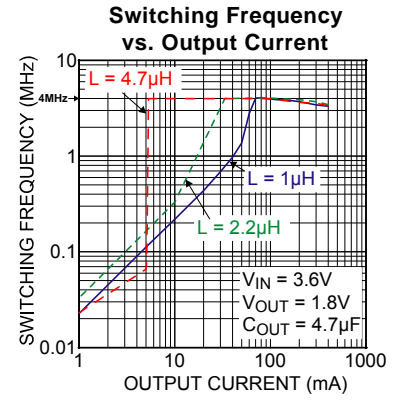
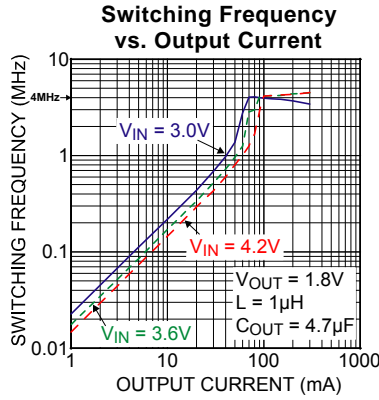
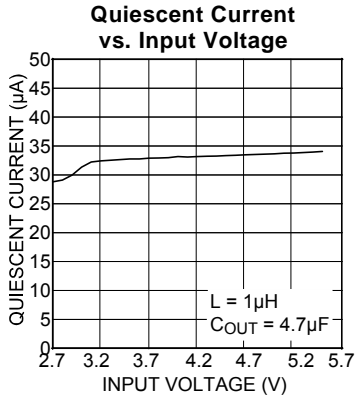
$T_A = 25^\circ\text{C}$  with  $V_{IN} = V_{EN} = 3.6\text{V}$ ;  $L = 1\mu\text{H}$ ;  $C_{OUT} = 4.7\mu\text{F}$ ;  $I_{OUT} = 20\text{mA}$ ; only one channel power is enabled, unless otherwise specified. **Bold** values indicate  $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ .

Parameter	Condition	Min	Typ	Max	Units
Supply Voltage Range		<b>2.7</b>		5.5	V
Under-Voltage Lockout Threshold	(turn-on)	2.45	2.55	2.65	V
UVLO Hysteresis			60		mV
Quiescent Current, Hyper LL mode	$V_{OUT1,2}$ (both Enabled), $I_{OUT1,2} = 0\text{mA}$ , $SNS1,2 > 1.2 * V_{OUT1,2}$ Nominal		35	50	$\mu\text{A}$
Shutdown Current	$V_{EN1,2} = 0\text{V}$ ; $V_{IN} = 5.5\text{V}$		0.01	<b>4</b>	$\mu\text{A}$
Output Voltage Accuracy	$V_{IN} = 3.6\text{V}$ , $I_{LOAD} = 20\text{mA}$	<b>-2.5</b>		<b>+2.5</b>	%
Current Limit in PWM Mode	$SNS = 0.9 * V_{OUT\text{NOM}}$	<b>0.410</b>	0.65	<b>1</b>	A
Output Voltage Line Regulation	$V_{IN} = 3.0\text{V}$ to $5.5\text{V}$ , $I_{LOAD} = 20\text{mA}$		0.4		%/V
Output Voltage Load Regulation	$20\text{mA} < I_{LOAD} < 400\text{mA}$ , $V_{IN} = 3.6\text{V}$		0.5		%
Maximum Duty Cycle	$SNS \leq V_{NOM}$ , $V_{OUT} = 1.8\text{V}$ , $V_{IN} = 2.7\text{V}$	<b>80</b>	86		%
PWM Switch ON-Resistance	$I_{SW} = 100\text{mA}$ PMOS		0.6		$\Omega$
	$I_{SW} = -100\text{mA}$ NMOS		0.8		$\Omega$
Frequency	$I_{LOAD} = 120\text{mA}$	<b>3.4</b>	4	<b>4.6</b>	MHz
Soft Start Time	$V_{OUT} = 90\%$		260		$\mu\text{s}$
Enable Threshold		<b>0.5</b>	0.8	<b>1.2</b>	V
Enable Input Current			0.1	<b>2</b>	$\mu\text{A}$
Over-temperature Shutdown			160		$^\circ\text{C}$
Over-temperature Shutdown Hysteresis			40		$^\circ\text{C}$

**Notes:**

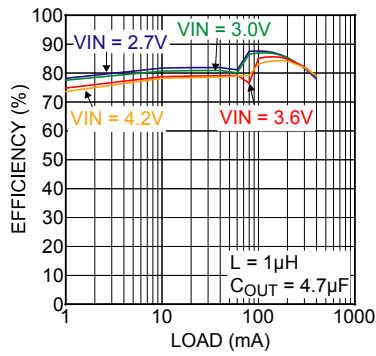
- Exceeding the absolute maximum rating may damage the device.
- The device is not guaranteed to function outside its operating rating.
- Devices are ESD sensitive. Handling precautions recommended. Human body model: 1.5k $\Omega$  in series with 100pF.
- Specification for packaged product only.

# Typical Characteristics

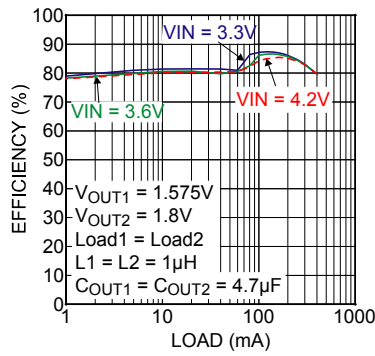


## Typical Characteristics (Continued)

Efficiency  $V_{OUT} = 1.575V$

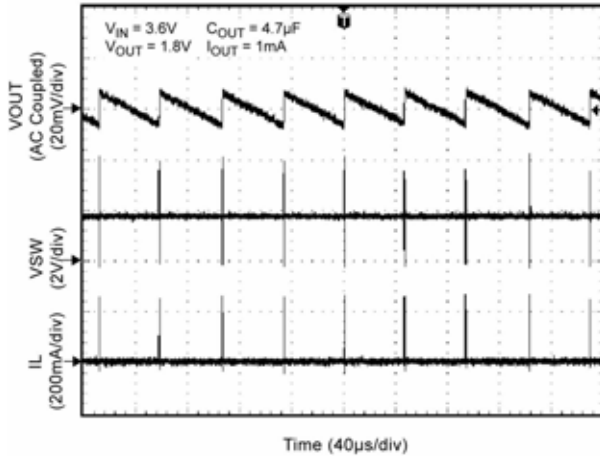


Dual Output Efficiency

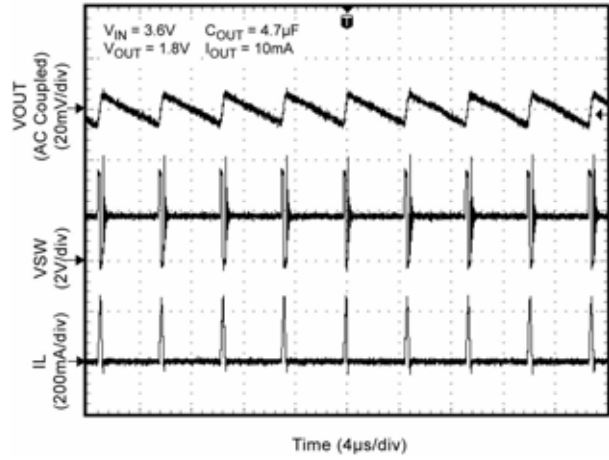


## Functional Characteristics

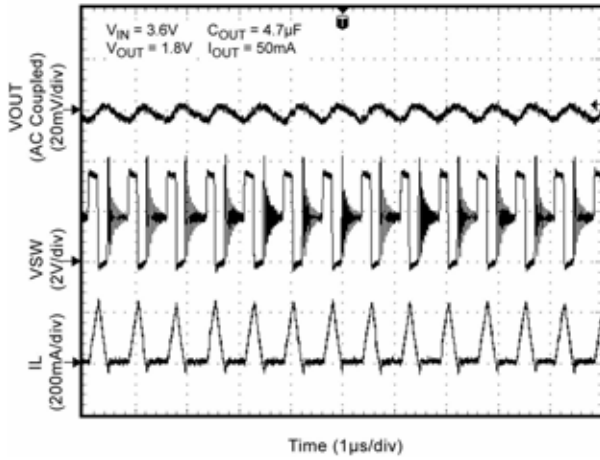
Switching Waveform - Discontinuous Mode



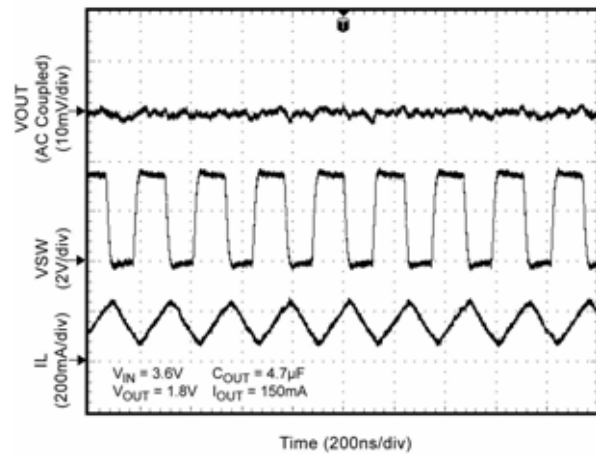
Switching Waveform - Discontinuous Mode



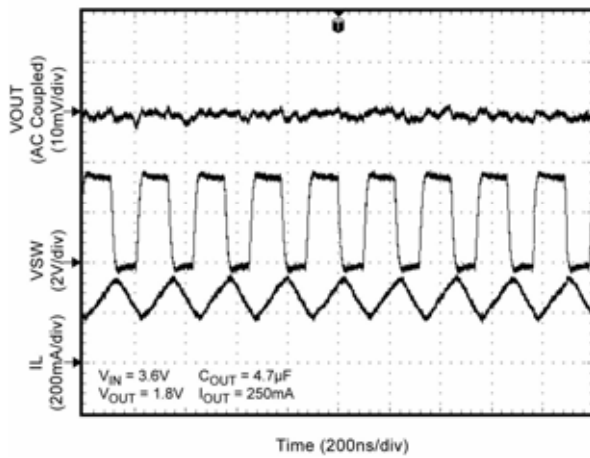
Switching Waveform - Discontinuous Mode



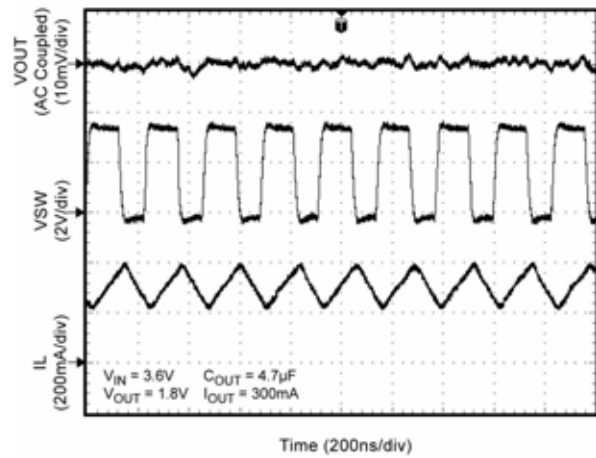
Switching Waveform - Continuous Mode



Switching Waveform - Continuous Mode

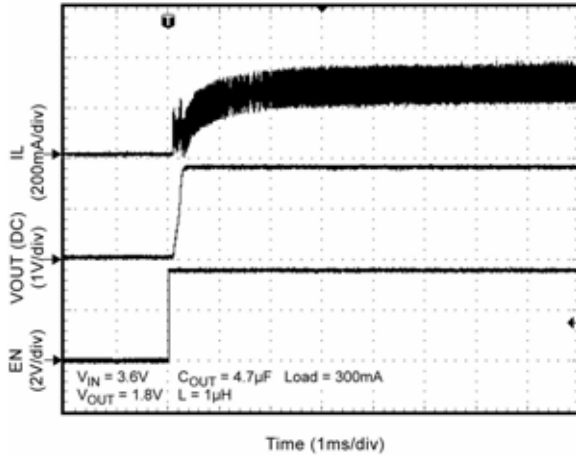


Switching Waveform - Continuous Mode

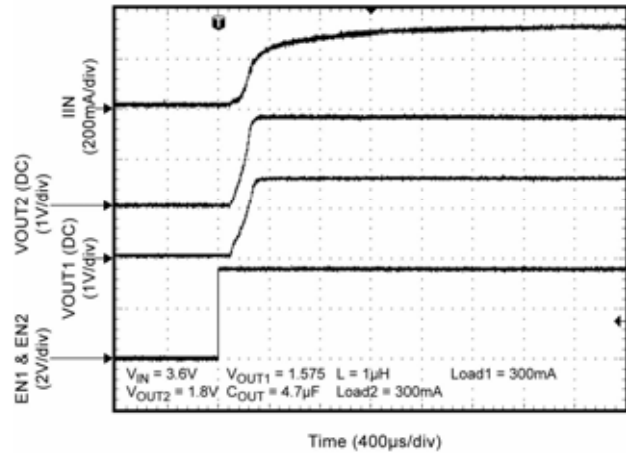


## Functional Characteristics (Continued)

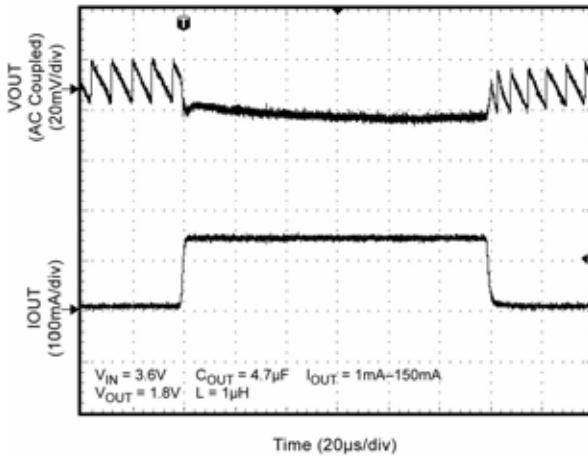
Start-Up Waveform



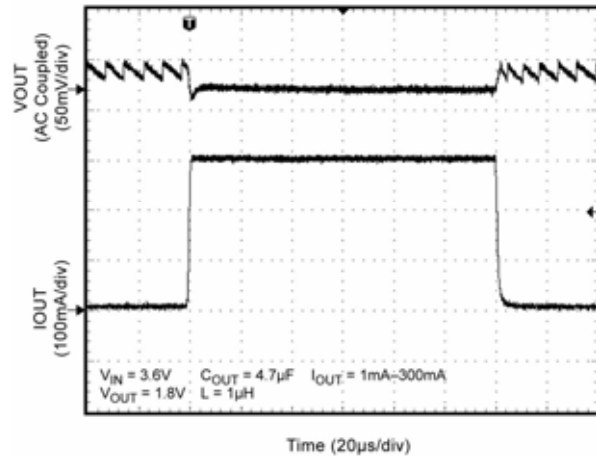
Start-Up Waveform



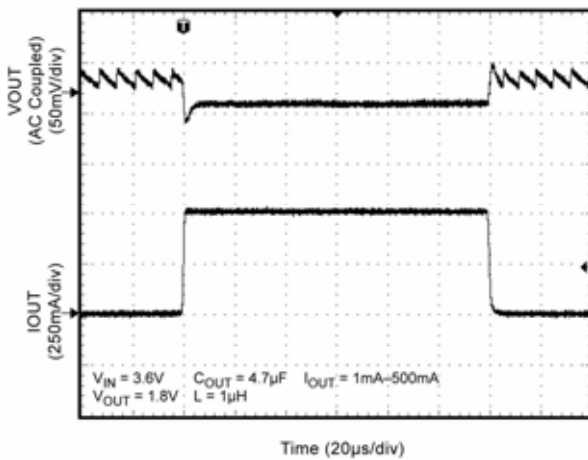
Load Transient



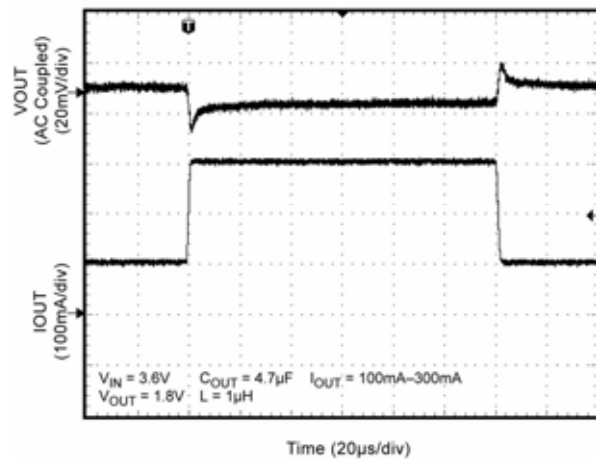
Load Transient



Load Transient



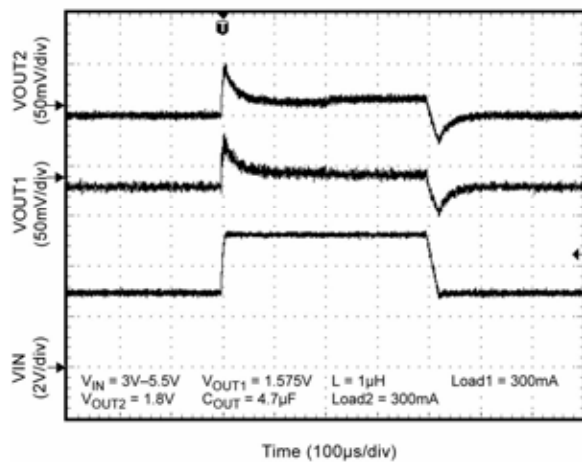
Load Transient



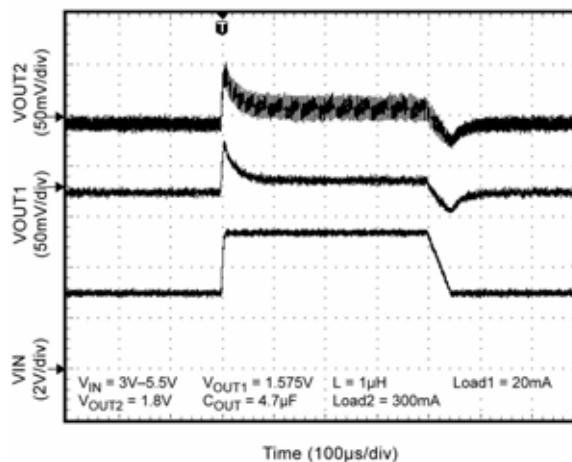


## Functional Characteristics (Continued)

Line Transient

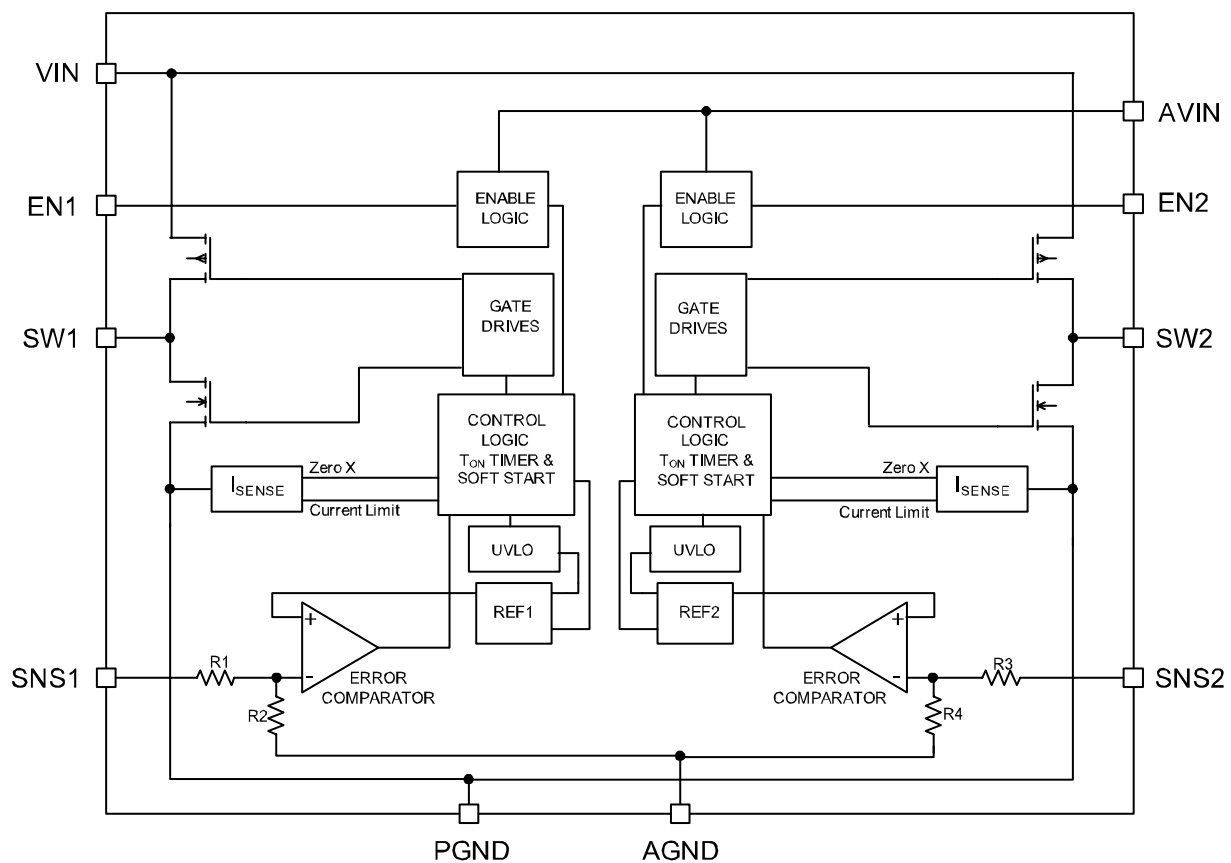


Line Transient





### Functional Diagram



**MIC23250 Simplified Block Diagram**

## Functional Description

### VIN

The VIN provides power to the internal MOSFETs for the switch mode regulator along with the current limit sensing. The VIN operating range is 2.7V to 5.5V so an input capacitor with a minimum of 6.3V voltage rating is recommended. Due to the high switching speed, a minimum of 2.2 $\mu$ F bypass capacitor placed close to VIN and the power ground (PGND) pin is required. Based upon size, performance and cost, a TDK C1608X5R0J476K, size 0603, 4.7 $\mu$ F ceramic capacitor is highly recommended for most applications. Refer to the layout recommendations for details.

### AVIN

The analog VIN (AVIN) provides power to the analog supply circuitry. AVIN and VIN must be tied together. Careful layout should be considered to ensure high frequency switching noise caused by VIN is reduced before reaching AVIN. A 0.01 $\mu$ F bypass capacitor placed as close to AVIN as possible is recommended. See layout recommendations for details.

### EN1/EN2

The enable pins (EN1 and EN2) control the on and off states of outputs 1 and 2, respectively. A logic high signal on the enable pin activates the output voltage of the device. A logic low signal on each enable pin deactivates the output. MIC23250 features built-in soft-start circuitry that reduces in-rush current and prevents the output voltage from overshooting at start up.

### SW1/SW2

The switching pin (SW1 or SW2) connects directly to one end of the inductor (L1 or L2) and provides the current path during switching cycles. The other end of the inductor is connected to the load and SNS pin. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes.

### SNS1/SNS2

The SNS pin (SNS1 or SNS2) is connected to the output of the device to provide feedback to the control circuitry. A minimum of 2.2 $\mu$ F bypass capacitor should be connected in shunt with each output. Based upon size, performance and cost, a TDK C1608X5R0J476K, size 0603, 4.7 $\mu$ F ceramic capacitor is highly recommended for most applications. In order to reduce parasitic inductance, it is good practice to place the output bypass capacitor as close to the inductor as possible. The SNS connection should be placed close to the output bypass capacitor. Refer to the layout recommendations for more details.

### PGND

The power ground (PGND) is the ground path for the high current in PWM mode. The current loop for the power ground should be as small as possible and separate from the Analog ground (AGND) loop. Refer to the layout recommendations for more details.

### AGND

The signal ground (AGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the Power ground (PGND) loop. Refer to the layout recommendations for more details.

## Applications Information

The MIC23250 is designed for high performance with a small solution size. With a dual 400mA output inside a tiny 2mm x 2mm Thin MLF<sup>®</sup> package and requiring only six external components, the MIC23250 meets today's miniature portable electronic device needs. While small solution size is one of its advantages, the MIC23250 is big in performance. Using the Hyper Light Load™ switching scheme, the MIC23250 is able to maintain high efficiency throughout the entire load range while providing ultra-fast load transient response. Even with all the given benefits, the MIC23250 can be as easy to use as linear regulators. The following sections provide an over view of implementing MIC23250 into related applications

### Input Capacitor

A minimum of 2.2µF ceramic capacitor should be placed close to the VIN pin and PGND pin for bypassing. A TDK C1608X5R0J476K, size 0603, 4.7µF ceramic capacitor is recommended based upon performance, size and cost. A X5R or X7R temperature rating is recommended for the input capacitor. Y5V temperature rating capacitors, aside from losing most of their capacitance over temperature, can also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

### Output Capacitor

The MIC23250 was designed for use with a 2.2µF or greater ceramic output capacitor. Increasing the output capacitance will lower output ripple and improve load transient response but could increase solution size or cost. A low equivalent series resistance (ESR) ceramic output capacitor such as the TDK C1608X5R0J476K, size 0603, 4.7µF ceramic capacitor is recommended based upon performance, size and cost. Either the X7R or X5R temperature rating capacitors are recommended. The Y5V and Z5U temperature rating capacitors, aside from the undesirable effect of their wide variation in capacitance over temperature, become resistive at high frequencies.

### Inductor Selection

Inductor selection will be determined by the following (not necessarily in the order of importance);

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC23250 was designed for use with an inductance range from 0.47µH to 4.7µH. Typically, a 1µH inductor is recommended for a balance of transient response, efficiency and output ripple. For faster transient response a 0.47µH inductor may be used. For lower output ripple, a 4.7µH is recommended.

Maximum current ratings of the inductor are generally

given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin so that the peak current of the inductor does not cause it to saturate. Peak current can be calculated as follows:

$$I_{PEAK} = \left[ I_{OUT} + V_{OUT} \left( \frac{1 - V_{OUT} / V_{IN}}{2 \times f \times L} \right) \right]$$

As shown by the previous calculation, the peak inductor current is inversely proportional to the switching frequency and the inductance; the lower the switching frequency or the inductance the higher the peak current. As input voltage increases the peak current also increases.

The size of the inductor depends on the requirements of the application. Refer to the Application Circuit and Bill of Material for details.

DC resistance (DCR) is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the Efficiency Considerations.

### Compensation

The MIC23250 is designed to be stable with a 0.47µH to 4.7µH inductor with a minimum of 2.2µF ceramic (X5R) output capacitor.

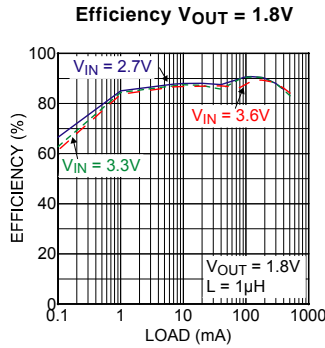
### Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

$$Efficiency \text{ \%} = \left( \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it reduces consumption of current for battery powered applications. Reduced current draw from a battery increases the devices operating time and is critical in hand held devices.

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of  $I^2R$ . Power is dissipated in the high side switch during the on cycle. Power loss is equal to the high side MOSFET  $R_{DS(ON)}$  multiplied by the Switch Current squared. During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage is another DC loss. The current required driving the gates on and off at a constant 4MHz frequency and the switching transitions make up the switching losses.



The Figure above shows an efficiency curve. From no load to 100mA, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. By using the Hyper Light Load™ mode the MIC23250 is able to maintain high efficiency at low output currents.

Over 100mA, efficiency loss is dominated by MOSFET  $R_{DSON}$  and inductor losses. Higher input supply voltages will increase the Gate-to-Source threshold on the internal MOSFETs, thereby reducing the internal  $R_{DSON}$ . This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

$$L\_Pd = I_{OUT}^2 \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows:

$$Efficiency\_Loss = \left[ 1 - \left( \frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + L\_Pd} \right) \right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

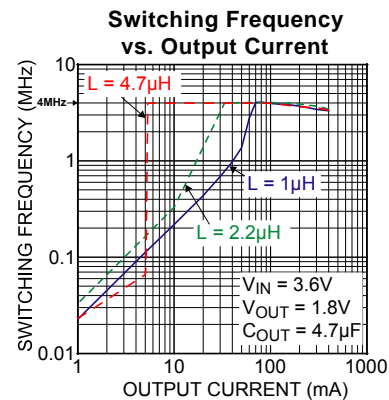
**Hyper Light Load Mode™**

The MIC23250 uses a minimum on and off time proprietary control loop (patented by Micrel). When the output voltage falls below the regulation threshold, the error comparator begins a switching cycle that turns the PMOS on and keeps it on for the duration of the minimum-on-time. This increases the output voltage. If the output voltage is over the regulation threshold, then the error

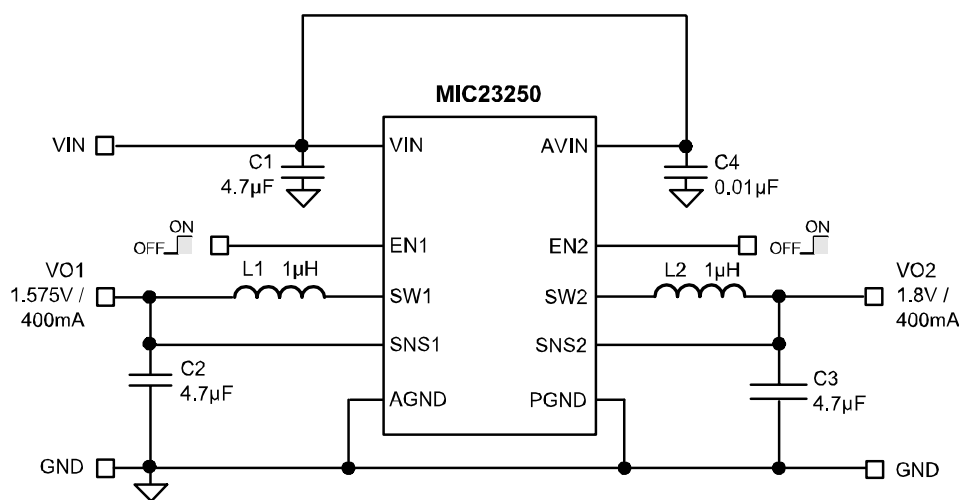
comparator turns the PMOS off for a minimum-off-time until the output drops below the threshold. The NMOS acts as an ideal rectifier that conducts when the PMOS is off. Using a NMOS switch instead of a diode allows for lower voltage drop across the switching device when it is on. The asynchronous switching combination between the PMOS and the NMOS allows the control loop to work in discontinuous mode for light load operations. In discontinuous mode, the MIC23250 works in pulse frequency modulation (PFM) to regulate the output. As the output current increases, the off-time decreases, thus providing more energy to the output. This switching scheme improves the efficiency of MIC23250 during light load currents by only switching when it is needed. As the load current increases, the MIC23250 goes into continuous conduction mode (CCM) and switches at a frequency centered at 4MHz. The equation to calculate the load when the MIC23250 goes into continuous conduction mode may be approximated by the following formula:

$$I_{LOAD} = \left( \frac{V_{IN} - V_{OUT} \times D}{2L \times f} \right)$$

As shown in the previous equation, the load at which MIC23250 transitions from Hyper Light Load™ mode to PWM mode is a function of the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), duty cycle (D), inductance (L) and frequency (f). This is illustrated in the graph below. Since the inductance range of MIC23250 is from 0.47μH to 4.7μH, the device may then be tailored to enter Hyper Light Load™ mode or PWM mode at a specific load current by selecting the appropriate inductance. For example, in the graph below, when the inductance is 4.7μH the MIC23250 will transition into PWM mode at a load of approximately 4mA. Under the same condition, when the inductance is 1μH, the MIC23250 will transition into PWM mode at approximately 70mA.



### MIC23250 Typical Application Circuit (Fixed 1.575V, 1.8V)



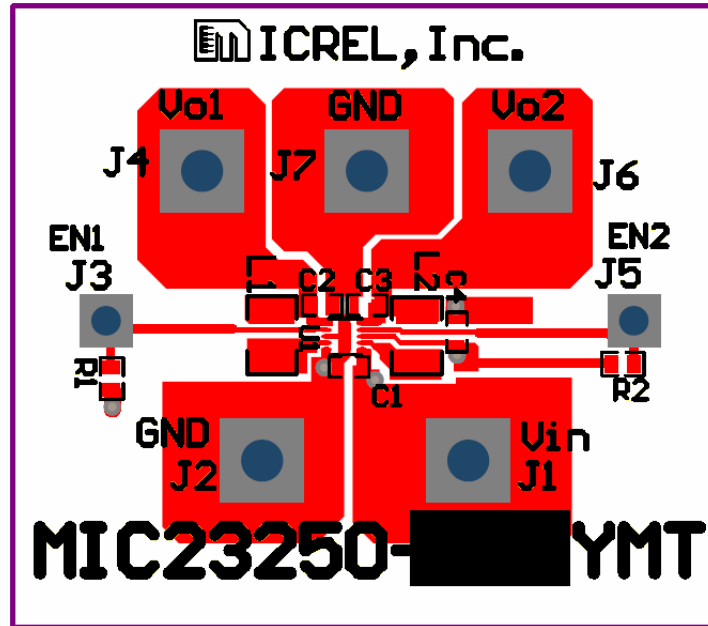
### Bill of Materials

Item	Part Number	Manufacturer	Description	Qty
C1, C2, C3	C1608X5R0J476K	TDK <sup>(1)</sup>	4.7µF Ceramic Capacitor, 6.3V, X5R, Size 0603	3
C4	VJ0603Y103KXXAT	Vishay <sup>(2)</sup>	0.01µF Ceramic Capacitor, 25V, X7R, Size 0603	1
L1, L2	LQM21PN1R0M00	Murata <sup>(3)</sup>	1µH, 0.8A, 190mΩ, L2mm x W1.25mm x H0.5mm	2
	LQH32CNR1R0M33	Murata <sup>(3)</sup>	1µH, 1A, 60mΩ, L3.2mm x W2.5mm x H2.0mm	
	LQM31P1R0M00	Murata <sup>(3)</sup>	1µH, 1.2A, 120mΩ, L3.2mm x W1.6mm x H0.95mm	
	GFL251812T	TDK <sup>(1)</sup>	1µH, 0.8A, 100mΩ, L2.5mm x W1.8mm x H1.35mm	
	LQM31PNR47M00	Murata <sup>(3)</sup>	0.47µH, 1.4A, 80mΩ, L3.2mm x W1.6mm x H0.85mm	
	MIPF2520D1R5	FDK <sup>(4)</sup>	1.5µH, 1.5A, 70mΩ, L2.5mm x W2mm x H1.0mm	
U1	MIC23250-GFHYMT	Micrel, Inc. <sup>(5)</sup>	4MHz Dual 400mA Buck Regulator with Hyper Light Load™ Mode	1

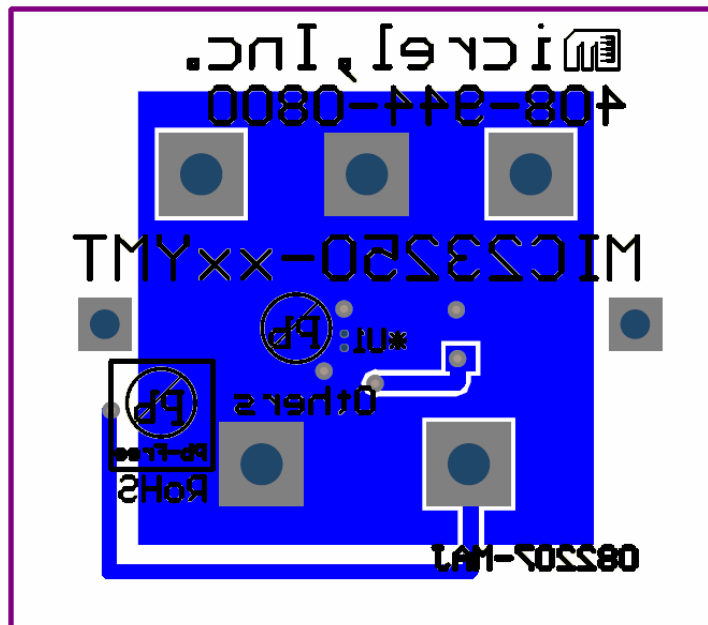
**Notes:**

1. TDK: [www.tdk.com](http://www.tdk.com)
2. Vishay: [www.vishay.com](http://www.vishay.com)
3. Murata: [www.murata.com](http://www.murata.com)
4. FDK: [www.fdk.co.jp](http://www.fdk.co.jp)
5. Micrel, Inc: [www.micrel.com](http://www.micrel.com)

### PCB Layout Recommendations

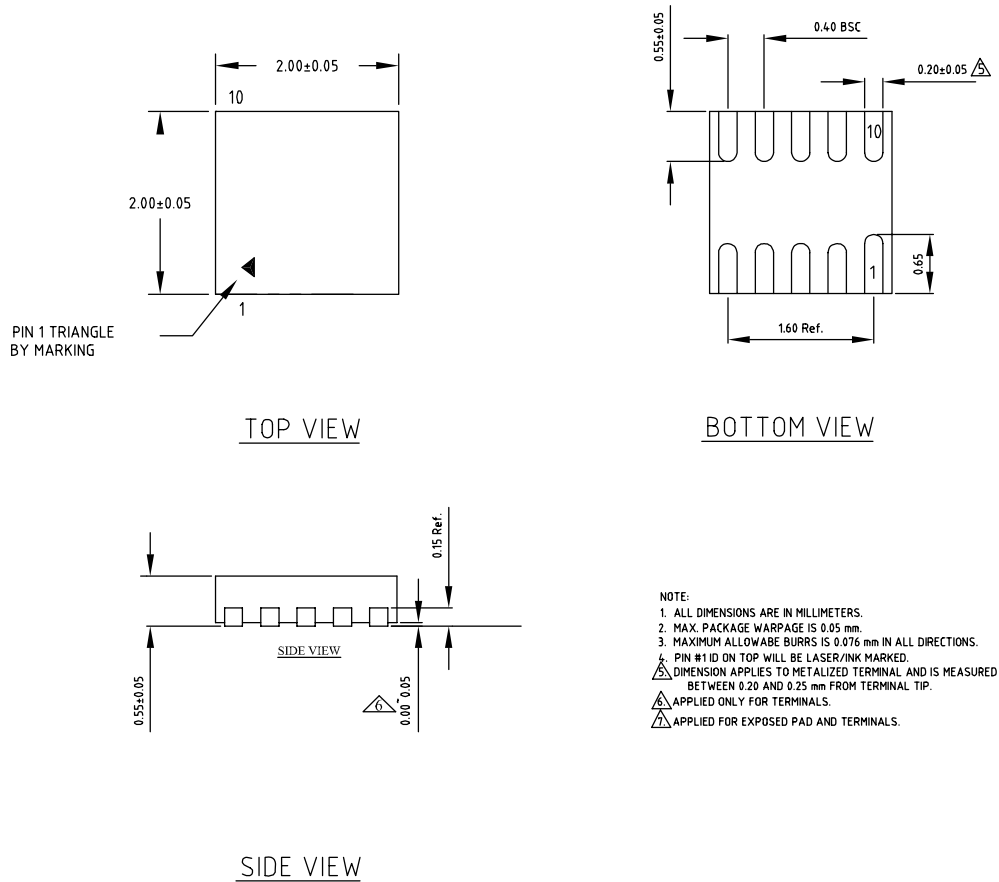


Top Layer



Bottom Layer

**Package Information**



- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. MAX. PACKAGE WARPAGE IS 0.05 mm.
  3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
  4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
- ▲ DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
- ▲ APPLIED ONLY FOR TERMINALS.
- ▲ APPLIED FOR EXPOSED PAD AND TERMINALS.

**10-Pin 2mm x 2mm Thin MLF<sup>®</sup> (MT)**

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**  
 TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

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