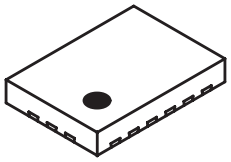
SONY

CXG1192UR

SP3T × 2 Antenna Switch for GSM Quad-Band

18 pin UQFN (Plastic)



Description

The CXG1192UR is a high power SP3T × 2 antenna switch for GSM/GPRS Quad-band applications. The low insertion loss on transmit means increased talk time as the Tx power amplifier can be operated at a lower output level. On chip logic reduces component count and simplifies PCB layout by allowing direct connection of the switch to digital baseband control lines with CMOS logic levels. This switch is SP3T × 2, each antenna can be routed to either of the 1Tx or 2Rx ports. It requires 3 CMOS control lines. The Sony GaAs JPHEMT MMIC Process is used for low insertion loss.

Features

- Insertion loss (Tx) 0.25dB typical at 34dBm (GSM900)
  0.35dB typical at 32dBm (GSM1800)
- 3 CMOS compatible control lines
- Small package size: 18-pin UQFN (2.5mm × 3.5mm × 0.6mm (Max.))

Applications

Quad-band handsets using combinations of GSM850/900/1800/1900

Structure

GaAs JPHEMT MMIC

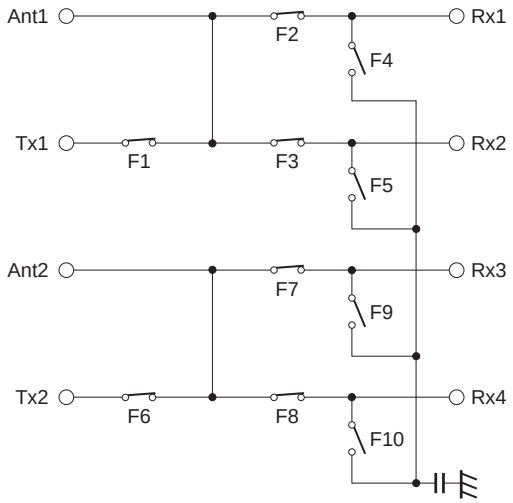
Absolute Maximum Ratings

• Bias voltage	V_{DD}	7V (Ta = 25°C)	
• Control voltage	Vctl	5V (Ta = 25°C)	
• Input power max. (Tx1)		37dBm (Ta = 25°C)	
• Input power max. (Tx2)		35dBm (Ta = 25°C)	
• Input power max. (all_Rx)		13dBm (Ta = 25°C)	
• Operating temperature	Topr	–30 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

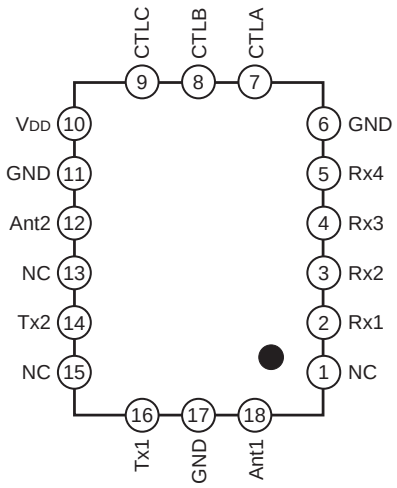
GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E04322-PS

Block Diagram



Pin Configuration



Truth Table

Path	CTLA	CTLB	CTLC	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
ANT1 – Tx1	H	L	—	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	ON
ANT2 – Tx2	H	H	—	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON
ANT1 – Rx1	L	H	L	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
ANT1 – Rx2	L	L	H	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON
ANT2 – Rx3	L	L	L	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	ON
ANT2 – Rx4	L	H	H	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Path	Conditions	Min.	Typ.	Max.	Unit
Insertion loss	IL	ANT1 – Tx1	*1		0.25	0.40	dB
		ANT2 – Tx2	*2		0.35	0.50	dB
		ANT1 – Rx1	*3, *4		0.50	0.65	dB
		ANT1 – Rx2	*3, *4		0.50	0.65	dB
		ANT2 – Rx3	*5, *6		0.70	0.85	dB
		ANT2 – Rx4	*5, *6		0.70	0.85	dB
Isolation	ISO.	Tx1 – Rx1	*1	25	30		dB
		Tx1 – Rx2	*1	25	30		dB
		Tx2 – Rx3	*2	25	30		dB
		Tx2 – Rx4	*2	25	30		dB
		Rx1 – Tx1	*3, *4	19	23		dB
		Rx2 – Tx1	*3, *4	19	23		dB
		Rx3 – Tx2	*5, *6	14	17		dB
		Rx4 – Tx2	*5, *6	14	17		dB
VSWR	VSWR				1.2		—
Harmonics*	2fo	Tx1 – Ant1	*1		–36	–30	dBm
	3fo				–37	–32	dBm
	2fo	Tx2 – Ant2	*2		–32	–29	dBm
	3fo				–40	–37	dBm
1dB compression input power	P1dB	Tx1 – Ant1	*1	36			dBm
		Tx2 – Ant2	*2	34			dBm
Control current	Ictl		Vctl = 2.8V		20	45	µA
Supply current	I_{DD}		V_{DD} = 2.8V		0.15	0.23	mA
Switching speed	Swt				8	15	µs

Electrical Characteristics are measured with all RF ports terminated in 50Ω.

* Harmonics measured with Tx inputs harmonically matched. We recommend the use of harmonic matching to ensure optimum performance.

*1 Power incident on Tx1, Pin = 34dBm, 824 to 915MHz, V_{DD} = 2.4V, Tx1 enabled

*2 Power incident on Tx2, Pin = 32dBm, 1710 to 1910MHz, V_{DD} = 2.4V, Tx2 enabled

*3 Power incident on Ant, Pin = 10dBm, 869 to 894MHz, V_{DD} = 2.4V, Rx1 or Rx2 enabled

*4 Power incident on Ant, Pin = 10dBm, 925 to 960MHz, V_{DD} = 2.4V, Rx1 or Rx2 enabled

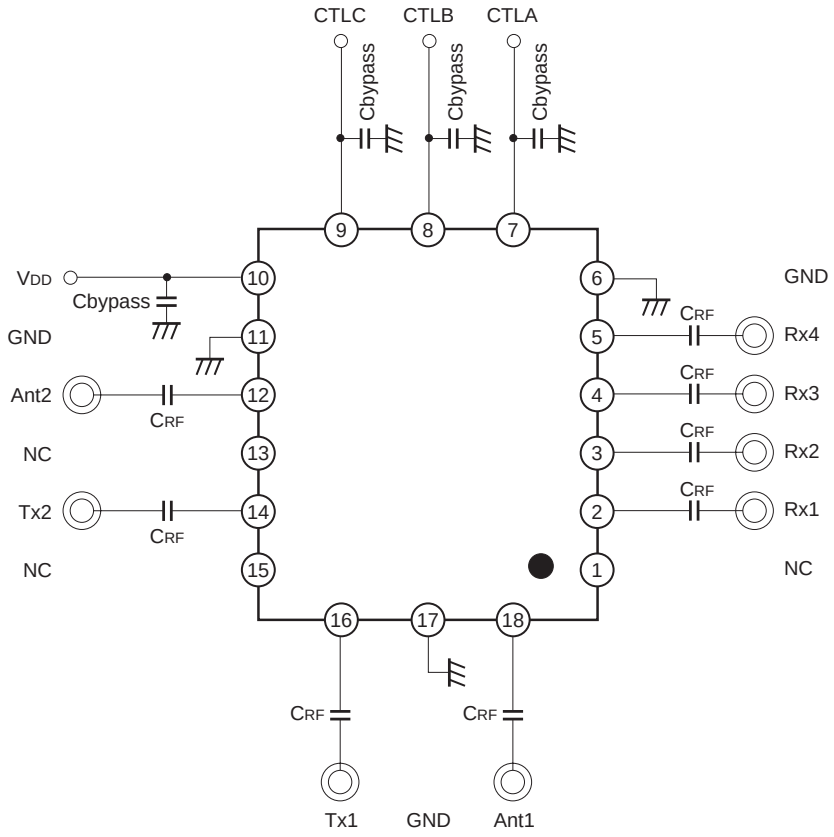
*5 Power incident on Ant, Pin = 10dBm, 1805 to 1880MHz, V_{DD} = 2.4V, Rx3 or Rx4 enabled

*6 Power incident on Ant, Pin = 10dBm, 1930 to 1990MHz, V_{DD} = 2.4V, Rx3 or Rx4 enabled

DC Bias Condition (Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.0	2.8	3.6	V
Vctl (L)	0	—	0.4	V
V_{DD}	2.4	2.8	3.6	V

Recommended Circuit



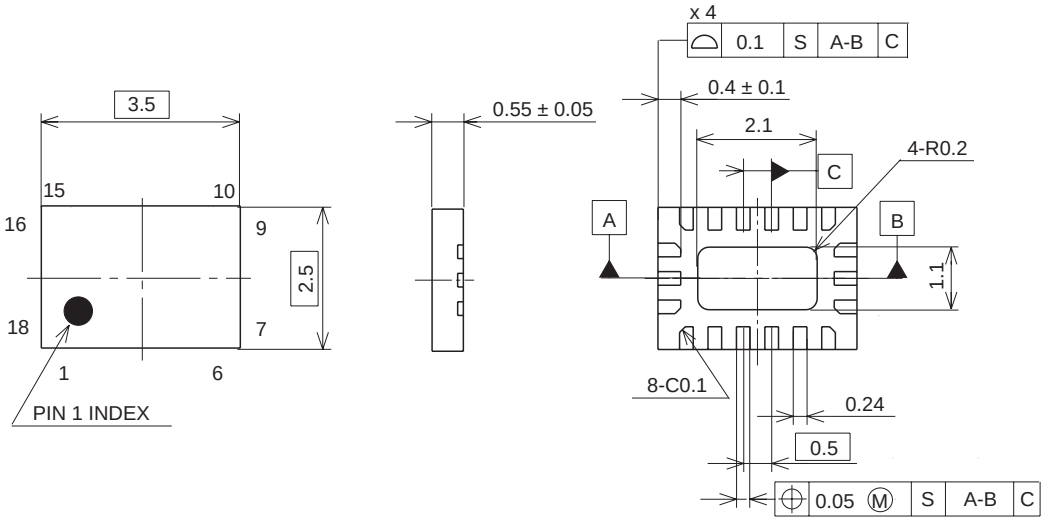
When using this IC, the following external components should be used:

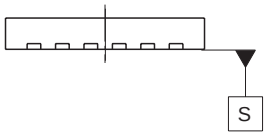
C_{RF}: This capacitor is used for RF decoupling and must be used all applications.

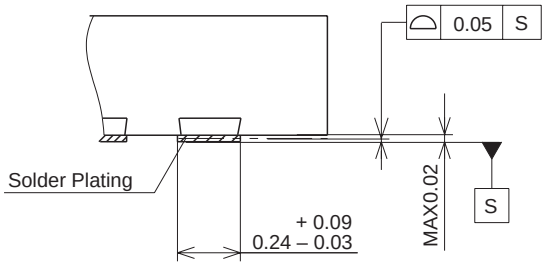
Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

Package Outline Unit: mm

18PIN UQFN (PLASTIC)







TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	UQFN-18P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm