CONEXANT™

PCI Audio/Video Broadcast Decoder

CX23880/CX23881

Single-Chip Solution Allows TV, Radio, Digital TV and Broadband Data Capture Over the PCI Bus

Conexant's highly-flexible audio and video broadcast decoder supports all analog broadcast video and audio formats in use worldwide. This single-chip solution enables the host PC to perform audio/video capture, video display, audio playback, or storage and playback at a later time through software or hardware audio/video codecs.

The CX23880/CX23881 is fully compatible with Conexant's family of digital channel demodulators for capture of (HDTV) High Definition Television and Standard Definition Television (SDTV) streams, as well as broadband data over terrestrial, satellite or cable links. The CX23880 interfaces directly to the CX23490 HDTV hardware decoder for offloading the CPU of high-level MPEG-2 decoding tasks.

A variety of third-party peripheral connectivity options are supported by the CX23880/CX23881. Its General Purpose Input/Output pins and CPU host port interface enable vendor-specific board functionality and marketplace differentiation.

Functional Overview

The CX23880/CX23881 video and broadcast audio capture chip is a mixed-signal monolithic ic enabling a new platform for video, audio, and data communications in the PC. The CX23880/CX23881 chips are designed to offer higher integration, functionality and are significantly more flexible and configurable than the previous generation Fusion™ 878A.

Distinguishing Features

- 10-bit video decoder
- Adaptive comb filter
- Global broadcast audio decoder
- Stereo DACs
- I^2S input and output
- DTV and broadband support
- MPEG encoder and decoder interfaces

PCI Audio/Video Broadcast Decoder

CX23880/CX23881

CX23880 Overview

The CX23880 is designed to offer global support for all analog video broadcast standards in addition to digital broadcasts via an external channel demodulator. It is also designed to offload the CPU of decoding tasks for High Level MPEG-2 (HDTV), 4:2:2 de-interlacing and progressive-scan DVD via a dedicated ViP 2 Host Port interface to the CX23490 high-level MPEG-2 Decoder.

CX23881 Overview

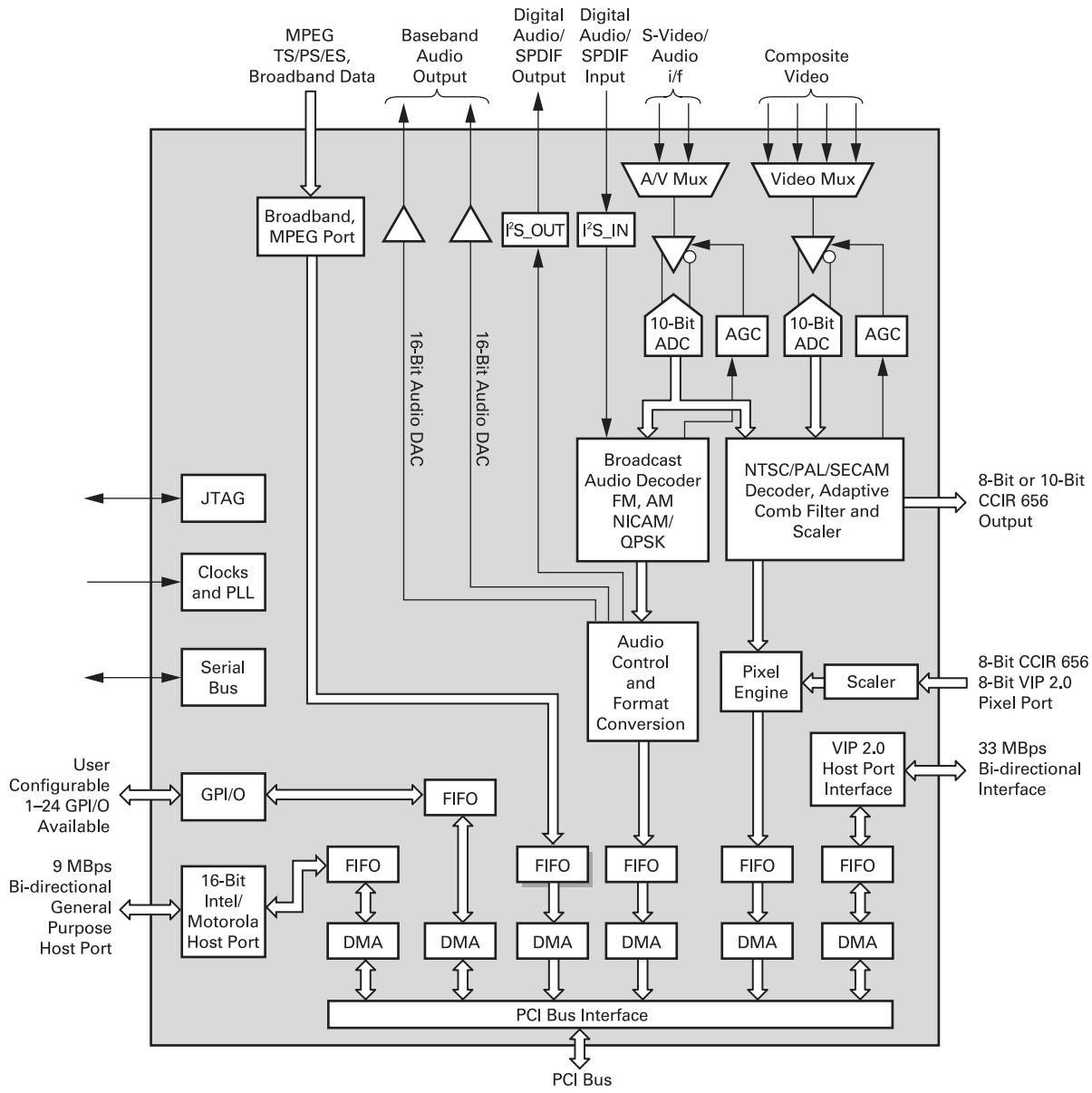
The CX23881 is a 100% pin-compatible and software-compatible subset of the CX23880. It is particularly suited to the European marketplace and therefore does not support BTSC-dBX and EIAJ audio as broadcast in the U.S. and Japan. In addition, the ViP host port is not supported on the CX23881 as there is no requirement for supporting high-level MPEG-2 decoding for digital television applications. Main Level MPEG-2 decoding for DVB broadcast applications is supported via a dedicated MPEG port for streaming of compressed data streams to the host for software-based decompression.

Both the CX23880 and CX23881 support a general purpose host port for connection to external CODECs for compression of analog video/audio broadcasts that can be stored on the host's hard disk or played back in software.

Analog Video Capture Overview

The CX23880/CX23881 integrates a 10-bit NTSC/PAL/SECAM composite and s-video decoder, image resizer/scaler, Direct Memory Access (DMA) controller and Peripheral Component Interface (PCI) bus master on a single device. The CX23880/CX23881 can place video data directly into host memory for video capture applications and into a target video display frame buffer for video overlay applications.

Feature	Fusion 878A	CX23880	CX23881
Video A/Ds	8-bit	10-bit	10-bit
Y/C separation	Luma Notch and Chroma Comb	Adaptive multi-line 2-D comb filter	Adaptive multi-line 2-D comb filter
Decoded video data output	Via GPIO	8- or 10-bit ITU-R 656 4:2:2 output	8- or 10-bit ITU-R 656 4:2:2 output
Video data input	Via GPIO	8-bit ITU-R 656/VIP 2.0 pixel input	8-bit ITU-R 656/VIP 2.0 pixel input
Broadcast audio	BTSC Mono	BTSC dbx, NICAM, A2, EIAJ, FM	NICAM, A2, FM
Audio input	Mono line level or I^2S port	Stereo I^2S port	Stereo I^2S port
Audio output	N/A	Stereo DACs, I^2S port or PCI Bus	Stereo DACs, I^2S port or PCI Bus
MPEG data streaming	I^2S port	Dedicated 80 Mbps MPEG port	Dedicated 80 Mbps MPEG port
Bi-directional streaming data ports	N/A	Intel/Motorola host port and VIP 2.0 host master port	Intel/Motorola host port only
Power supply	5V	3.3/1.8V	3.3/1.8V



CX23880 block diagram

As a PCI initiator, the CX23880/CX23881 can take control of the PCI bus to stream data as soon as the bus is available, thereby avoiding the need for on-board frame buffers. The CX23880/CX23881 contains a pixel data First In, First Out (FIFO) to decouple the high-speed PCI bus from the continuous video data stream. The video data input may be scaled, color translated, and burst-transferred to a target location on a field basis. This allows for simultaneous preview of one field and capture of the other field. Alternatively, the CX23880/CX23881 is able to capture or preview both fields simultaneously. The fields may be interlaced into memory or sent to separate field buffers.

Video Input

Analog video signals are input to the CX23880/CX23881 via a four-input multiplexer. The multiplexer can select between four composite source inputs or between three composite and a single s-video input source. When an s-video source is input to the CX23880/CX23881, the luma component is fed through the input analog multiplexer, and the chroma component feeds directly into the C-input pin. An Automatic Gain Control (AGC) circuit enables the CX23880/CX23881 to compensate for non-standard amplitudes in the analog signal input.

Reduced Instruction Set Computing (RISC) Engine

The CX23880/CX23881 enables separate destinations for the odd and even video fields, each controlled by a pixel RISC instruction list. This instruction list is created by the CX23880/CX23881 device driver and may be run in the on-chip memory or host memory. The instructions control the transfer of pixels to target memory locations on a byte resolution basis. Complex clipping can be accomplished by the instruction list, blocking the generation of PCI bus cycles for pixels that are not to be seen on the display.

The DMA channels can be programmed on a field basis to deliver the video data in packed or planar format. In packed mode, YCrCb data is stored in a single continuous block of memory. In planar mode, the YCrCb data is separated into three streams which are burst to different target memory blocks. Having the video data in planar format is useful for applications where data compression is accomplished via software and the CPU.

UltraLock™

The CX23880/CX23881 employs a proprietary technique known as UltraLock to lock on to the incoming analog video signal. It consistently generates the required number of pixels per line from an analog source in which line length can vary by as much as a few microseconds. UltraLock's digital locking circuitry enables the CX23880/CX23881 to lock onto video signals quickly and accurately, regardless of their source. The technique is completely digital, so UltraLock can recognize unstable signals caused by VCR head switches or any other deviation and can adapt the locking mechanism to accommodate the source. UltraLock uses nonlinear techniques that are difficult, if not impossible, to implement in genlock systems. Unlike linear techniques, it adapts the locking mechanism automatically.

Vertical Blanking Interval (VBI) Data Capture

The CX23880/CX23881 provides a flexible solution for capturing and decoding disparate VBI data types such as closed-caption data, teletext, vertical internal time and control (VITC) codes, HTML data, or multicast data. The CX23880/CX23881 can operate in a VBI line output mode, in which the VBI data is only captured from selected lines. This mode of operation enables concurrent capture of VBI lines containing ancillary data and normal video image data. In addition, the CX23880/CX23881 supports a VBI frame output mode in which every line in the video frame is treated as if it were a VBI line. This mode of operation is designed for use with still-frame capture and processing applications, where sophisticated image decoding can be performed in the software domain.

Macrovision® Detector

With the advent of more powerful CPUs that enable software-based video compression, low-cost hardware MPEG encoders, cheap and rewritable storage media, and pervasive broadband communications, original content protection is paramount. To this end, the CX23880/CX23881 fully implements Macrovision 7.01 detection. When an end-user attempts to connect a digital video disk (DVD) player, a digital satellite/cable decoder's composite, or s-video outputs to the input of a CX23880/ CX23881-based PCI card, Macrovision pulses and signals are detected, and appropriate flag bits are set. It is up to the board vendor to read the flag bits and determine what action will be taken.

Analog Audio Capture

The CX23880/CX23881 captures and decodes all major terrestrial broadcast audio standards. The CX23880/CX23881 digitizes and oversamples the low intermediate frequency (IF) signal from a TV tuner, and extracts and decodes the broadcast audio signal. The decoded audio is sample rate converted to a 48 KHz pulse code modulation (PCM) stereo signal to simplify processing and interfacing. This 48 KHz stream can be routed to the built-in (90 dB Signal-to-Noise Ratio (SNR) stereo audio Digital-to-Analog Converters (DACs) for connection to the PC's sound card or headphones, to an external Digital-Audio Interface, or to the PCI bus and host for direct capture by a software audio codec. The CX23881 only supports NICAM, A2 and FM broadcast audio standards primarily for the European marketplace.

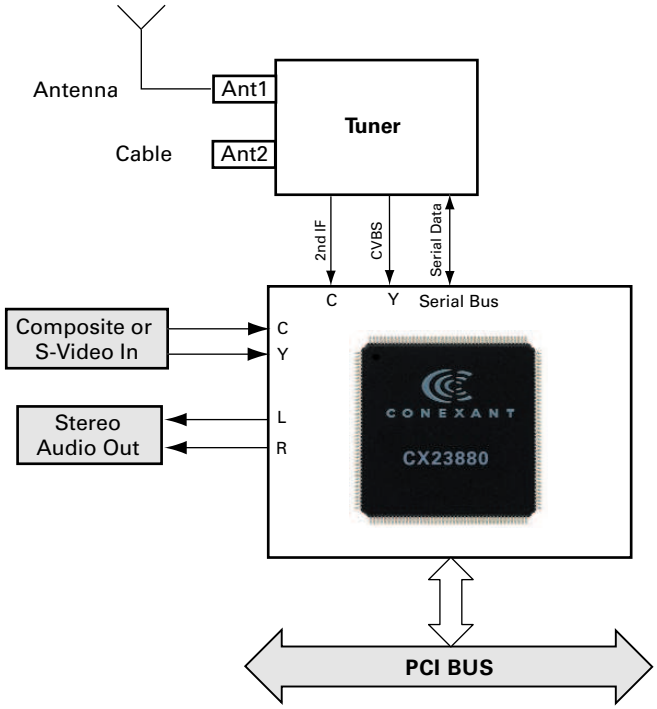
If capture of line-level stereo audio signals is required, an inexpensive audio analog-to-digital converter A/D may be directly connected to the CX23880/CX23881's I^2S input port and controlled via the serial bus master.

ITU-R 656 4:2:2 Data Output

The CX23880/CX23881 provides a 27 MHz, 8- or 10-bit ITU-R 656 decoded video output interface to allow connection of a third-party MPEG-2 encoder or other type of video codec. This is useful when the host CPU is not powerful enough to perform such tasks in software, or when high-quality encoding must be achieved. Please contact Conexant Application Engineering for a list of supported third-party video compressors.

ITU-R 656/VIP 2.0 Pixel Data Input

The CX23880/CX23881 provides a 27 MHz, 8-bit ITU-R 656 decoded video input interface to allow a third-party MPEG-2 decoder or codec to send 4:2:2 data over the PCI bus to a target video display frame buffer for video overlay. Alternatively, 480-line progressive scan video from the CX23490 all-format MPEG-2 decoder may be input to this port using Video Interface Port (VIP) 2.0-compliant pixel timing at up to 54 MHz.



TV/FM block diagram

TV/FM application example

Features:

- Single-chip capture/record of broadcast TV and radio to PC
- Global video standards support
- Global audio standards support including FM/AM radio
- Many I/O ports to differentiate design

What is a Broadcast Decoder?

A broadcast decoder is designed to capture and decode the video and audio portions of any analog TV broadcast signal. In addition, a broadcast decoder must be able to address the transition to all-digital broadcasting by offering a variety of methods to connect to digital TV channel demodulators. Sufficient I/O must be provided to support external hardware-based compression of analog video/audio signals in order to enable storage onto hard disks or CDROM.

Conexant's broadcast decoder meets these objectives in the following way:

1) It captures and decodes all variations of NTSC, PAL and SECAM video standards into digital RGB or YUV pixel streams.
2) It captures and decodes all broadcast audio standards used worldwide such as BTSC/DBX, NICAM, A2, EIAJ and FM/AM, into 48 KHz PCM streams or stereo left and right audio signals.
3) It facilitates "analog to MPEG" conversion by providing an 8- or 10-bit ITU-R 656 pixel interface to an external MPEG 2 encoder for real-time compression. Providing a streaming host port or MPEG port for DMA of compressed data to the host or hard disk.
4) It provides a dedicated high-speed streaming MPEG port that is compatible with ATSC, DVB and ISDB digital television channel demodulators for DMA to the host or hard disk.

MPEG Data Port

Channel demodulators used for digital TV or broadband data applications over terrestrial, satellite, or cable networks may be directly connected to the CX23880/CX23881's MPEG data port to deliver transport streams to the host for subsequent storage to disk or software decode. Either parallel Digital Video Broadcasting (DVB) (common interface) or serial data paths from the channel demodulator may be supported at data transfer rates of up to 80 Mbps. If the serial interface mode is used, then the remaining unused pins on this port may be allocated as GPIO.

VIP 2.0 Host-Master Interface Port (CX23880 only)

The VIP 2.0 host-master interface allows the CX23880 to communicate with all devices that are compliant with the VIP slave specification. This implementation of a VIP 2.0 master is backwards-compatible with all VIP 1.1-compliant slave interfaces. The CX23880 is designed to connect to the CX23490 all-format MPEG-2 decoder via this interface. The functionality of the VIP host-master interface is threefold. The first concept is to stream data from a VIP slave into host memory via the PCI bus. The second concept is to stream out data to a VIP slave that is sent over the PCI bus from the host. The third concept is for the host to be able to access register space on connected VIP slave devices. The CX23881 does not support the VIP 2.0 host master interface port and in order to retain pin compatability with the CX23880, these pins are configured as GPIO.

General Purpose Host Interface Port

The general purpose host interface allows the connection of moderate to relatively slow-speed third-party peripherals (such as infrared remote control processors, codec host ports, smart card controllers, etc.), to the CX23880/CX23881. This port allows simultaneous connection to two peripherals glue free, or as many as four peripherals with the use of external glue logic to provide the additional chip selects. This interface may have one upstream and one downstream DMA channel active to or from the external peripherals at any given time.

GPIO Port

The CX23880/CX23881 provides up to 24 GPIO pins. These GPIO pins are shared with the following pins/ports groups so that the user can determine exactly which pins can be dedicated to specific functions versus GPIO functions:

- MPEG parallel data port
- ITU–R 656 4:2:2 data output
- ITU–R 656 4:2:2 data input
- Extended VIP host port

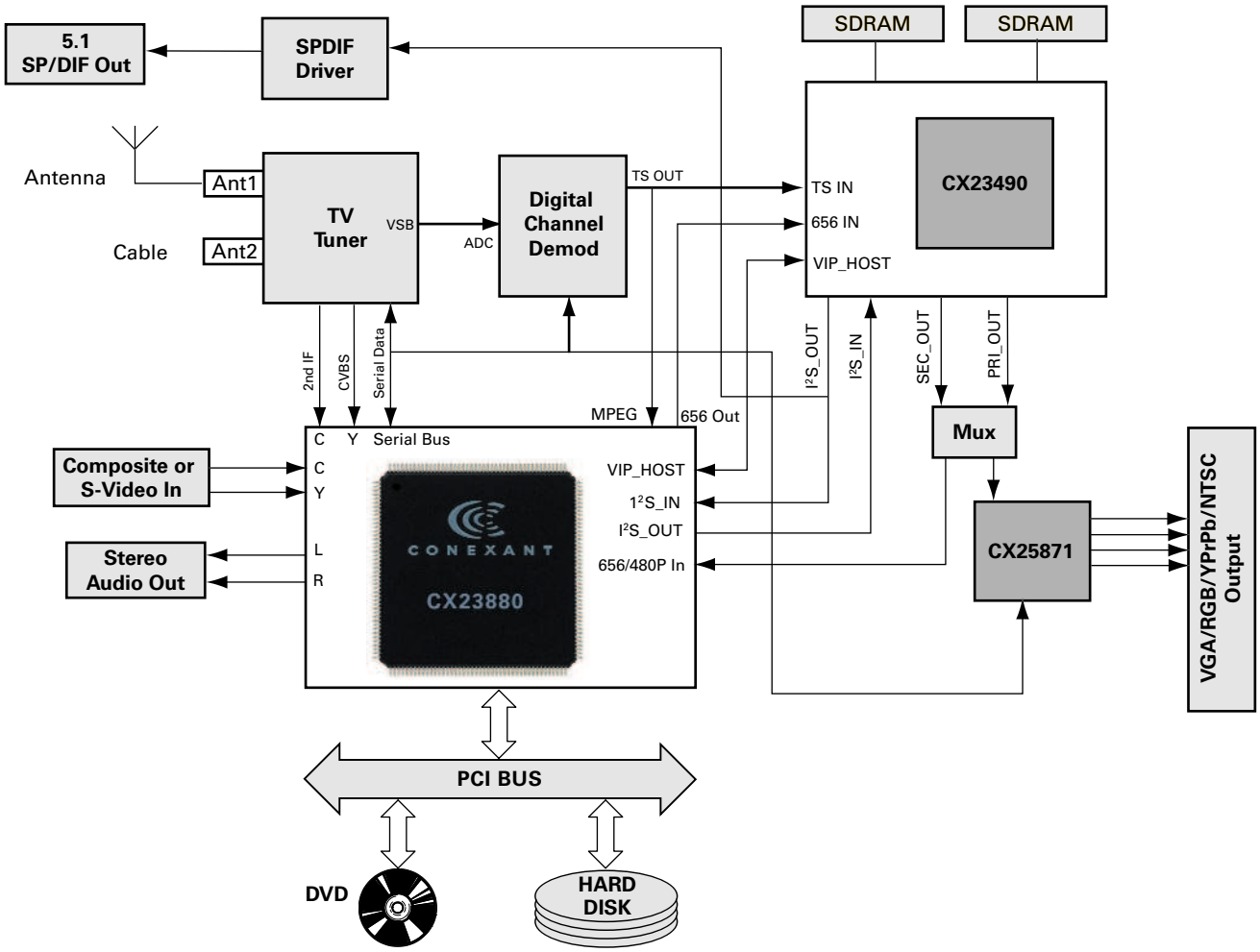
Serial Bus Interface

The CX23880/CX23881's serial bus interface supports both 99.2 KHz timing transactions and 396.8 kHz, repeated start, multibyte sequential transactions. As a serial bus master, the CX23880/CX23881 can program other devices on the video card, such as a TV tuner, as long as the device address is known. The CX23880/CX23881 supports multibyte sequential reads (more than one transaction) and multibyte write transactions (greater than three transactions), which enable communication to devices that support auto-incremental internal addressing.

PCI Bus Interface

The CX23880/CX23881 is designed to efficiently utilize the available 132 Mbps PCI bus. The 32-bit words are output on the PCI bus with the appropriate image data under the control of the DMA channels. The video stream consumes bus bandwidth with average data rates varying from 44 Mbps for full-size 768 x 576 PAL RGB32, to 4.6 Mbps for NTSC CIF 320 x 240 RGB16, to 0.14 Mbps for NTSC ICON 80 x 60 8-bit mode.

The pixel instruction stream for the DMA channels consumes a minimum of 0.1 Mbps. The CX23880/CX23881 provides the means for handling the bandwidth bottlenecks caused by slow targets and long bus access latencies that can occur in some system configurations. To overcome these system bottlenecks, the CX23880 gracefully degrades and recovers from FIFO overruns to the nearest pixel in real time.

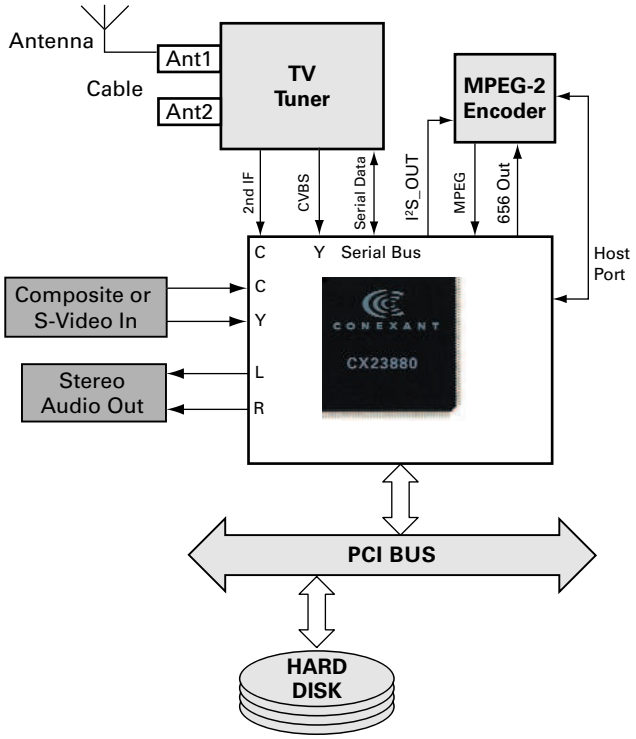


HD-Theater block diagram

HD-Theater application example

Features:

- ATSC high-definition TV decoding
- 480P/720P/1080i output resolution from HDTV or DVD sources
- 5.1 Dolby Digital™, Pro-Logic™ and down-mixed 2.0 audio
- NTSC up-conversion and de-interlacing to 480P/720P/1080i
- Virtual surround spatialization for analog broadcast audio
- Record HD programs to disk



Digital VCR block diagram

Digital VCR application example

Features:

- Compresses broadcast video (ITU-R 656) and broadcast audio (PCM) to MPEG PS/ES
- Allows real-time video preview in a window
- Simultaneous "watch and record" with VGA overlay
- Time-shift television programs

Product Features

Video Subsystem Features

- 10-bit video A/D
- Global video standards support [NTSC (M, J, 4.43), PAL (B, D, G, H, I, M, N, N-combination), SECAM (K, L)]
- Capture resolution up to 768 x 576 (square pixel PAL/SECAM)
- NTSC and PAL adaptive comb filter for 2-D Y/C luminance and chrominance separation
- AGC video circuit
- Multiple YCrCb and RGB pixel formats and YUV planar formats supported on output
- Selectable pixel density: 8, 16, 24 and 32-bits per pixel
- Performs complex clipping of video source and VGA video overlay
- Permits different program control and color space/scaling for even and odd fields
- Supports Windows® "Scatter/Gather" DMA
- High-quality multi-tap horizontal and vertical image scaler for decoded video or 4:2:2 sources
- ITU-R BT.656 8-bit or 10-bit 4:2:2 output port for MPEG-2 encoder connection
- ITU-R BT.656/VIP 2.0 pixel input port for MPEG-2 ML or HL decoder connection
- Flexible VBI data capture for closed captioning, teletext, other analog broadcast data types
- Hue, brightness, contrast, saturation control for video decoder

Audio Subsystem

- Low IF sampling direct from tuner
- CX23880: Global broadcast audio support (BTSC-DBX, NICAM, A2, EIAJ, FM)
- CX23881: European broadcast audio support (NICAM, A2, FM)
- Decoded 48 KHz audio stream to PCI bus for real-time encoding to MP3
- Integrated 90 dB SNR stereo audio DACs to drive sound card or headphones
- I²S Input port for external source connectivity to on-board stereo DACs
- I²S Output port to drive coaxial/optical digital audio interface
- Flexible audio sample rate converter

Multipurpose I/O Subsystem

- Bi-directional 33 Mbps VIP 2.0 host port. Comapatible with the CX23490 all-format MPEG-2 decoder (CX23880 only)
- Bi-directional 10 Mbps Intel/Motorola-compatible general purpose host port
- Unidirectional 10 Mbps parallel/serial MPEG transport/data stream port. Compatible with all Conexant digital television channel demodulator ICs
- MPEG packet synchronization
- User-defined general purpose input/output pins

PCI Subsystem

- 5 independent functions each with target/master and local register space (video, audio, MPEG port, VIP 2.0 host port, GP host port)
- All RISC/control programs executed on chip
- On-chip SRAM for PCI data buffering up/down
- Vital product data
- DMA byte alignment
- PCI revision 2.2 compliant

Miscellaneous

- ACPI and power-down support
- Requires only one crystal for all video and audio decoding
- 400 KHz serial bus master
- JTAG boundary scan interface
- Compact 176-pin TQFP
- Low power

Applications

- PC TV
- PC TV
- Digital television
- Digital VCR
- Analog and digital video editing
- MP3 radio
- PCI cable modem
- PCI satellite modem
- Data broadcast receiver
- Media hub for home server

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