3.0 Volt Multi-Chip Package (MCP) — 128 Mbit Simultaneous Operation Flash Memory and 32 Mbit Pseudo Static RAM

PRELIMINARY INFORMATION
MARCH 2003

MCP FEATURES

- Power supply voltage 2.7V to 3.3V
- High performance:
  Flash: 70ns maximum access time
  PSRAM: 65ns maximum access time
- Package: 107-ball BGA
- Operating Temperature: -30C to +85C

FLASH FEATURES

- Power Dissipation:
  Read Current at 1 Mhz: 4 mA maximum
  Read Current at 5 Mhz:18 mA maximum
  Sleep Mode: 5 µA maximum
- User Configurable Banks
  Flash 1 (64 Mbit)
  Bank A1: 8Mbit (8KB x 8 and 64KB x 15)
  Bank B1: 24Mbit (64KB x 48)
  Bank C1: 24Mbit (64KB x 48)
  Bank D1: 8Mbit (8KB x 8 and 64KB x 15)

  Flash 2 (64 Mbit)
  Bank A2: 8Mbit (8KB x 8 and 64KB x 15)
  Bank B2: 24Mbit (64KB x 48)
  Bank C2: 24Mbit (64KB x 48)
  Bank D2: 8Mbit (8KB x 8 and 64KB x 15)
  User chooses two virtual banks from a combination of four physical banks
- Simultaneous R/W Operations (dual virtual bank):
  Zero latency between read and write operations; Data can be programmed or erased in one bank while data is simultaneously being read from the other bank
- Low-Power Mode:
  A period of no activity causes flash to enter a low-power state
- Erase Suspend/Resume:
  Suspends of erase activity to allow a read in the same bank
- Sector Erase Architecture:
  16 sectors of 4K words each and 126 sectors of 32K words each in Word mode. Any combination of sectors, or the entire flash can be simultaneously erased
- Erase Algorithms:
  Automatically preprograms/erases the flash memory entirely, or by sector
- Program Algorithms:
  Automatically writes and verifies data at specified address
- Hidden ROM Region:
  256 byte with a Factory-serialized secure electronic serial number (ESN), which is accessible through a command sequence
- Data Polling and Toggle Bit:
  Detects the completion of the program or erase cycle
- Ready-Busy Outputs (RY/$\overline{BY}$)
  Detection of program or erase cycle completion for each flash chip
- Over 100,000 write/erase cycles
- Low supply voltage (Vccf ≤ 2.5V) inhibits writes
- $\overline{WP}$/ACC input pin:
  If V_{IL}, allows partial protection of boot sectors
  If V_{IH}, allows removal of boot sector protection
  If Vacc, program time is improved

PSRAM FEATURES (32 Mb density)

- Power Dissipation:
  Operating: 25 mA maximum
  Standby: 110 µA maximum
- Chip Selects: $\overline{CE1}$r, CE2r
- Power down feature using CE2r
  Sleep Mode: 10 µA maximum
  Nap: 65 µA maximum
  8 mbit Partial: 80 µA maximum
- Data retention supply voltage: 2.1 V to 3.3V
- Byte data control: $\overline{LB}$ (DQ0–DQ7), $\overline{UB}$ (DQ8–DQ15)

GENERAL DESCRIPTION

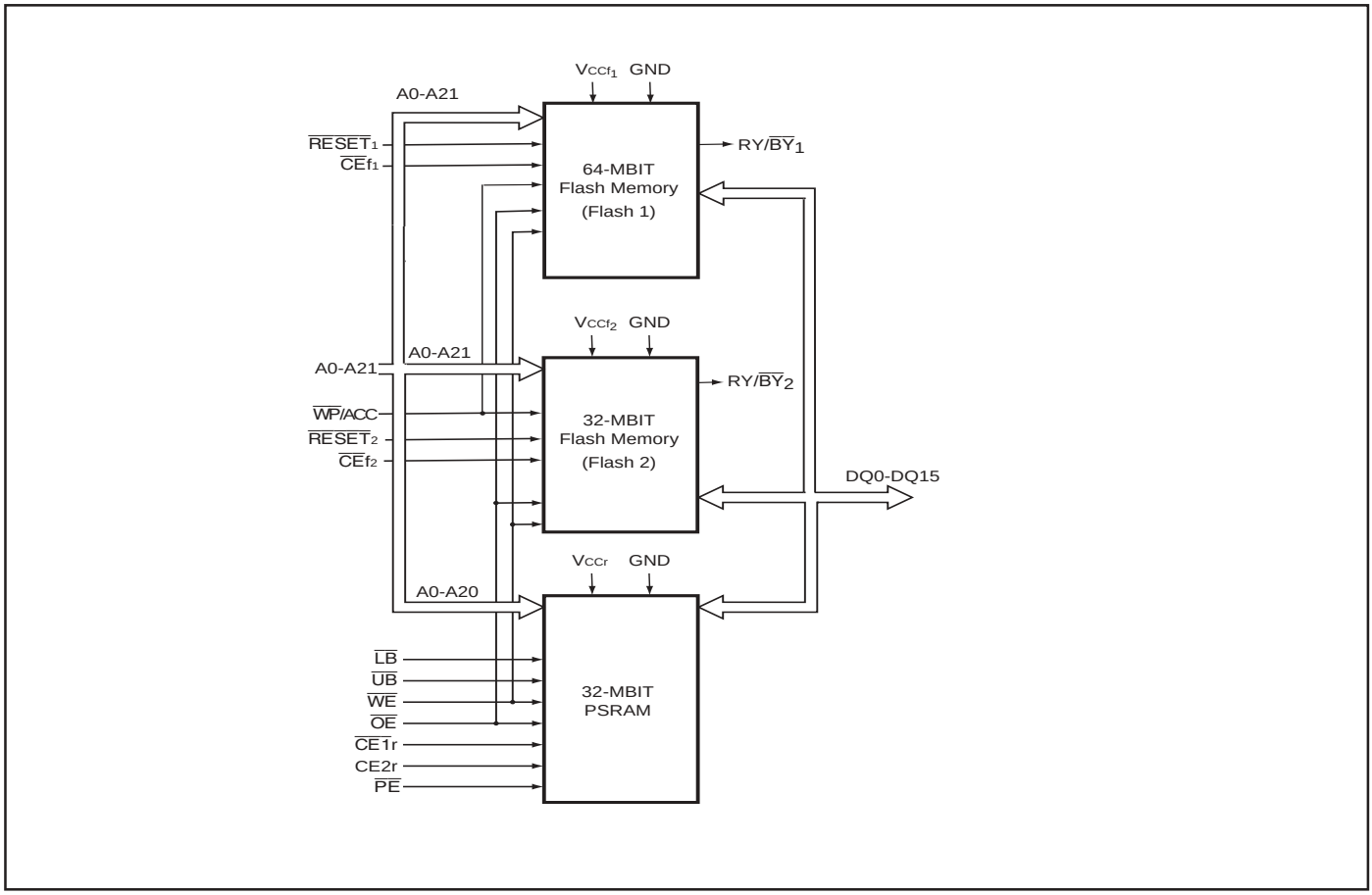
This 107-ball MCP is a space-saving combination of 3 memories: two 64Mbit Flash and one 32Mbit Pseudo SRAM. Each 64Mbit Flash (Flash1 and Flash 2) contains 4,194,304 words and the 32Mbit PSRAM contains 2,097,152 words. Each word is 16 bits wide. Data lines DQ0-DQ15 handle the access for all three memories. Write Enable, Output Enable, and A0-A20 are shared among the three memories. Single Byte data on the PSRAM can be accessed one at a time on DQ0-DQ7 or DQ8-DQ15 by using $\overline{LB}$ or $\overline{UB}$, respectively.

The package uses a 3.0V power supply for all operations. No other source is required for program and erase operations. The flash can be programmed in system using this 3.0V supply, or can be programmed in a standard EPROM programmer.

The flash chips are compatible with the JEDEC Flash command set standard. The flash access time is 70ns and the PSRAM access time is 65ns.

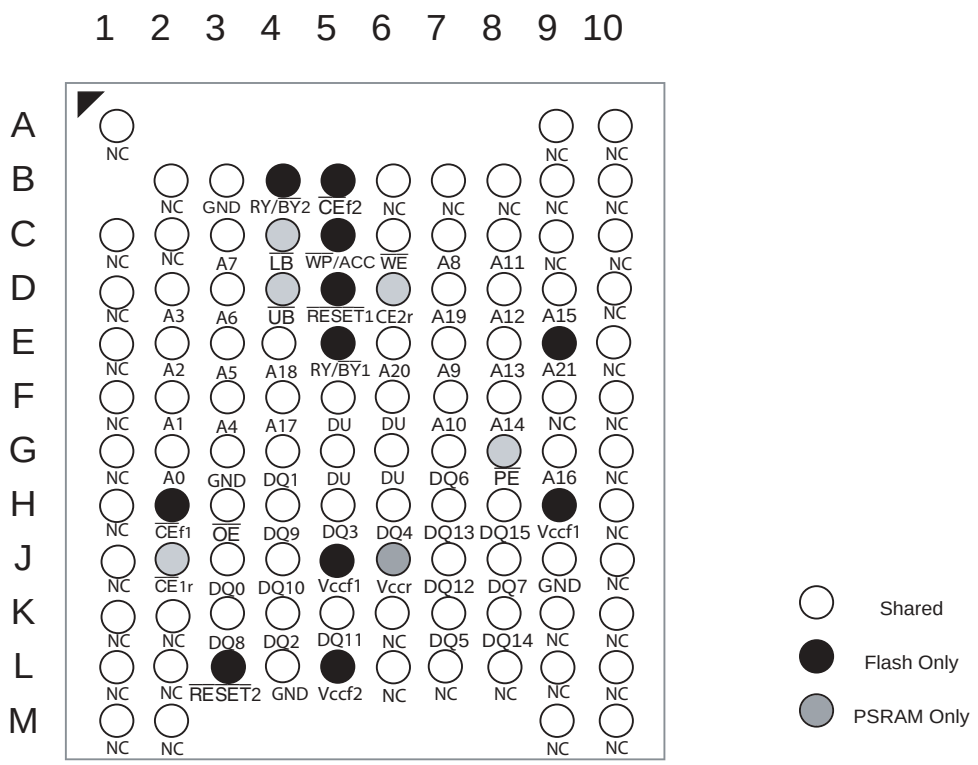
Each Flash memory implements an architecture composed of two virtual banks that allows simultaneous operation on each bank. Optimized performance can be achieved by first initializing a program or erase function in one bank, then immediately starting a read from the other bank. Both operations would then be operating simultaneously on the same chip, with zero latency.

MCP BLOCK DIAGRAM



PIN CONFIGURATION (128 Mb Flash and 32 Mb PSRAM)

PACKAGE CODE: B 107 BALL FBGA (Top View) (9.00 mm x 10.00 mm Body, 0.8 mm Ball Pitch)



PIN DESCRIPTIONS

A0-A20	Address Inputs, Common
A21	Address Input, Both Flash
DQ0-DQ15	Data Inputs/Outputs, Common
$\overline{RESET}$1	Reset, Flash1
$\overline{RESET}$2	Reset, Flash2
$\overline{CE1}$r, CE2r	Chip Enable, PSRAM
$\overline{CE}$f1	Chip Enable, Flash1
$\overline{CE}$f2	Chip Enable, Flash2
$\overline{OE}$	Output Enable, Common
$\overline{WE}$	Write Enable, Common
$\overline{PE}$	Partial Enable, PSRAM

$\overline{LB}$	Lower-byte Control, PSRAM
$\overline{UB}$	Upper-byte Control, PSRAM
$\overline{WP}$/ACC	Write Protect/Acceleration Pin, Both Flash
RY/$\overline{BY1}$	Ready/Busy Output , Flash1
RY/$\overline{BY2}$	Ready/Busy Output , Flash2
NC	No Connection
DU	Do Not Use
Vccf1	Power, Flash1
Vccf2	Power, Flash2
Vccr	Power, PSRAM
GND	Ground, Common

DEVICE BUS OPERATION

OPERATION[1,2]	$\overline{CE}$f1	$\overline{CE}$f2	$\overline{CE1}$r	CE2r	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$s	$\overline{UB}$s	$\overline{PE}$	A_{21}-A_0	DQ_7-DQ_0	DQ_{15}-DQ_8	$\overline{RESET1}$	$\overline{RESET2}$	$\overline{WP}$/ACC[12]
Full Standby	H	H	H	H	X	X	X	X	H	X	High-Z	High-Z	H	H	X
Output Disable[3]	H	H	L	H	H	H	X	X	H	X[10]	High-Z	High-Z	H	H	X
	L	H	H	H	H	H	X	X	H	X	High-Z	High-Z	H	H	X
	H	L	H	H	H	H	X	X	H	X	High-Z	High-Z	H	H	X
Read from FLASH 1[4]	L	H	H	H	L	H	X	X	H	Valid	DOUT	DOUT	H	H	X
Read from FLASH 2[4]	H	L	H	H	L	H	X	X	H	Valid	DOUT	DOUT	H	H	X
Write to FLASH 1	L	H	H	H	H	L	X	X	H	Valid	DIN	DIN	H	H	X
Write to FLASH 2	H	L	H	H	H	L	X	X	H	Valid	DIN	DIN	H	H	X
Read from PSRAM[5]	H	H	L	H	L	H	L[9]	L[9]	H	Valid	DOUT	DOUT	H	H	X
Write to PSRAM	H	H	L	H	H	L	L	L	H	Valid	DIN	DIN	H	H	X
	H	H	L	H	H	L	H	L	H	Valid	High-Z	DIN	H	H	X
	H	H	L	H	H	L	L	H	H	Valid	DIN	High-Z	H	H	X
FLASH 1Temporary Sector Group Unprotection[6]	X	X	X	X	X	X	X	X	X	X	X	X	VID	X	X
FLASH 2 Temporary Sector Group Unprotection[6]	X	X	X	X	X	X	X	X	X	X	X	X	X	VID	X
FLASH 1 Hardware Reset	X	X	H	H	X	X	X	X	X	X	High-Z	High-Z	L	X	X
FLASH 2 Hardware Reset	X	X	H	H	X	X	X	X	X	X	High-Z	High-Z	X	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
PSRAM Power[7] Down Program	H	H	H	H	X	X	X	X	L	Valid	High-Z	High-Z	H	H	X
PSRAM No Read	H	H	L	H	L	H	H	H	H	Valid	High-Z	High-Z	H	H	X
PSRAM Power Down[8]	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X

Legend : L = VIL, H = VIH, X = VIL or VIH. See “DC CHARACTERISTICS” for voltage levels.

Notes:

1. Other operations except for indicated this column are prohibited.
2. Do not apply $\overline{CE}$f = VIL, $\overline{CE}$1r = VIL and CE2r = VIH all at once.
3. PSRAM Output Disable condition should not be kept longer than 1ms.
4. $\overline{WE}$ can be VIL if $\overline{OE}$ is VIL, $\overline{OE}$ at VIH initiates the write operations.
5. PSRAM $\overline{LB}$,$\overline{UB}$ control at Read operation is not supported.
6. It is also used for the extended sector group protections.
7. The PSRAM Power Down Program can be performed one time after compliance of Power-UP timings and it should not be re-programmed after regular Read or Write.
8. PSRAM Power Down mode can be entered from Standby state and all DQ pins are in High-Z state. IPDr current and data retention depends on the selection of Power Down Program.
9. Either or both $\overline{LB}$ and $\overline{UB}$ must be Low for PSRAM Read Operation.
10. Can be either VIL or VIH but must be valid before Read or Write.
11. See “ PSRAM Power Down Program Key Table “ located in the next page.
12. Protect “ outer most “ 2x8K bytes (4 words) on both ends of the boot block sectors.

ABSOLUTE MAXIMUM RATINGS(1,5)

Symbol	Parameter	Rating Min.	Rating Max.	Unit
Tstg	Storage Temperature	–55	+125	℃
T_A	Ambient Temperature with Power Applied	–30	+85	°C
V_{IN},V_{OUT}	Voltage with Respect to Ground All Pins(2)	–0.3	V_{CC} + 0.3(6)	V
V_{ccf1},V_{ccf2}	V_{ccf} Supply(2)	–0.3	3.5	V
V_{ccr}	V_{ccr} Supply(2)	–0.3	3.5	V
V_{IN}	$\overline{RESET1}$, $\overline{RESET2}$(3)	-0.5	+13.0	V
V_{ACC}	$\overline{WP}$/ACC(4)	–0.5	+10.5	V

Notes:

1. Voltage is defined on the basis of GND = 0 V.
2. Minimum DC voltage on input or I/O pins is -0.3 V. During voltage transitions, input or I/O pins may undershoot GND to -1.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{ccf1}+ 0.3V , V_{ccf2}+ 0.3V or VCCr + 0.3 V. During voltage transitions, input or I/O pins may overshoot to V_{ccf1}+ 2.0V , V_{ccf2}+ 2.0 V or VCCr + 1.0 V for periods of up to 20 ns.
3. Minimum DC input voltage on $\overline{RESET1}$ or $\overline{RESET2}$ pin is -0.5 V. During voltage transitions, $\overline{RESET1}$ or $\overline{RESET2}$ pin may undershoot GND to -2.0 V for periods of up to 20 ns.
   The voltage difference between input and supply voltage (VIN-V_{ccf1} or V_{ccf2}) does not exceed 9.0 V.
   The maximum DC input voltage on the $\overline{RESET}$ pin is +13.0 V that may overshoot to +14.0 V for periods of up to 20 ns.
4. Minimum DC input voltage on $\overline{WP}$/ACC pin is -0.5 V. During voltage transitions, $\overline{WP}$/ACC pin may undershoot GND to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{WP}$/ACC pin is +10.5 V which may overshoot to +12.0 V for periods of up to 20 ns, when V_{ccf1} or V_{ccf2} is applied.
5. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
6. This Vcc refers to the minimum of V_{ccf1}, V_{ccf2}, or V_{ccr} .

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating Min.	Rating Max.	Unit
T_A	Ambient Temperature	–30	+85	°C
V_{ccf1},V_{ccf2}	V_{ccf} Supply Voltages	2.7	3.3	V
V_{ccr}	V_{ccr} Supply Voltages	2.7	3.3	V

Note:

Voltage is defined on the basis of GND = 0 V.

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage	V_{IN}=GND to Vccf, Vccr		-1.0	—	+1.0	µA
I_{LO}	Output Leakage	V_{OUT}=GND to Vccf, Vccr		-1.0	—	+1.0	µA
I_{LIT}	$\overline{RESET}$ Inputs Leakage Current	Vccf=Vccf max., $\overline{RESET}$ = 12.5V		—	—	35	µA
$I_{CC}1f$	FLASH Vcc [1] Active Current (Read)	$\overline{CE}$f=V_{IL}, $\overline{OE}$=V_{IH}	tCycle = 5Mhz	—	—	18	mA
			tCycle = 1Mhz	—	—	4	mA
$I_{CC}2f$	FLASH Vcc Active[2] Current(Program/Erase)	$\overline{CE}$f=V_{IL}, $\overline{OE}$=V_{IH}		—	—	35	mA
$I_{CC}3f$	FLASH Vcc Active[5] Current (Read-While-Program)	$\overline{CE}$f=V_{IL}, $\overline{OE}$=V_{IH}		—	—	53	mA
$I_{CC}4f$	FLASH Vcc Active[5] Current (Read-While-Erase)	$\overline{CE}$f=V_{IL}, $\overline{OE}$=V_{IH}		—	—	53	mA
$I_{CC}5f$	FLASH Vcc Active Current (Erase-Suspend-Program)	$\overline{CE}$f=V_{IL}, $\overline{OE}$=V_{IH}		—	—	40	mA
I_{ACC}	$\overline{WP}$/ACC Acceleration Program Current	Vccf = Vcc max, $\overline{WP}$/ACC = V_{ACC} max		—	—	20	mA
$I_{CC}1r$	PSRAM Vcc Active Current	Vccr = Vccr max, $\overline{CE}$1r=V_{IL}, CE2r=V_{IH}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0 mA	trc / twc = min	—	—	25	mA
			trc / twc = 1 µs	—	—	3	mA
$I_{SB}1f$	FLASH Vcc Standby Current[7]	Vccf = Vccf max, $\overline{CE}$f= Vccf ± 0.3V, $\overline{RESET}$ = Vccf ± 0.3V, $\overline{WP}$/ACC = Vccf ± 0.3V		—	1	5	µA
$I_{SB}2f$	FLASH Vcc [7] Standby Current ($\overline{RESET}$)	Vccf = Vccf max, $\overline{RESET}$= GND ± 0.3V, $\overline{WP}$/ACC = Vccf ± 0.3V		—	1	5	µA
$I_{SB}3f$	FLASH Vcc [3,7] Current (Automatic Sleep Mode)	Vccf = Vccf max, $\overline{CE}$f = GND ± 0.3V, $\overline{RESET}$ = Vccf ± 0.3V, $\overline{WP}$/ACC = Vccf ± 0.3V, V_{IN} = Vccf ± 0.3V or GND ± 0.3V		—	1	5	µA
$I_{SB}1r$	PSRAM Vcc Standby[8] Current	Vccr = Vccr max, $\overline{CE}$1r ≥ Vccr -0.2V, CE2r ≥ Vccr -0.2V, V_{IN} ≤ 0.2 V or V_{IN} ≥ Vccr -0.2V		—	—	110	µA
$I_{PDS}r$	PSRAM Vcc Power Down Current (Sleep Mode)	Vccr = Vccr max., $\overline{CE}$1r ≥ Vccr - 0.2 V CE2r ≤ 0.2 V, V_{IN} Cycle time = t_{RC} min		—	—	10	µA
$I_{PDN}r$	PSRAM Vcc Power [8] Down Current (Nap Mode)	Vccr = Vccr max., $\overline{CE}$1r ≥ Vccr - 0.2 V CE2r ≤ 0.2 V, V_{IN} Cycle time = t_{RC} min		—	—	65	µA

DC CHARACTERISTICS (Continued)

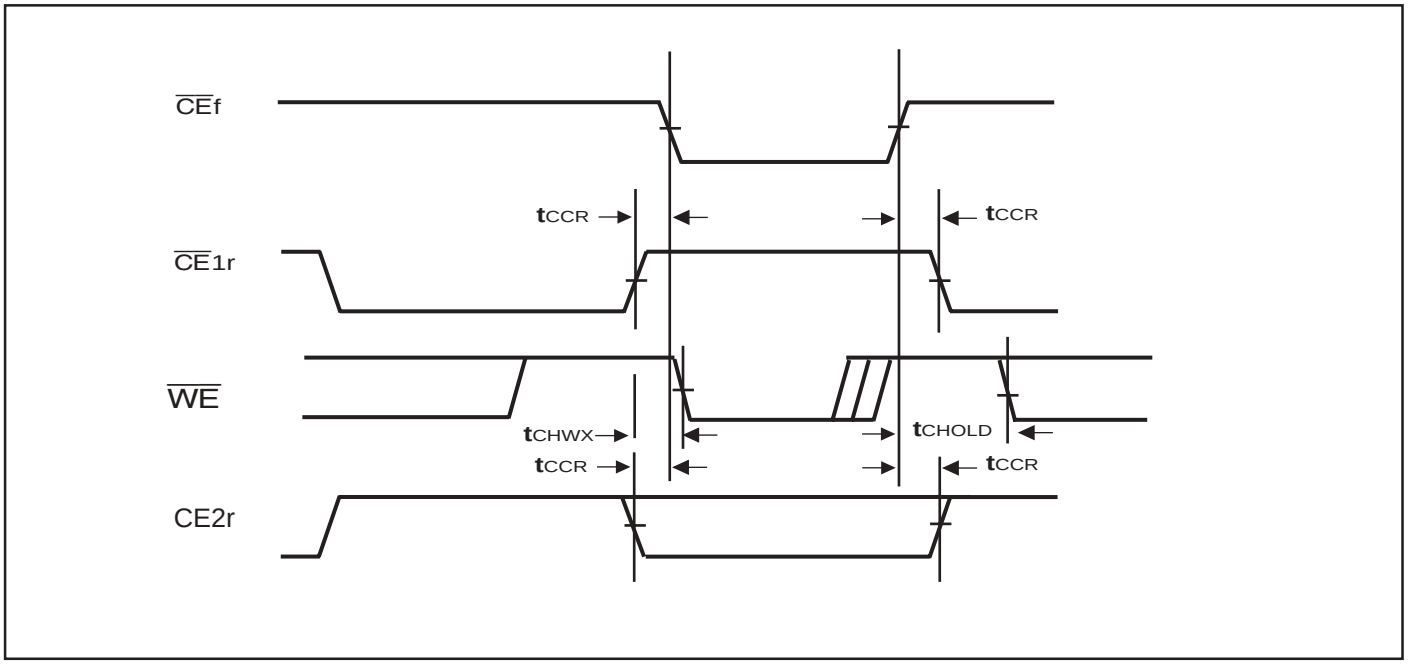
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{PD8r}	PSRAM V_{CC} Power Down Current (8M Partial)[8]	V_{CCr} = V_{CCr} max., $\overline{CE1}r \geq V_{CCr}$ - 0.2 V CE2r ≤ 0.2 V, V_{IN} Cycle time = t_{RC} min	—	—	80	µA
V_{IL}	Input Low Level		-0.3	—	0.5	V
V_{IH}	Input High Level (FLASH 1 or FLASH 2)		V_{CCf} x 0.75	—	V_{CCf} ± 0.3	V
V_{IH}	Input High Level (PSRAM)		V_{CCr} x 0.75	—	V_{CCr} ± 0.3	V
V_{ID}	Voltage for Sector Protection and Temp. Unprotection($\overline{RESET}$)[4]		11.5	—	12.5	V
V_{ACC}	Voltage for $\overline{WP}$/ACC Sector Protection/Unprotection and Program Acceleration [4]		8.5	9.0	9.5	V
V_{OL}	Output Low Level (PSRAM)	V_{CCr} = V_{CCr} min., V_{CCS}=V_{CCS} min. I_{OL} = 1.0 mA	—	—	0.4	V
V_{OH}	Output High Level (PSRAM)	V_{CCr} = V_{CCr} min., V_{CCS}=V_{CCS} min. I_{OH} = -0.5 mA	2.2	—	—	V
V_{OL}	Output Low Level (Flash)	V_{CCf} = V_{CCf} min., V_{CCS}=V_{CCS} min. I_{OL} = 4.0 mA	—	—	0.45	V
V_{OH}	Output High Level (Flash)	V_{CCf} = V_{CCf} min., V_{CCS}=V_{CCS} min. I_{OH} = -0.1 mA	V_{CCf} - 0.4	—	—	V
V_{LKO}	FLASH Low Vccf Lock-Out Voltage		2.3	2.4	2.5	V

Notes:
1. ICC current listed includes both the DC operating current and the frequency dependent component.
2. ICC active while Embedded Algorithm (program or erase) is in progress.
3. Automatic sleep mode enables the low power mode when address remains stable for 150 ns.
4. Applicable for only VCCf applying.
5. Embedded Algorithm (program or erase) is in progress. (@5 MHz)
6. ISB2 r depends on VIN cycle time. Please refer to “APPENDIX A”.
7. Standby current listed is for each FLASH chip.
8. Standby and Power down currents are reduced with $V_{CCr} \leq 3.0$ V .

AC CHARACTERISTICS - $\overline{CE}$ TIMING

Parameter	Symbol	Condition	Min	Max	Unit
$\overline{CE}$f Recover Time	t_{CCR}	—	0	—	ns
$\overline{CE}$f Hold Time	t_{CHOLD}	—	3	—	ns
$\overline{CE}$1r High to $\overline{WE}$ Invalid time for Standby Entry	t_{CHWX}	—	10	—	ns

TIMING DIAGRAM FOR ALTERNATING PSRAM TO FLASH 1 OR FLASH 2



FLEXIBLE SECTOR-ERASE ARCHITECTURE ON FLASH 1 or FLASH 2

Bank	Sector Address	K-Word	Address	Bank	Sector Address	K-Word	Address
Bank A	SA0	4	000000h	Bank B	SA36	32	0E8000h
Bank A	SA1	4	001000h	Bank B	SA37	32	0F0000h
Bank A	SA2	4	002000h	Bank B	SA38	32	0F8000h
Bank A	SA3	4	003000h	Bank B	SA39	32	100000h
Bank A	SA4	4	004000h	Bank B	SA40	32	108000h
Bank A	SA5	4	005000h	Bank B	SA41	32	110000h
Bank A	SA6	4	006000h	Bank B	SA42	32	118000h
Bank A	SA7	4	007000h	Bank B	SA43	32	120000h
Bank A	SA8	32	008000h	Bank B	SA44	32	128000h
Bank A	SA9	32	010000h	Bank B	SA45	32	130000h
Bank A	SA10	32	018000h	Bank B	SA46	32	138000h
Bank A	SA11	32	020000h	Bank B	SA47	32	140000h
Bank A	SA12	32	028000h	Bank B	SA48	32	148000h
Bank A	SA13	32	030000h	Bank B	SA49	32	150000h
Bank A	SA14	32	038000h	Bank B	SA50	32	158000h
Bank A	SA15	32	040000h	Bank B	SA51	32	160000h
Bank A	SA16	32	048000h	Bank B	SA52	32	168000h
Bank A	SA17	32	050000h	Bank B	SA53	32	170000h
Bank A	SA18	32	058000h	Bank B	SA54	32	178000h
Bank A	SA19	32	060000h	Bank B	SA55	32	180000h
Bank A	SA20	32	068000h	Bank B	SA56	32	188000h
Bank A	SA21	32	070000h	Bank B	SA57	32	190000h
Bank A	SA22	32	078000h	Bank B	SA58	32	198000h
Bank B	SA23	32	080000h	Bank B	SA59	32	1A0000h
Bank B	SA24	32	088000h	Bank B	SA60	32	1A8000h
Bank B	SA25	32	090000h	Bank B	SA61	32	1B0000h
Bank B	SA26	32	098000h	Bank B	SA62	32	1B8000h
Bank B	SA27	32	0A0000h	Bank B	SA63	32	1C0000h
Bank B	SA28	32	0A8000h	Bank B	SA64	32	1C8000h
Bank B	SA29	32	0B0000h	Bank B	SA65	32	1D0000h
Bank B	SA30	32	0B8000h	Bank B	SA66	32	1D8000h
Bank B	SA31	32	0C0000h	Bank B	SA67	32	1E0000h
Bank B	SA32	32	0C8000h	Bank B	SA68	32	1E8000h
Bank B	SA33	32	0D0000h	Bank B	SA69	32	1F0000h
Bank B	SA34	32	0D8000h	Bank B	SA70	32	1F8000h
Bank B	SA35	32	0E0000h	Bank C	SA71	32	200000h

FLEXIBLE SECTOR-ERASE ARCHITECTURE ON FLASH 1 or FLASH 2 (Continued)

Bank	Sector Address	K-Word	Address	Bank	Sector Address	K-Word	Address
Bank C	SA72	32	208000h	Bank C	SA107	32	320000h
Bank C	SA73	32	210000h	Bank C	SA108	32	328000h
Bank C	SA74	32	218000h	Bank C	SA109	32	330000h
Bank C	SA75	32	220000h	Bank C	SA110	32	338000h
Bank C	SA76	32	228000h	Bank C	SA111	32	340000h
Bank C	SA77	32	230000h	Bank C	SA112	32	348000h
Bank C	SA78	32	238000h	Bank C	SA113	32	350000h
Bank C	SA79	32	240000h	Bank C	SA114	32	358000h
Bank C	SA80	32	248000h	Bank C	SA115	32	360000h
Bank C	SA81	32	250000h	Bank C	SA116	32	368000h
Bank C	SA82	32	258000h	Bank C	SA117	32	370000h
Bank C	SA83	32	260000h	Bank C	SA118	32	378000h
Bank C	SA84	32	268000h	Bank D	SA119	32	380000h
Bank C	SA85	32	270000h	Bank D	SA120	32	388000h
Bank C	SA86	32	278000h	Bank D	SA121	32	390000h
Bank C	SA87	32	280000h	Bank D	SA122	32	398000h
Bank C	SA89	32	290000h	Bank D	SA124	32	3A8000h
Bank C	SA90	32	298000h	Bank D	SA125	32	3B0000h
Bank C	SA91	32	2A0000h	Bank D	SA126	32	3B8000h
Bank C	SA92	32	2A8000h	Bank D	SA127	32	3C0000h
Bank C	SA93	32	2B0000h	Bank D	SA128	32	3C8000h
Bank C	SA94	32	2B8000h	Bank D	SA129	32	3D0000h
Bank C	SA95	32	2C0000h	Bank D	SA130	32	3D8000h
Bank C	SA96	32	2C8000h	Bank D	SA131	32	3E0000h
Bank C	SA97	32	2D0000h	Bank D	SA132	32	3E8000h
Bank C	SA98	32	2D8000h	Bank D	SA133	32	3F0000h
Bank C	SA99	32	2E0000h	Bank D	SA134	4	3F8000h
Bank C	SA100	32	2E8000h	Bank D	SA135	4	3F9000h
Bank C	SA101	32	2F0000h	Bank D	SA136	4	3FA000h
Bank C	SA102	32	2F8000h	Bank D	SA137	4	3FB000h
Bank C	SA103	32	300000h	Bank D	SA138	4	3FC000h
Bank C	SA104	32	308000h	Bank D	SA139	4	3FD000h
Bank C	SA105	32	310000h	Bank D	SA140	4	3FE000h
Bank C	SA106	32	318000h	Bank D	SA141	4	3FF000h

USER CONFIGURABLE BANK ARCHITECTURE TABLE - FLASH 1 or FLASH 2

	Virtual Bank 1		Virtual Bank 2	
Bank Split	**Volume**	**Combination**	**Volume**	**Combination**
Choice 1	8 Mbit	Bank A	56 Mbit	Bank B, C, D
Choice 2	24 Mbit	Bank B	40 Mbit	Bank A, C, D
Choice 3	24 Mbit	Bank C	40 Mbit	Bank A, B, D
Choice 4	8 Mbit	Bank D	56 Mbit	Bank A, B, C

EXAMPLE OF VIRTUAL BANKS COMBINATION TABLE - FLASH 1 or FLASH 2

	Virtual Bank 1			Virtual Bank 2		
Bank Split	**Volume**	**Combination**	**Sector Size**	**Volume**	**Combination**	**Sector Size**
Choice 1	8 Mbit	Bank A	8x4 Kword 15x32 Kword	56 Mbit	Bank B, C, D	8x4 Kword 111x32 Kword
Choice 2	16 Mbit	Bank A,D	16x4 Kword 30x32 Kword	48 Mbit	Bank B,C	96x32 Kword
Choice 3	24 Mbit	Bank B	48x32 Kword	40 Mbit	Bank A, C, D	16x4 Kword 78x32 Kword
Choice 4	32 Mbit	Bank A,B	8x4 Kword 63x32 Kword	32 Mbit	Bank C,D	8x4 Kword 63x32 Kword

Notes:

1) When multiple sector erase over several banks is operated, the system cannot read out of the bank to which a sector being erased belongs. For example, if erasing is taking place at both Bank A and Bank B, neither Bank A nor Bank B is read out. They would output the sequence flag once they were selected. Meanwhile the system would get to read from either Bank C or Bank D.

2) Each word is made-up of 2 bytes: one upper byte and one lower byte. A KWord is 2^{10} words.

SIMULTANEOUS OPERATION TABLE - FLASH 1 or FLASH 2

Case	Virtual Bank 1 Status	Virtual Bank 2 Status
1	Read Mode	Read Mode
2	Read Mode	Autoselect Mode
3	Read Mode	Program Mode
4	Read Mode	Erase Mode (1)
5	Autoselect Mode	Read Mode
6	Program Mode	Read Mode
7	Erase Mode (1)	Read Mode

Note:

1) By writing erase suspend command on the bank address of sector being erased, the erase operation gets suspended so that it enables reading from or programming the remaining sectors.
2) Bank 1 and Bank 2 are divided for the sake of convenience at Simultaneous Operation. Actually, the Bank consists of 4 banks, Bank A, Bank B, Bank C, and Bank D. Bank Address (BA) means to specify each of the Banks.

SECTOR ADDRESS TABLE - FLASH 1 or FLASH 2

		Bank Address			Sector Address							Address Range
Bank	**Sector**	**A21**	**A20**	**A19**	**A18**	**A17**	**A16**	**A15**	**A14**	**A13**	**A12**	**Word Mode**
Bank A	SA0	0	0	0	0	0	0	0	0	0	0	000000h to 000FFFh
Bank A	SA1	0	0	0	0	0	0	0	0	0	1	001000h to 001FFFh
Bank A	SA2	0	0	0	0	0	0	0	0	1	0	002000h to 002FFFh
Bank A	SA3	0	0	0	0	0	0	0	0	1	1	003000h to 003FFFh
Bank A	SA4	0	0	0	0	0	0	0	1	0	0	004000h to 004FFFh
Bank A	SA5	0	0	0	0	0	0	0	1	0	1	005000h to 005FFFh
Bank A	SA6	0	0	0	0	0	0	0	1	1	0	006000h to 006FFFh
Bank A	SA7	0	0	0	0	0	0	0	1	1	1	007000h to 007FFFh
Bank A	SA8	0	0	0	0	0	0	1	X	X	X	008000h to 00FFFFh
Bank A	SA9	0	0	0	0	0	1	0	X	X	X	010000h to 017FFFh
Bank A	SA10	0	0	0	0	0	1	1	X	X	X	018000h to 01FFFFh
Bank A	SA11	0	0	0	0	1	0	0	X	X	X	020000h to 027FFFh
Bank A	SA12	0	0	0	0	1	0	1	X	X	X	028000h to 02FFFFh
Bank A	SA13	0	0	0	0	1	1	0	X	X	X	030000h to 037FFFh
Bank A	SA14	0	0	0	0	1	1	1	X	X	X	038000h to 03FFFFh
Bank A	SA15	0	0	0	1	0	0	0	X	X	X	040000h to 047FFFh
Bank A	SA16	0	0	0	1	0	0	1	X	X	X	048000h to 04FFFFh
Bank A	SA17	0	0	0	1	0	1	0	X	X	X	050000h to 057FFFh
Bank A	SA18	0	0	0	1	0	1	1	X	X	X	058000h to 05FFFFh
Bank A	SA19	0	0	0	1	1	0	0	X	X	X	060000h to 067FFFh
Bank A	SA20	0	0	0	1	1	0	1	X	X	X	068000h to 06FFFFh
Bank A	SA21	0	0	0	1	1	1	0	X	X	X	070000h to 077FFFh
Bank A	SA22	0	0	0	1	1	1	1	X	X	X	078000h to 07FFFFh
Bank B	SA23	0	0	1	0	0	0	0	X	X	X	080000h to 087FFFh
Bank B	SA24	0	0	1	0	0	0	1	X	X	X	088000h to 08FFFFh
Bank B	SA25	0	0	1	0	0	1	0	X	X	X	090000h to 097FFFh
Bank B	SA26	0	0	1	0	0	1	1	X	X	X	098000h to 09FFFFh
Bank B	SA27	0	0	1	0	1	0	0	X	X	X	0A0000h to 0A7FFFh
Bank B	SA28	0	0	1	0	1	0	1	X	X	X	0A8000h to 0AFFFFh
Bank B	SA29	0	0	1	0	1	1	0	X	X	X	0B0000h to 0B7FFFh
Bank B	SA30	0	0	1	0	1	1	1	X	X	X	0B8000h to 0BFFFFh
Bank B	SA31	0	0	1	1	0	0	0	X	X	X	0C0000h to 0C7FFFh
Bank B	SA32	0	0	1	1	0	0	1	X	X	X	0C8000h to 0CFFFFh

SECTOR ADDRESS TABLE - FLASH 1 or FLASH 2 (Continued)

		Bank Address			Sector Address							Address Range
Bank	**Sector**	**A21**	**A20**	**A19**	**A18**	**A17**	**A16**	**A15**	**A14**	**A13**	**A12**	**Word Mode**
Bank B	SA33	0	0	1	1	0	1	0	X	X	X	0D0000h to 0D7FFFh
Bank B	SA34	0	0	1	1	0	1	1	X	X	X	0D8000h to 0DFFFFh
Bank B	SA35	0	0	1	1	1	0	0	X	X	X	0E0000h to 0E7FFFh
Bank B	SA36	0	0	1	1	1	0	1	X	X	X	0E8000h to 0EFFFFh
Bank B	SA37	0	0	1	1	1	1	0	X	X	X	0F0000h to 0F7FFFh
Bank B	SA38	0	0	1	1	1	1	1	X	X	X	0F8000h to 0FFFFFh
Bank B	SA39	0	1	0	0	0	0	0	X	X	X	100000h to 107FFFh
Bank B	SA40	0	1	0	0	0	0	1	X	X	X	108000h to 10FFFFh
Bank B	SA41	0	1	0	0	0	1	0	X	X	X	110000h to 117FFFh
Bank B	SA42	0	1	0	0	0	1	1	X	X	X	118000h to 11FFFFh
Bank B	SA43	0	1	0	0	1	0	0	X	X	X	120000h to 127FFFh
Bank B	SA44	0	1	0	0	1	0	1	X	X	X	128000h to 12FFFFh
Bank B	SA45	0	1	0	0	1	1	0	X	X	X	130000h to 137FFFh
Bank B	SA46	0	1	0	0	1	1	1	X	X	X	138000h to 13FFFFh
Bank B	SA47	0	1	0	1	0	0	0	X	X	X	140000h to 147FFFh
Bank B	SA48	0	1	0	1	0	0	1	X	X	X	148000h to 14FFFFh
Bank B	SA49	0	1	0	1	0	1	0	X	X	X	150000h to 157FFFh
Bank B	SA50	0	1	0	1	0	1	1	X	X	X	158000h to 15FFFFh
Bank B	SA51	0	1	0	1	1	0	0	X	X	X	160000h to 167FFFh
Bank B	SA52	0	1	0	1	1	0	1	X	X	X	168000h to 16FFFFh
Bank B	SA53	0	1	0	1	1	1	0	X	X	X	170000h to 177FFFh
Bank B	SA54	0	1	0	1	1	1	1	X	X	X	178000h to 17FFFFh
Bank B	SA55	0	1	1	0	0	0	0	X	X	X	180000h to 187FFFh
Bank B	SA56	0	1	1	0	0	0	1	X	X	X	188000h to 18FFFFh
Bank B	SA57	0	1	1	0	0	1	0	X	X	X	190000h to 197FFFh
Bank B	SA58	0	1	1	0	0	1	1	X	X	X	198000h to 19FFFFh
Bank B	SA59	0	1	1	0	1	0	0	X	X	X	1A0000h to 1A7FFFh
Bank B	SA60	0	1	1	0	1	0	1	X	X	X	1A8000h to 1AFFFFh
Bank B	SA61	0	1	1	0	1	1	0	X	X	X	1B0000h to 1B7FFFh
Bank B	SA62	0	1	1	0	1	1	1	X	X	X	1B8000h to 1BFFFFh
Bank B	SA63	0	1	1	1	0	0	0	X	X	X	1C0000h to 1C7FFFh
Bank B	SA64	0	1	1	1	0	0	1	X	X	X	1C8000h to 1CFFFFh
Bank B	SA65	0	1	1	1	0	1	0	X	X	X	1D0000h to 1D7FFFh

SECTOR ADDRESS TABLE - FLASH 1 or FLASH 2 (Continued)

		Bank Address			Sector Address							Address Range
Bank	**Sector**	**A21**	**A20**	**A19**	**A18**	**A17**	**A16**	**A15**	**A14**	**A13**	**A12**	**Word Mode**
Bank B	SA66	0	1	1	1	0	1	1	X	X	X	1D8000h to 1DFFFFh
Bank B	SA67	0	1	1	1	1	0	0	X	X	X	1E0000h to 1E7FFFh
Bank B	SA68	0	1	1	1	1	0	1	X	X	X	1E8000h to 1EFFFFh
Bank B	SA69	0	1	1	1	1	1	0	X	X	X	1F0000h to 1F7FFFh
Bank B	SA70	0	1	1	1	1	1	1	X	X	X	1F8000h to 1FFFFFh
Bank C	SA71	1	0	0	0	0	0	0	X	X	X	200000h to 207FFFh
Bank C	SA72	1	0	0	0	0	0	1	X	X	X	208000h to 20FFFFh
Bank C	SA73	1	0	0	0	0	1	0	X	X	X	210000h to 217FFFh
Bank C	SA74	1	0	0	0	0	1	1	X	X	X	218000h to 21FFFFh
Bank C	SA75	1	0	0	0	1	0	0	X	X	X	220000h to 227FFFh
Bank C	SA76	1	0	0	0	1	0	1	X	X	X	228000h to 22FFFFh
Bank C	SA77	1	0	0	0	1	1	0	X	X	X	230000h to 237FFFh
Bank C	SA78	1	0	0	0	1	1	1	X	X	X	238000h to 23FFFFh
Bank C	SA79	1	0	0	1	0	0	0	X	X	X	240000h to 247FFFh
Bank C	SA80	1	0	0	1	0	0	1	X	X	X	248000h to 24FFFFh
Bank C	SA81	1	0	0	1	0	1	0	X	X	X	250000h to 257FFFh
Bank C	SA82	1	0	0	1	0	1	1	X	X	X	258000h to 25FFFFh
Bank C	SA83	1	0	0	1	1	0	0	X	X	X	260000h to 267FFFh
Bank C	SA84	1	0	0	1	1	0	1	X	X	X	268000h to 26FFFFh
Bank C	SA85	1	0	0	1	1	1	0	X	X	X	270000h to 277FFFh
Bank C	SA86	1	0	0	1	1	1	1	X	X	X	278000h to 27FFFFh
Bank C	SA87	1	0	1	0	0	0	0	X	X	X	280000h to 287FFFh
Bank C	SA88	1	0	1	0	0	0	1	X	X	X	288000h to 28FFFFh
Bank C	SA89	1	0	1	0	0	1	0	X	X	X	290000h to 297FFFh
Bank C	SA90	1	0	1	0	0	1	1	X	X	X	298000h to 29FFFFh
Bank C	SA91	1	0	1	0	1	0	0	X	X	X	2A0000h to 2A7FFFh
Bank C	SA92	1	0	1	0	1	0	1	X	X	X	2A8000h to 2AFFFFh
Bank C	SA93	1	0	1	0	1	1	0	X	X	X	2B0000h to 2B7FFFh
Bank C	SA94	1	0	1	0	1	1	1	X	X	X	2B8000h to 2BFFFFh
Bank C	SA95	1	0	1	1	0	0	0	X	X	X	2C0000h to 2C7FFFh
Bank C	SA96	1	0	1	1	0	0	1	X	X	X	2C8000h to 2CFFFFh
Bank C	SA97	1	0	1	1	0	1	0	X	X	X	2D0000h to 2D7FFFh
Bank C	SA98	1	0	1	1	0	1	1	X	X	X	2D8000h to 2DFFFFh
Bank C	SA99	1	0	1	1	1	0	0	X	X	X	2E0000h to 2E7FFFh

SECTOR ADDRESS TABLE - FLASH 1 or FLASH 2 (Continued)

		Bank Address			Sector Address							Address Range
Bank	**Sector**	**A21**	**A20**	**A19**	**A18**	**A17**	**A16**	**A15**	**A14**	**A13**	**A12**	**Word Mode**
Bank C	SA100	1	0	1	1	1	0	1	X	X	X	2E8000h to 2EFFFFh
Bank C	SA101	1	0	1	1	1	1	0	X	X	X	2F0000h to 2F7FFFh
Bank C	SA102	1	0	1	1	1	1	1	X	X	X	2F8000h to 2FFFFFh
Bank C	SA103	1	1	0	0	0	0	0	X	X	X	300000h to 307FFFh
Bank C	SA104	1	1	0	0	0	0	1	X	X	X	308000h to 30FFFFh
Bank C	SA105	1	1	0	0	0	1	0	X	X	X	310000h to 317FFFh
Bank C	SA106	1	1	0	0	0	1	1	X	X	X	318000h to 31FFFFh
Bank C	SA107	1	1	0	0	1	0	0	X	X	X	320000h to 327FFFh
Bank C	SA108	1	1	0	0	1	0	1	X	X	X	328000h to 32FFFFh
Bank C	SA109	1	1	0	0	1	1	0	X	X	X	330000h to 337FFFh
Bank C	SA110	1	1	0	0	1	1	1	X	X	X	338000h to 33FFFFh
Bank C	SA111	1	1	0	1	0	0	0	X	X	X	340000h to 347FFFh
Bank C	SA112	1	1	0	1	0	0	1	X	X	X	348000h to 34FFFFh
Bank C	SA113	1	1	0	1	0	1	0	X	X	X	350000h to 357FFFh
Bank C	SA114	1	1	0	1	0	1	1	X	X	X	358000h to 35FFFFh
Bank C	SA115	1	1	0	1	1	0	0	X	X	X	360000h to 367FFFh
Bank C	SA116	1	1	0	1	1	0	1	X	X	X	368000h to 36FFFFh
Bank C	SA117	1	1	0	1	1	1	0	X	X	X	370000h to 377FFFh
Bank C	SA118	1	1	0	1	1	1	1	X	X	X	378000h to 37FFFFh
Bank D	SA119	1	1	1	0	0	0	0	X	X	X	380000h to 387FFFh
Bank D	SA120	1	1	1	0	0	0	1	X	X	X	388000h to 38FFFFh
Bank D	SA121	1	1	1	0	0	1	0	X	X	X	390000h to 397FFFh
Bank D	SA122	1	1	1	0	0	1	1	X	X	X	398000h to 39FFFFh
Bank D	SA123	1	1	1	0	1	0	0	X	X	X	3A0000h to 3A7FFFh
Bank D	SA124	1	1	1	0	1	0	1	X	X	X	3A8000h to 3AFFFFh
Bank D	SA125	1	1	1	0	1	1	0	X	X	X	3B0000h to 3B7FFFh
Bank D	SA126	1	1	1	0	1	1	1	X	X	X	3B8000h to 3BFFFFh
Bank D	SA127	1	1	1	1	0	0	0	X	X	X	3C0000h to 3C7FFFh
Bank D	SA128	1	1	1	1	0	0	1	X	X	X	3C8000h to 3CFFFFh
Bank D	SA129	1	1	1	1	0	1	0	X	X	X	3D0000h to 3D7FFFh
Bank D	SA130	1	1	1	1	0	1	1	X	X	X	3D8000h to 3DFFFFh
Bank D	SA131	1	1	1	1	1	0	0	X	X	X	3E0000h to 3E7FFFh
Bank D	SA132	1	1	1	1	1	0	1	X	X	X	3E8000h to 3EFFFFh
Bank D	SA133	1	1	1	1	1	1	0	X	X	X	3F0000h to 3F7FFFh
Bank D	SA134	1	1	1	1	1	1	1	0	0	0	3F8000h to 3F8FFFh
Bank D	SA135	1	1	1	1	1	1	1	0	0	1	3F9000h to 3F9FFFh
Bank D	SA136	1	1	1	1	1	1	1	0	1	0	3FA000h to 3FAFFFh
Bank D	SA137	1	1	1	1	1	1	1	0	1	1	3FB000h to 3FBFFFh
Bank D	SA138	1	1	1	1	1	1	1	1	0	0	3FC000h to 3FCFFFh
Bank D	SA139	1	1	1	1	1	1	1	1	0	1	3FD000h to 3FDFFFh
Bank D	SA140	1	1	1	1	1	1	1	1	1	0	3FE000h to 3FEFFFh
Bank D	SA141	1	1	1	1	1	1	1	1	1	1	3FF000h to 3FFFFFh

SECTOR ADDRESS GROUP TABLE - FLASH 1 or FLASH 2

Sector	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	Sectors
SGA0	0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0	0 1 1	1 0 1	X	X	X	SA8 to SA10
SGA9	0	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	0	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	0	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	0	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA16	0	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA17	0	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA18	0	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA19	0	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA20	0	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA21	0	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA22	0	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA23	0	1	1	1	1	X	X	X	X	X	SA67 to SA70
SGA24	1	0	0	0	0	X	X	X	X	X	SA71 to SA74
SGA25	1	0	0	0	1	X	X	X	X	X	SA75 to SA78
SGA26	1	0	0	1	0	X	X	X	X	X	SA79 to SA82
SGA27	1	0	0	1	1	X	X	X	X	X	SA83 to SA86
SGA28	1	0	1	0	0	X	X	X	X	X	SA87 to SA90
SGA29	1	0	1	0	1	X	X	X	X	X	SA91 to SA94
SGA30	1	0	1	1	0	X	X	X	X	X	SA95 to SA98
SGA31	1	0	1	1	1	X	X	X	X	X	SA99 to SA102
SGA32	1	1	0	0	0	X	X	X	X	X	SA103 to SA106

SECTOR ADDRESS GROUP TABLE - FLASH 1 or FLASH 2 (Continued)

Sector	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	Sectors
SGA33	1	1	0	0	1	X	X	X	X	X	SA107 to SA110
SGA34	1	1	0	1	0	X	X	X	X	X	SA111 to SA114
SGA35	1	1	0	1	1	X	X	X	X	X	SA115 to SA118
SGA36	1	1	1	0	0	X	X	X	X	X	SA119 to SA122
SGA37	1	1	1	0	1	X	X	X	X	X	SA123 to SA126
SGA38	1	1	1	1	0	X	X	X	X	X	SA127 to SA130
SGA39	1	1	1	1	1	0 0 1	0 1 0	X	X	X	SA131 to SA133
SGA40	1	1	1	1	1	1	1	0	0	0	SA134
SGA41	1	1	1	1	1	1	1	0	0	1	SA135
SGA42	1	1	1	1	1	1	1	0	1	0	SA136
SGA43	1	1	1	1	1	1	1	0	1	1	SA137
SGA44	1	1	1	1	1	1	1	1	0	0	SA138
SGA45	1	1	1	1	1	1	1	1	0	1	SA139
SGA46	1	1	1	1	1	1	1	1	1	0	SA140
SGA47	1	1	1	1	1	1	1	1	1	1	SA141

FLASH MEMORY AUTOSELECT CODES TABLE - FLASH 1 or FLASH 2

Type	A21 to A12	A6	A3	A2	A1	A0	Code (HEX)
Manufacturer's Code	BA	L	L	L	L	L	04h
Device Code	BA	L	L	L	L	H	227Eh
Extended Device	BA	L	H	H	H	L	2202h
Code[2]	BA	L	H	H	H	H	2201h
Sector Group	Sector Group	L	L	L	H	L	01h[1]
Protection	Address						

Legend: L = VIL, H = VIH. See " DC CHARACTERISTICS" for voltage levels.

Notes:

1. Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.
2. A read cycle at address (BA) 01h outputs device code. When 227Eh was output, this indicates that there will require two additional codes, called Extended Device Codes. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh.

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FLASH MEMORY COMMAND DEFINITIONS - FLASH 1 or FLASH 2

Command Sequence	Bus Write Cycle Req'd	First Bus Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write		Fifth Bus Cycle		Sixth Bus Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read / Reset (1)	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Read / Reset (1)	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
Autoselect	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
Program Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Program Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
Erase Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Erase Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—
Extended Sector Group Protection (3)	4	XXXh	60h	SGA	60h	SGA	40h	SGA	SD	—	—	—	—
Set to Fast Mode (2)	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
Fast Program (2)	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode (2)	2	BA	90h	XXXh	(6) F0H	—	—	—	—	—	—	—	—
Query (4)	1	(BA) 55h	98h	—	—	—	—	—	—	—	—	—	—
Hi-ROM Entry	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—
Hi-ROM Program (5)	4	555h	AAh	2AAh	55h	555h	A0h	(HRA) PA	PD	—	—	—	—
Hi-ROM Exit (5)	4	555h	AAh	2AAh	55h	(HRBA) 555h	90h	XXXh	00h	—	—	—	—

Notes:
1. Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
2. This command is valid during Fast Mode.
3. This command is valid while $\overline{\text{RESET}}$ = V_{ID}
4. The valid address is A6 to A0.
5. This command is valid during Hi-ROM mode.
6. The data “00h” is also acceptable.

FLASH MEMORY COMMAND DEFINITIONS - FLASH 1 or FLASH 2 (Continued)

Notes:

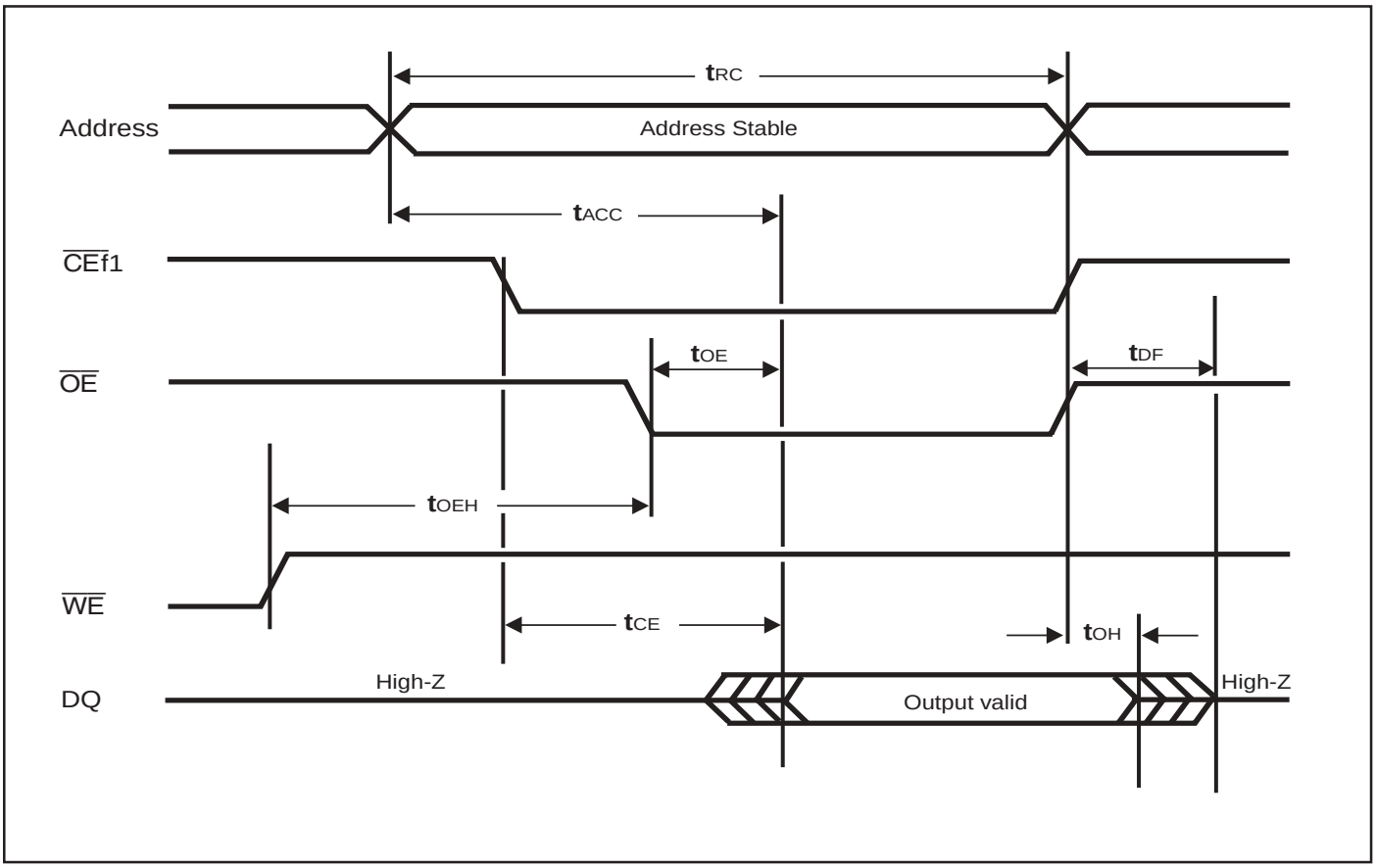
- Address bits A21 to A11 = X = “H” or “L” for all address commands except or Program Address (PA), Sector Address (SA), and Bank Address (BA), and Sector Group Address (SPA).
- Bus operations are defined in "DEVICE BUS OPERATIONS”.
- RA = Address of the memory location to be read
  PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the write pulse.
- SA = Address of the sector to be erased. The combination of A21, A20, A19, A18, A17, A16, A15, A14, A13, and A12 will uniquely select any sector. BA = Bank Address (A21, A20, A19)
- RD = Data read from location RA during read operation.
  PD = Data to be programmed at location PA. Data is latched on the rising edge of the write pulse.
- SPA = Sector group address to be protected. Set sector group address and (A6, A3, A2, A1, A0) = (0, 0, 0, 1, 0).
  SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.
- HRA = Address of the Hi-ROM area : 000000h to 00007Fh
  HRBA = Bank Address of the Hi-ROM area (A21 = A20 = A19 = VIL)
- The system should generate the following address patterns : 555h or 2AAh to addresses A10 to A0
- Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
- Command combinations not described in *FLASH Memory Command Definitions* are illegal.

FLASH READ ONLY OPERATIONS CHARACTERISTICS - FLASH 1 or FLASH 2

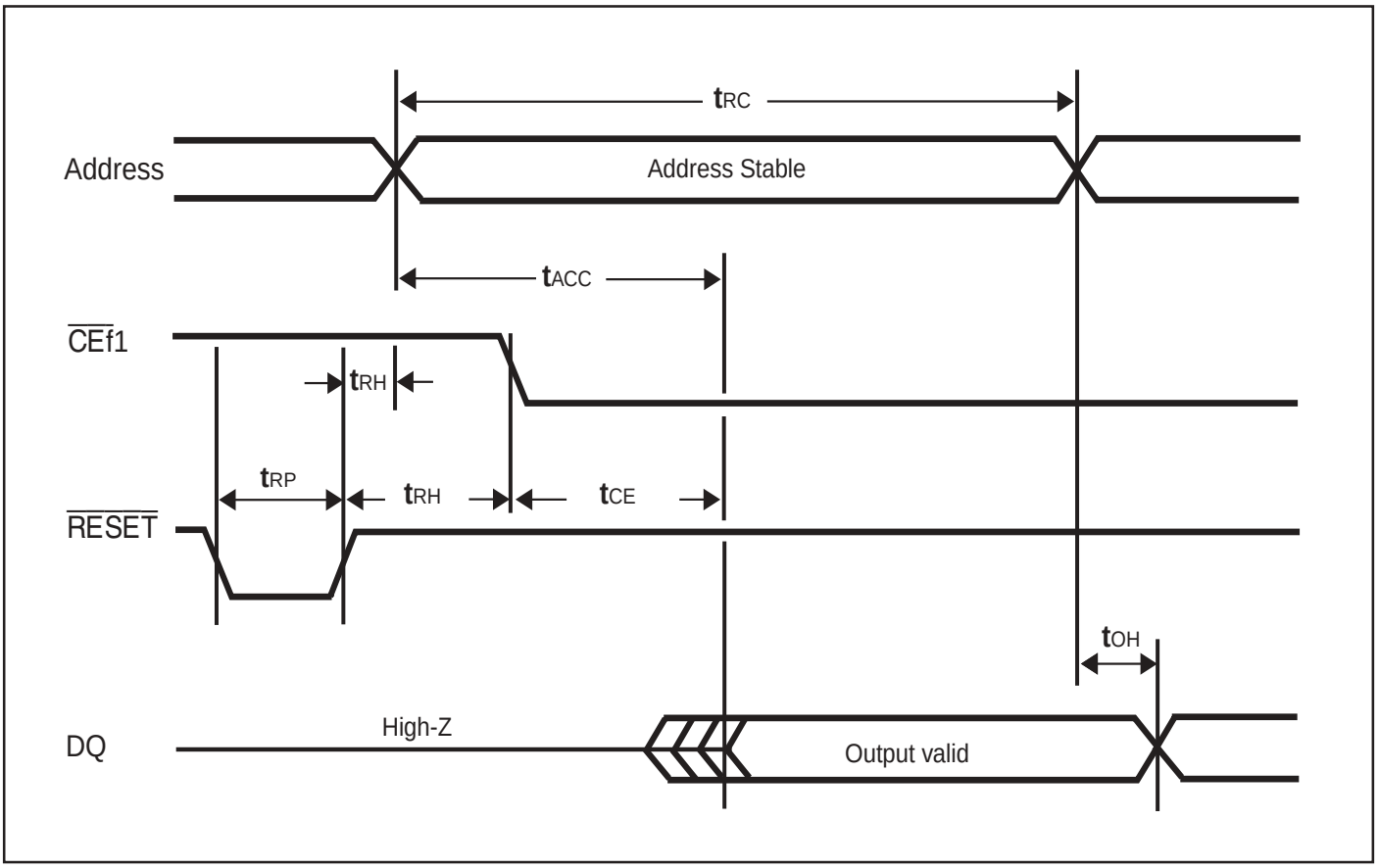
Parameter	JEDEC Symbol	Standard Symbol	Condition	Min	Max	Unit
Read Cycle Time	t_{AVAV}	t_{RC}		70	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE}f = V_{IL}$, $\overline{OE} = V_{IL}$	—	70	ns
Chip Enable to Output Delay	t_{ELQV}	t_{CE}	$\overline{OE} = V_{IL}$	—	70	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}		—	30	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}		—	25	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}		—	25	ns
Output Hold Time From Addresses, $\overline{CE}f$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}		0	—	ns
$\overline{RESET}$ Pin Low to Read Mode	—	t_{READY}		—	20	µs

Test Conditions:
Output Load : 1 TTL gate and 30 pF
Input rise and fall times : 5 ns
Input pulse levels : 0.0 V or VCCf
Timing measurement reference level
Input : VCCf/2
Output : VCCf/2

FLASH READ CYCLE - FLASH 1 or FLASH 2



FLASH HARDWARE $\overline{\text{RESET}}$ / READ OPERATION TIMING DIAGRAM - FLASH 1 or FLASH 2



FLASH WRITE/ERASE/PROGRAM OPERATIONS - FLASH 1 or FLASH 2

Parameter	JEDEC Symbol	Standard Symbol	Min	Typ	Max	Unit
Write Cycle Time	t_{AVAV}	t_{WC}	70	—	—	ns
Address Setup Time	t_{AVWL}	t_{AS}	0	—	—	ns
Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling	—	t_{ASO}	12	—	—	ns
Address Hold Time	t_{WLAX}	t_{AH}	45	—	—	ns
Address Hold Time from $\overline{CE}$f or $\overline{OE}$ High During Toggle Bit Polling	—	t_{AHT}	0	—	—	ns
Data Setup Time	t_{DVWH}	t_{DS}	30	—	—	ns
Data Hold Time	t_{WHDX}	t_{DH}	0	—	—	ns
Output Enable Hold Time Read	—	t_{OEH}	0	—	—	ns
Output Enable Hold Time Toggle and $\overline{Data}$ Polling	—	t_{OEH}	10	—	—	ns
$\overline{CE}$f High During Toggle Bit Polling	—	t_{CEPH}	20	—	—	ns
$\overline{OE}$ High During Toggle Bit Polling	—	t_{OEPH}	20	—	—	ns
Read Recover Time Before Write ($\overline{OE}$ to $\overline{CE}$f)	t_{GHWL}	t_{GHWL}	0	—	—	ns
Read Recover Time Before Write ($\overline{OE}$ to $\overline{WE}$)	t_{GHEL}	t_{GHEL}	0	—	—	ns
$\overline{WE}$ Setup Time ($\overline{CE}$f to $\overline{WE}$)	t_{WLEL}	t_{WS}	0	—	—	ns
$\overline{CE}$f Setup Time ($\overline{WE}$ to $\overline{CE}$f)	t_{ELWL}	t_{CS}	0	—	—	ns
$\overline{WE}$ Hold Time ($\overline{CE}$f to $\overline{WE}$)	t_{EHWH}	t_{WH}	0	—	—	ns
$\overline{CE}$f Hold Time ($\overline{WE}$ to $\overline{CE}$f)	t_{WHEH}	t_{CH}	0	—	—	ns
Write Pulse Width	t_{WHWL}	t_{WP}	35	—	—	ns
$\overline{CE}$f Pulse Width	t_{ELEH}	t_{CP}	35	—	—	ns
Write Pulse Width High	t_{WHWL}	t_{WP}	25	—	—	ns
$\overline{CE}$f Pulse Width High	t_{EHEL}	t_{CPH}	25	—	—	ns
Word Programming Operation (1)	t_{WHWH1}	t_{WHWH1}	—	6	100	µs
Sector Erase Operation (1)	t_{WHWH2}	t_{WHWH2}	—	0.5	2.0	s
V_{CC} Setup Time	—	t_{VCS}	50	—	—	µs
Rise Time to V_{ID} (2)	—	t_{VIDR}	500	—	—	ns
Rise Time to V_{ACC} (3)	—	t_{VACCR}	500	—	—	ns
Voltage Transition Time (2)	—	t_{VLHT}	4	—	—	µs
Write Pulse Width (2)	—	t_{WPP}	100	—	—	µs

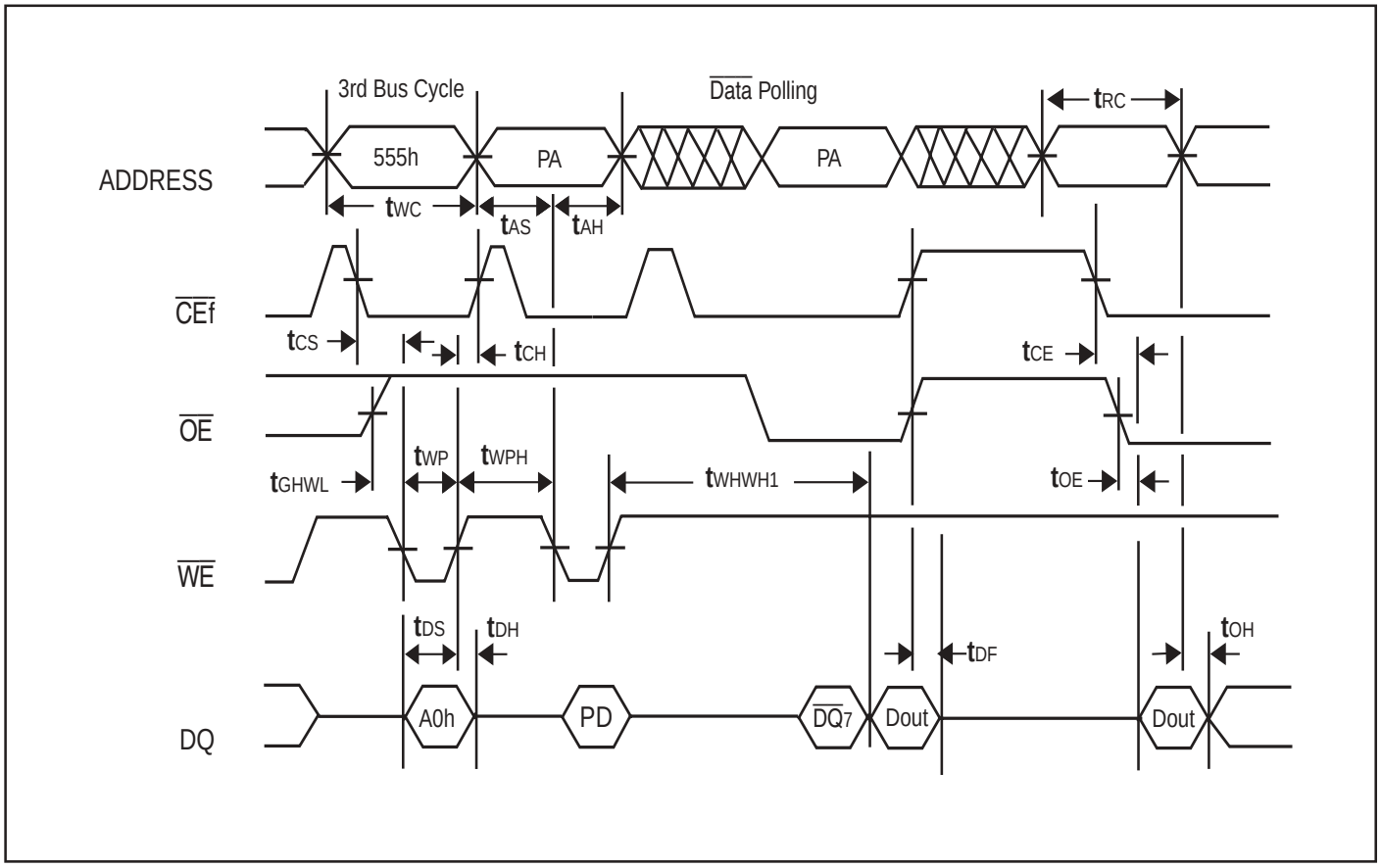
FLASH WRITE/ERASE/PROGRAM OPERATIONS - FLASH 1 or FLASH 2 (Continued)

Parameter	JEDEC Symbol	Standard Symbol	Min	Typ	Max	Unit
$\overline{OE}$ Setup Time to $\overline{WE}$ Active (2)	—	t_{OESP}	4	—	—	µs
$\overline{CE}_f$ Setup Time to $\overline{WE}$ Active (2)	—	t_{CSP}	4	—	—	µs
Recover Time from RY/$\overline{BY}$	—	t_{RB}	0	—	—	ns
$\overline{RESET}$ Pulse Width	—	t_{RP}	500	—	—	ns
$\overline{RESET}$ High Level Period Before Read	—	t_{RH}	200	—	—	ns
Program/Erase Valid to RY/$\overline{BY}$ $\overline{Delay}$	—	t_{BUSY}	—	—	90	ns
Delay Time from Embedded Output Enable	—	t_{EOE}	—	—	70	ns
Erase Time-Out Time	—	t_{TOW}	50	—	—	µs
Erase Suspend Transition Time	—	t_{SPD}	—	—	20	µs

Notes:
1. Does not include preprogramming time.
2. For Sector Group Protection operation.
3. For Accelerated Program operation.

FLASH WRITE CYCLE - FLASH 1 or FLASH 2

($\overline{WE}$ CONTROL)

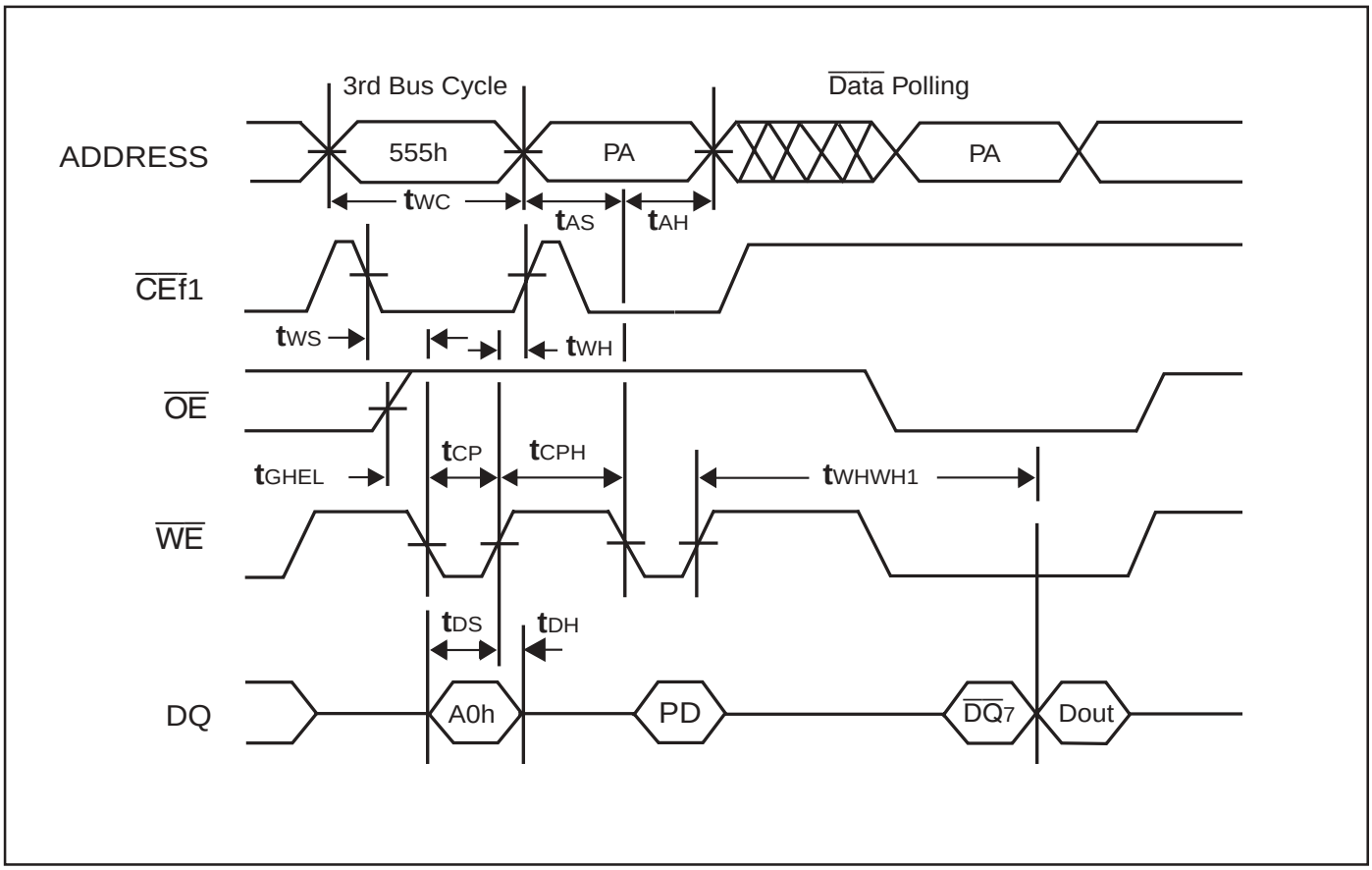


Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ}7$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.

FLASH WRITE CYCLE - FLASH 1 or FLASH 2

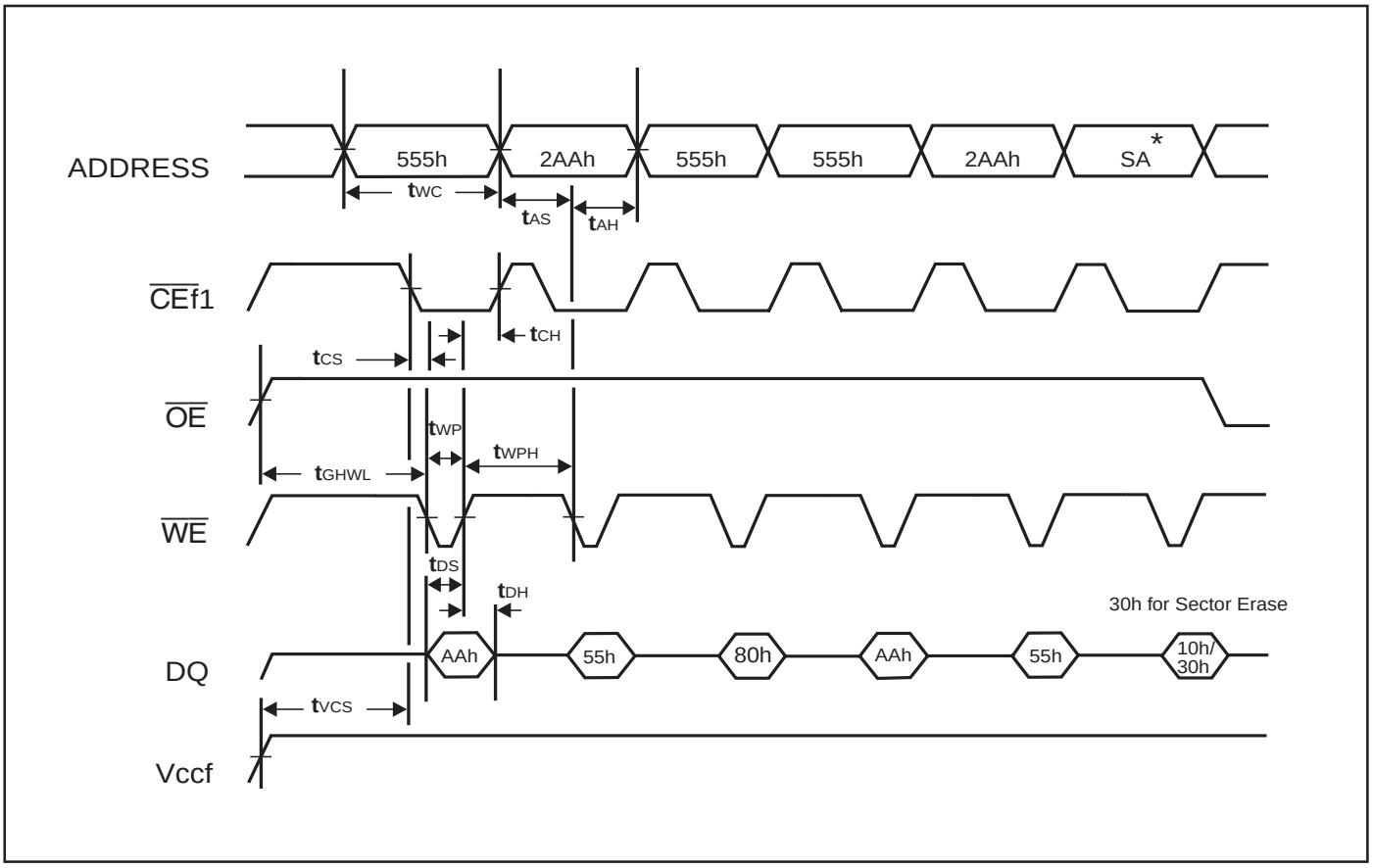
($\overline{CE}$f CONTROL)



Notes:

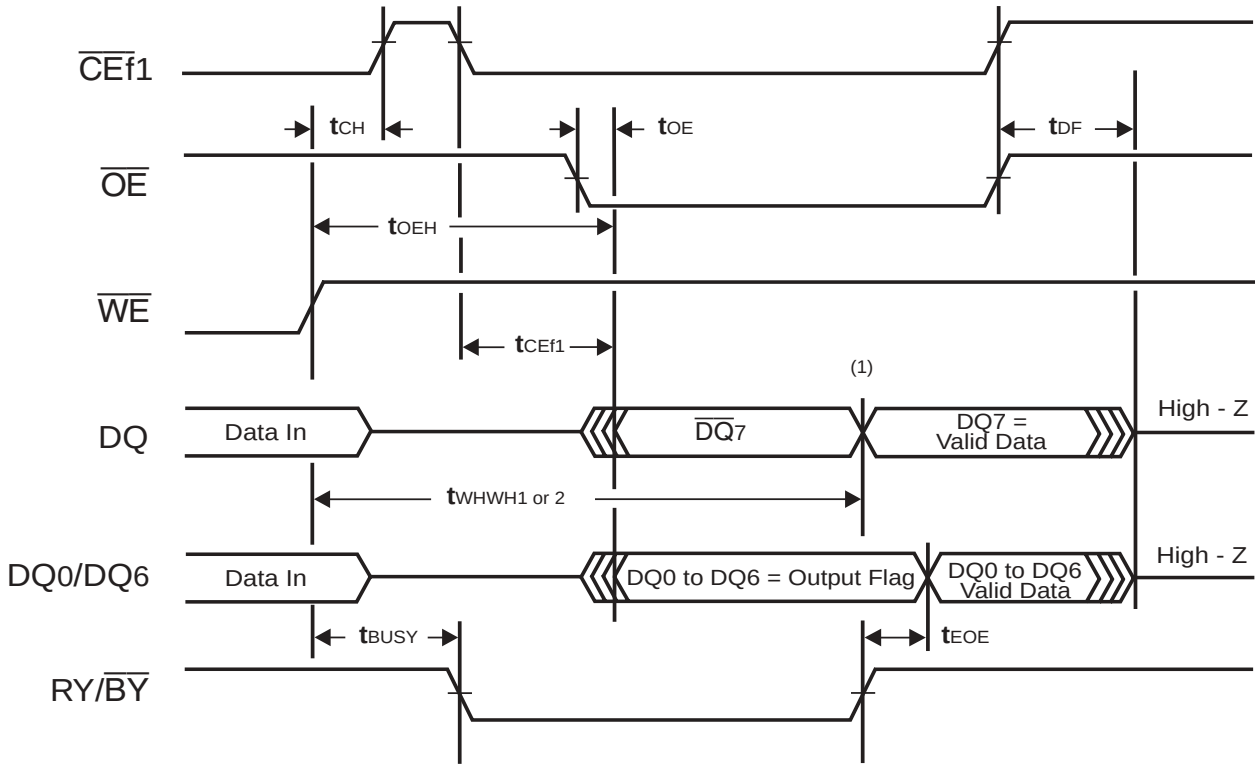
1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ}$7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.

FLASH AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS - FLASH 1 or FLASH 2



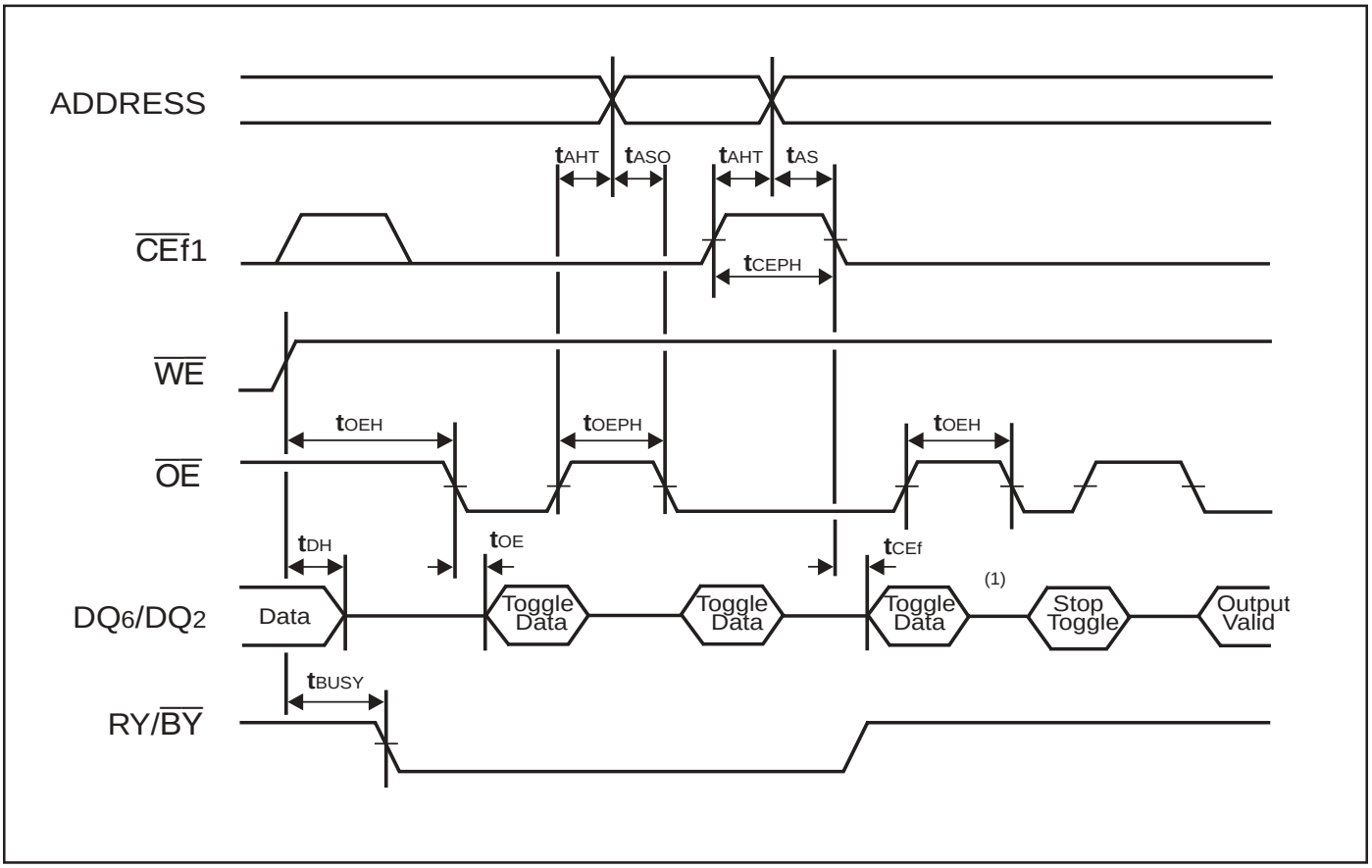
Notes:
1. SA is the sector address for Sector Erase. Address = 555h for Chip Erase.

FLASH AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS - FLASH 1 or FLASH 2



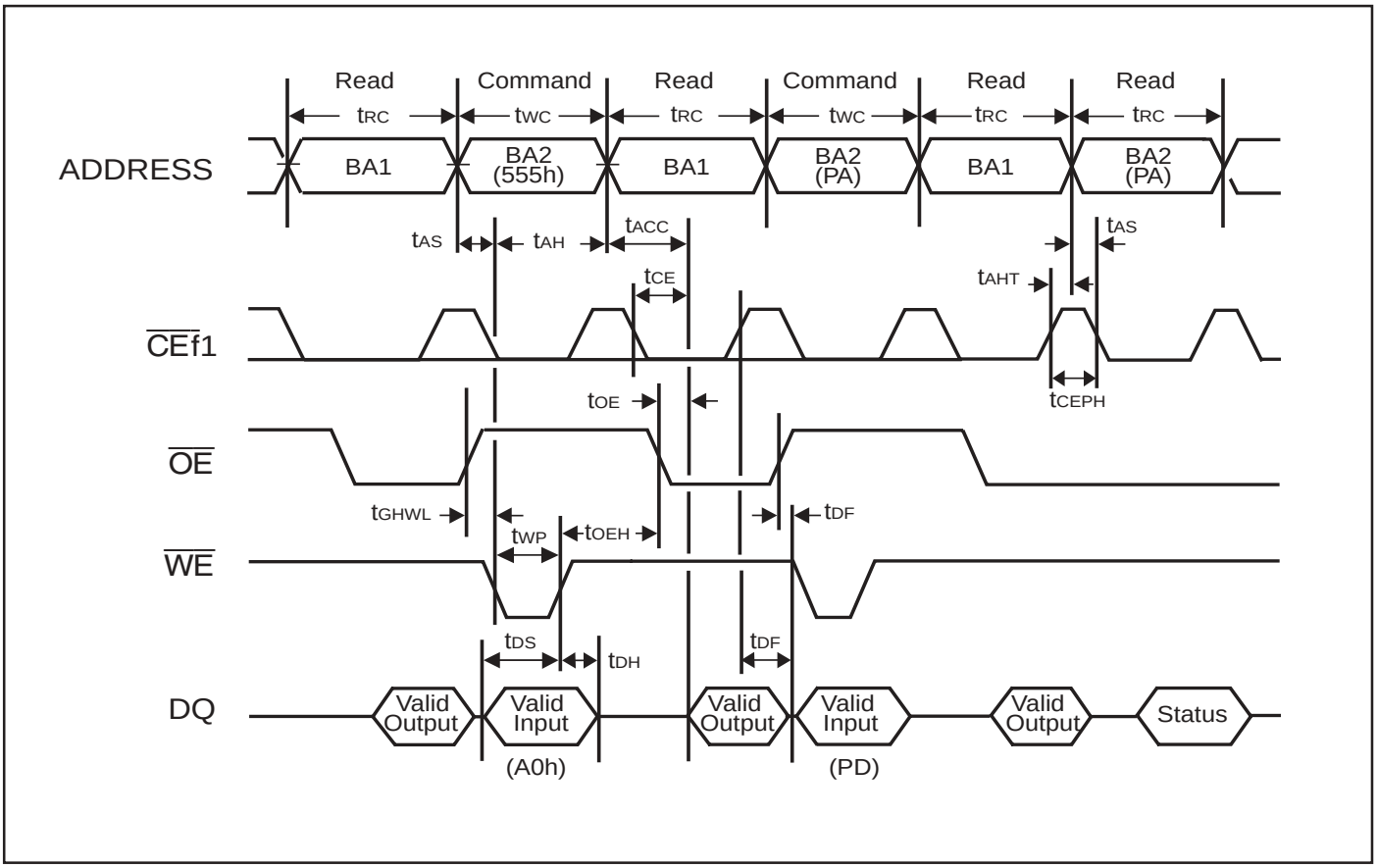
Notes:
1. $\overline{\text{DQ}}7$ = Valid Data (the device has completed the Embedded operation.)

FLASH AC WAVEFORMS
FOR TOGGLE BIT DURING EMBEDDED ALGORITHM OPERATIONS - FLASH 1 or FLASH 2



Notes:
1. DQ6 stops toggling (the device has completed the Embedded operation).

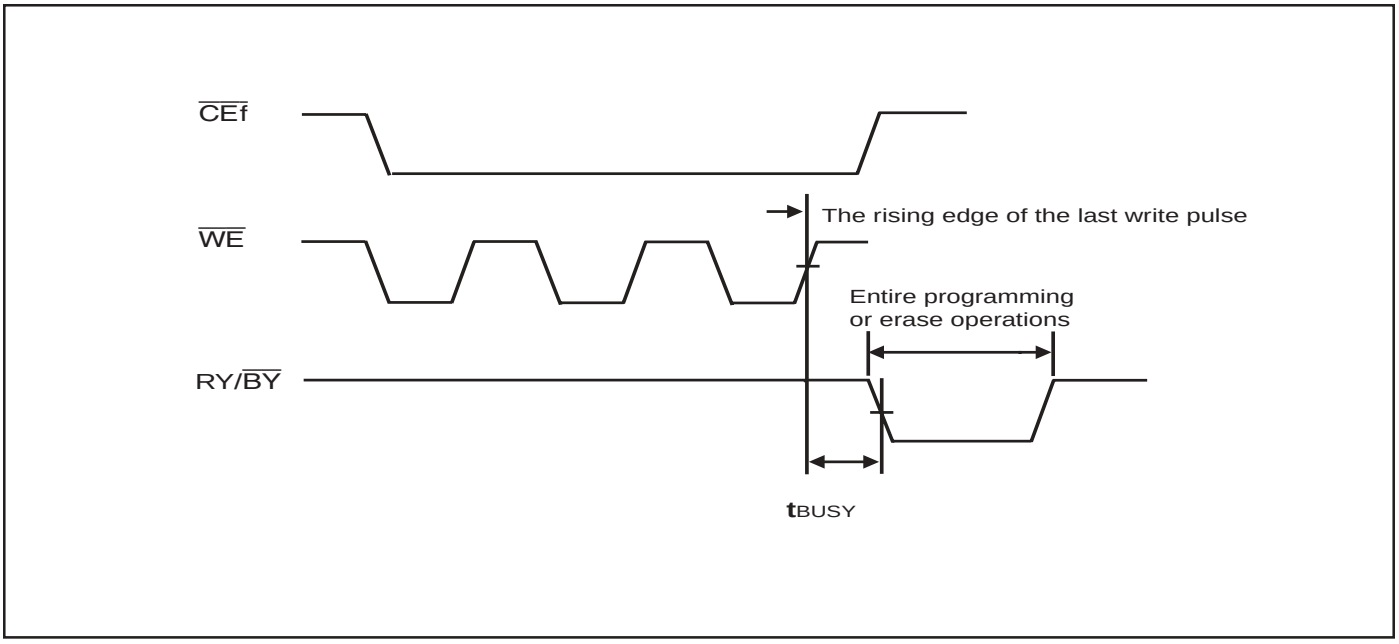
FLASH BACK-to-BACK READ/WRITE TIMING DIAGRAM - FLASH 1 or FLASH 2



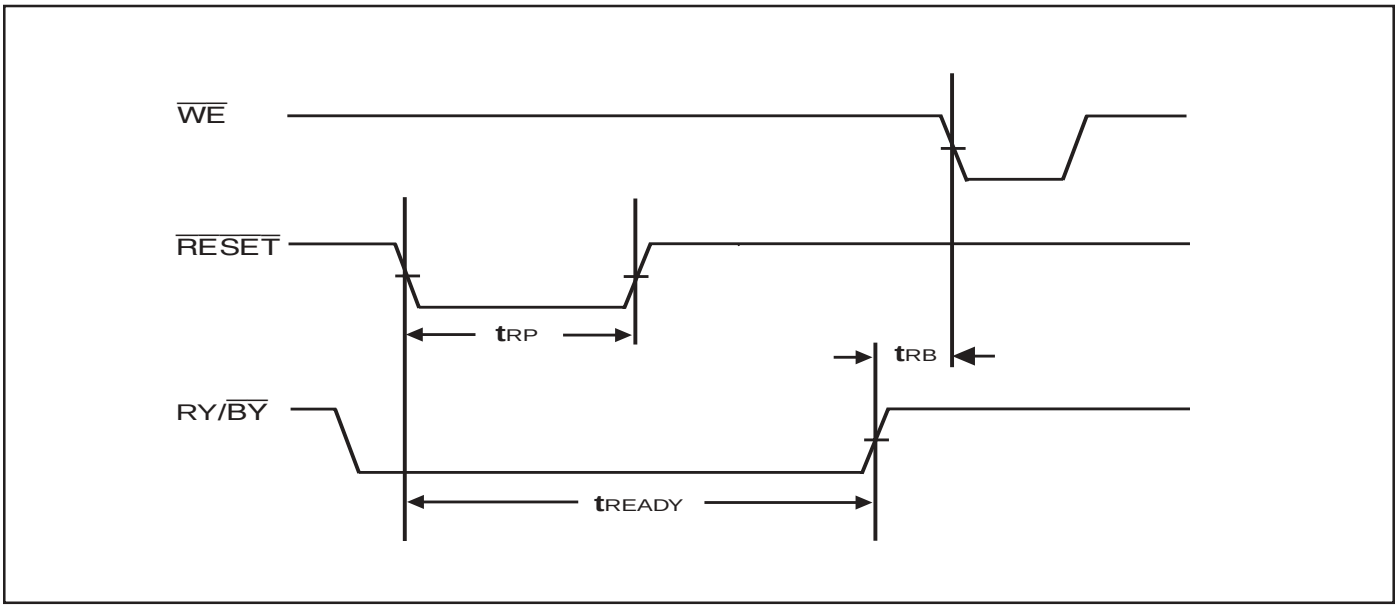
Note:

1. This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
   BA1: Address of Virtual Bank 1.
   BA2: Address of Virtual Bank 2.

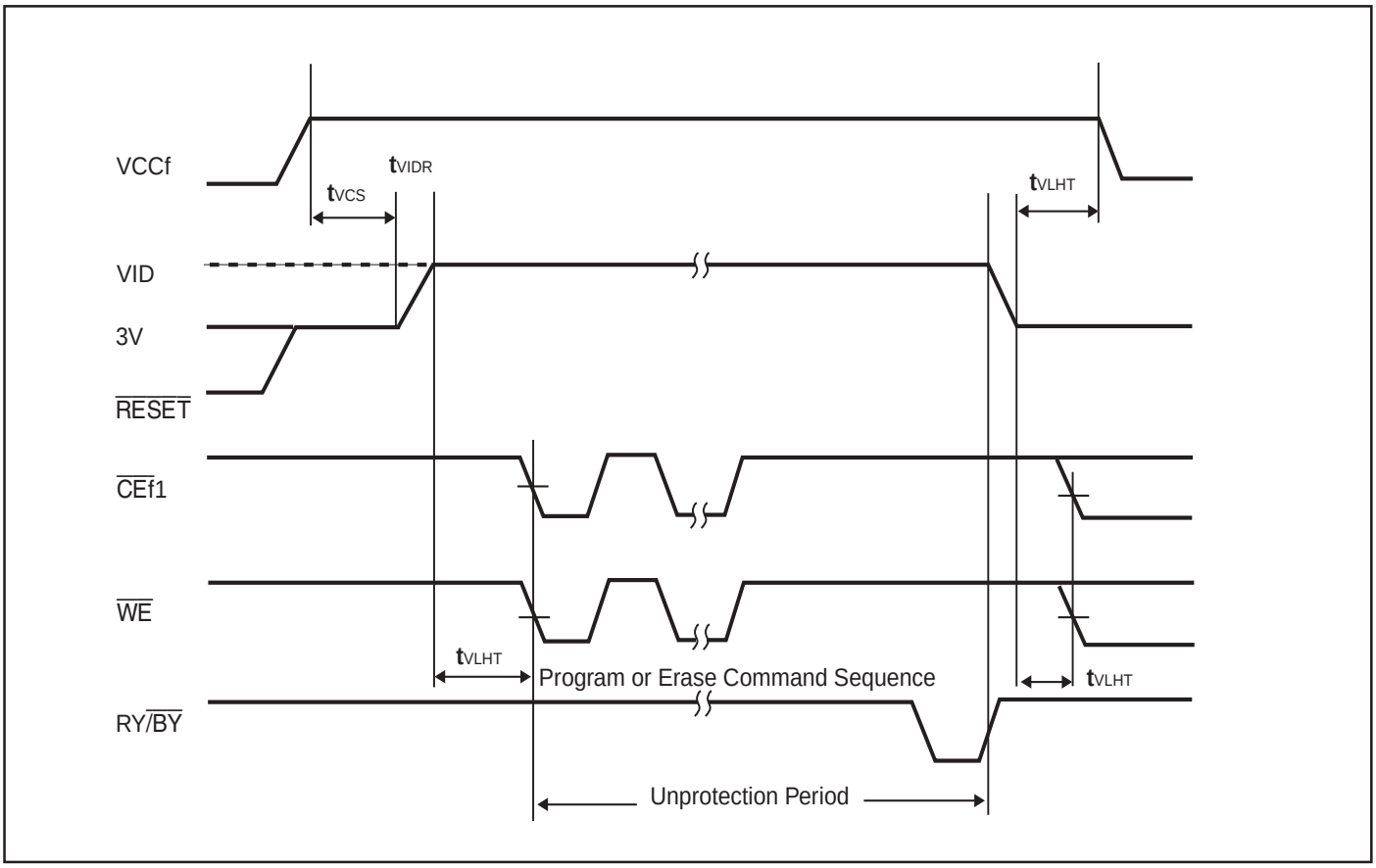
FLASH RY/$\overline{BY}$ TIMING DIAGRAM DURING WRITE/ERASE OPERATIONS - FLASH 1 or FLASH 2



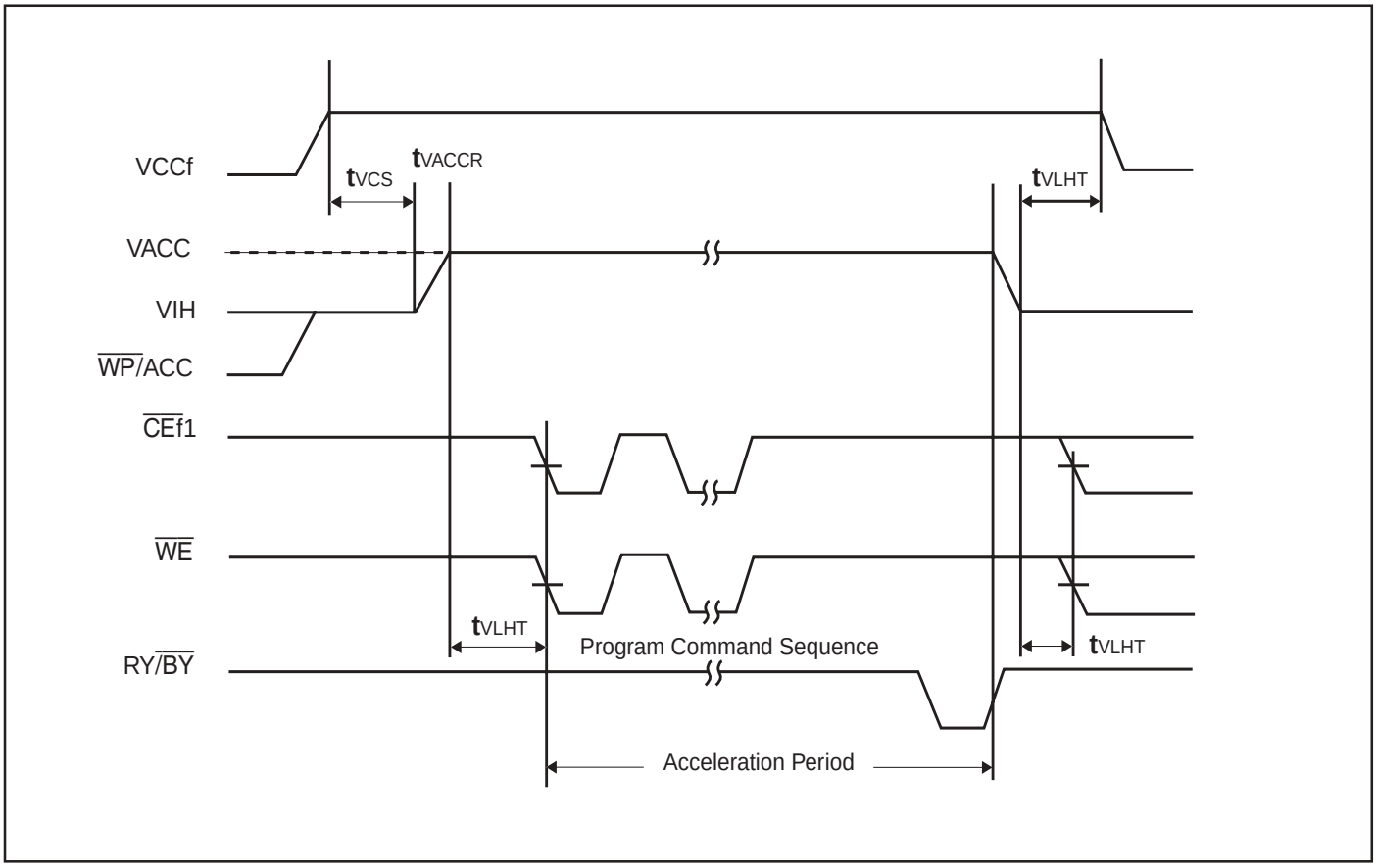
FLASH $\overline{RESET}$, RY/$\overline{BY}$ TIMING DIAGRAM - FLASH 1 or FLASH 2



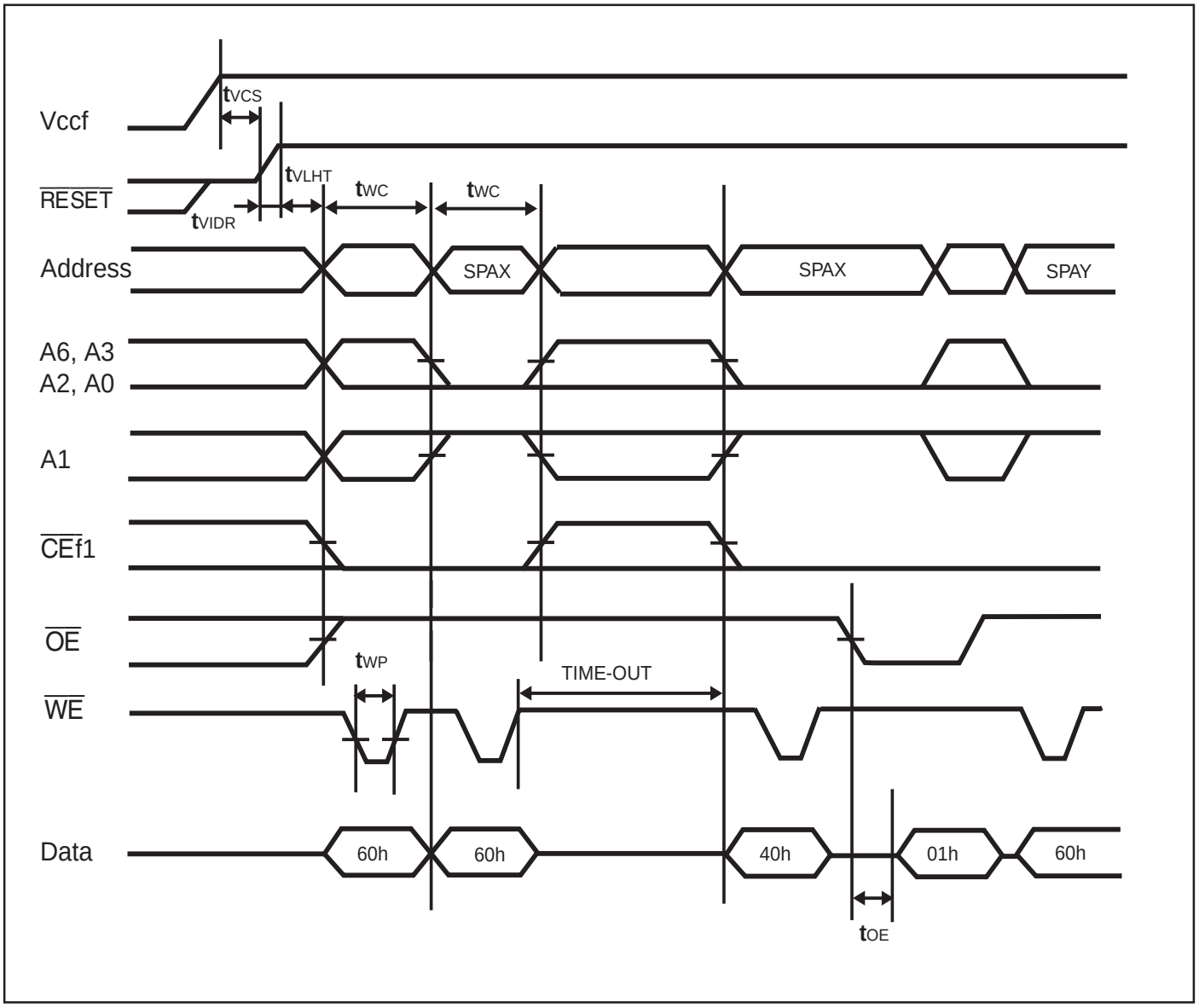
FLASH TEMPORARY SECTOR GROUP UNPROTECTION - FLASH 1 or FLASH 2



FLASH ACCELERATED PROGRAM - FLASH 1 or FLASH 2



FLASH EXTENDED SECTOR GROUP PROTECTION- FLASH 1 or FLASH 2



Notes:

1. SPAX : Sector Group Address to be protected, SPAY : Next Group Sector Address to be protected, TIME-OUT: Time-Out window = 250 µs (Min)

FLASH ERASE AND PROGRAMMING PERFORMANCE - FLASH 1 or FLASH 2

Parameter	Min.	Typ.(1)	Max.	Unit	Remarks
Sector Erase Time	—	0.5	2.0	s	Excludes programming time prior to erasure
Word Programming Time	—	6.0	100	µs	Excludes system-level overhead
Chip Programming Time	—	—	200	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	

Note:

1. Typical Erase conditions TA = 25°C, VCCf_1 & VCCf_2 = 2.9V. Typical Program conditions TA = 25°C, VCCf_1 & VCCf_2 = 2.9V. Data= Checker

PSRAM POWER DOWN PROGRAM KEY TABLE

Basic KEY Table

Definition	A16	A17	A18	A19	A20
KEY	Mode Select		Area Select		

A18	A19	A20	AREA
L	L	L	BOTTOM (3)
L	H	X	RESERVED
H	L	X	RESERVED
H	H	H	TOP (2)

A16	A17	MODE
L	L	NAP (4)
L	H	RESERVED
H	H	8M Partial
H	H	SLEEP (4,5)

Available KEY Table

MODE	A16	A17	A18	A19	A20	Data Retention Area
	Mode Select		Area Select			
NAP	L	L	X	X	X	None
8M Partial	H	L	L	L	L	Bottom 8M Only
	H	L	H	H	H	Top 8M only
SLEEP	H	H	X	X	X	None

Notes:
1: The Power Down Program can be performed one time after compliance of Power-up timings and it should not be re-programmed after regular Read or Write. Unspecified addresses, A0 to A15, can be either High or Low during the programming. The RESERVED key should not be used.
2: TOP area is from the lowest address location. (i.e., A[20:0] = H))
3: BOTTOM area is from the highest address location. (i.e., A[20:0] = L)
4: NAP and SLEEP do not retain the data and Area Select is ignored.
5: Default state. Power Down Program to this SLEEP mode can be omitted.

PSRAM READ OPERATIONS

Parameter	Symbol	Min	Max.	Unit
Read Cycle Time	t_{RC}	70	—	ns
Chip Enable Access Time(1,3)	t_{CE}	—	65	ns
Output Enable Access Time(1)	t_{OE}	—	40	ns
Address Access Time(1,4)	t_{AA}	—	65	ns
Output Data Hold Time(1)	t_{OH}	5	—	ns
$\overline{CE}$1r Low to Output Low-Z(2)	t_{CLZ}	5	—	ns
$\overline{OE}$ Low to Output Low-Z(2)	t_{OLZ}	0	—	ns
$\overline{CE}$1r High to Output High-Z(2)	t_{CHZ}	—	20	ns
$\overline{OE}$ High to Output High-Z(2)	t_{OHZ}	—	20	ns
Address Setup Time to $\overline{CE}$1r Low(5)	t_{ASC}	-5	—	ns
Address Setup Time to $\overline{OE}$(3,6)	t_{ASO}	25	—	ns
Address Setup Time to $\overline{OE}$(7)	$t_{ASO(ABS)}$	10	—	ns
$\overline{LB}$/$\overline{UB}$ Set up Time to $\overline{CE}$1r Low(5)	t_{BSC}	-5	—	ns
$\overline{LB}$/$\overline{UB}$ Set up Time to $\overline{OE}$ Low	t_{BSO}	-10	—	ns
Address Invalid Time(4)	t_{AX}	—	5	ns
Address Hold Time from $\overline{CE}$1r Low(4)	t_{CLAH}	70	—	ns
Address Hold Time from $\overline{OE}$ Low(4,8)	t_{OLAH}	45	—	ns
Address Hold Time from $\overline{CE}$1r High	t_{CHAH}	-5	—	ns
Address Hold Time from $\overline{OE}$ High	t_{OHAH}	-5	—	ns
$\overline{LB}$/$\overline{UB}$ Hold Time to $\overline{CE}$1r Low	t_{CHBH}	-5	—	ns
$\overline{LB}$/$\overline{UB}$ Hold Time to $\overline{OE}$ Low	t_{OHBH}	-5	—	ns
$\overline{CE}$1r Low to $\overline{OE}$ Low Delay Time(3,6,8,9)	t_{CLOL}	25	1000	ns
$\overline{OE}$ Low to $\overline{CE}$1r High Delay Time(8)	t_{OLCH}	45	—	ns
$\overline{CE}$1r High Pulse Width	t_{CP}	12	—	ns
$\overline{OE}$ High Pulse Width(6,8,9)	t_{OP}	25	1000	ns
$\overline{OE}$ High Pulse Width(7)	$t_{OP(ABS)}$	12	—	ns

Notes:

1. The output load is 30 pF.
2. The output load is 5 pF.
3. The t_{CE} is applicable if $\overline{OE}$ is brought to Low before $\overline{CE}$1r goes Low and is also applicable if actual value of both or either t_{ASO} or t_{CLOL} is shorter than specified value.
4. Applicable only to A0 and A1 when both $\overline{CE}$1r and $\overline{OE}$ are kept at Low for the address access.
5. Applicable if $\overline{OE}$ is brought to Low before $\overline{CE}$1r goes Low.
6. The t_{ASO}, t_{CLOL} (Min) and t_{OP} (Min) are reference values when the access time is determined by t_{OE}.
   If the actual value of each parameter is shorter than the specified minimum value, t_{OE} becomes longer by the amount of subtracting actual value from specified minimum value.
   For example, if actual t_{ASO}, t_{ASO} (actual) , is shorter than specified minimum value, t_{ASO} (Min) , during $\overline{OE}$ control access (i.e., $\overline{CE}$1r stays Low) , the t_{OE} becomes t_{OE} (Max) + t_{ASO} (Min) - t_{ASO} (actual) .
7. The $t_{ASO[ABS]}$ and $t_{OP[ABS]}$ are the absolute minimum values during $\overline{OE}$ control access.
8. If actual value of either t_{CLOL} or t_{OP} is shorter than specified minimum value, both t_{OLAH} and t_{OLCH} become t_{RC} (Min) - t_{CLOL} (actual) or t_{RC} (Min) - t_{OP} (actual) .
9. Maximum value is applicable if $\overline{CE}$1r is kept at Low.

PSRAM WRITE OPERATIONS

Parameter	Symbol	Value Min.	Max.	Unit
Write Cycle Time(1)	t_{WC}	70	—	ns
Address Setup Time(2)	t_{AS}	0	—	ns
Address Hold Time(2)	t_{AH}	35	—	ns
$\overline{CE}$1r Write Setup Time	t_{CS}	0	1000	ns
$\overline{CE}$1r Write Hold Time	t_{CH}	0	1000	ns
$\overline{WE}$ Setup Time	t_{WS}	0	—	ns
$\overline{WE}$ Hold Time	t_{WH}	0	—	ns
$\overline{LB}$ adnd $\overline{UB}$ Setup Time	t_{BS}	-5	—	ns
$\overline{LB}$ adnd $\overline{UB}$ Hold Time	t_{BH}	-5	—	ns
$\overline{OE}$ Setup Time(3)	t_{OES}	0	1000	ns
$\overline{OE}$ Hold Time(3,4)	t_{OEH}	25	1000	ns
$\overline{OE}$ Hold Time(5)	$t_{OEH(ABS)}$	12	—	ns
$\overline{OE}$ High to $\overline{CE}$1r Low Setup Time(6)	t_{OHCL}	-5	—	ns
$\overline{OE}$ High to Address Hold Time(7)	t_{OHAH}	-5	—	ns
$\overline{CE}$1r Write Pulse Width(1,8)	t_{CW}	45	—	ns
$\overline{WE}$ Write Pulse Width(1,8)	t_{WP}	45	—	ns
$\overline{CE}$1r Write Recovery Time(1,9)	t_{WRC}	10	—	ns
$\overline{WE}$ Write Recovery Time(1,3,9)	t_{WR}	10	1000	ns
Data Setup Time	t_{DS}	15	—	ns
Data Hold Time	t_{DH}	0	—	ns
$\overline{CE}$1r High Pulse Width(9)	t_{CP}	12	—	ns

Notes:

1. Minimum value must be equal or greater than the sum of actual t_{CW} (or t_{WP}) and t_{WRC} (or t_{WR}).
2. New write address is valid from either $\overline{CE}$1r or $\overline{WE}$ that is brought to High.
3. Maximum value is applicable if $\overline{CE}$1r is kept at Low and both $\overline{WE}$ and $\overline{OE}$ are kept at High.
4. The t_{OEH} is specified from end of t_{WC} (Min), and is a reference value when access time is determined by t_{OE}.
If actual value is shorter than specified minimum value, tOE becomes longer by the amount of subtracting actual value from specified minimum value.
5. The $t_{OEH[ABS]}$ is the absolute minimum value if write cycle is terminated by $\overline{WE}$ and $\overline{CE}$1r stay Low.
6. t_{OHCL} (Min) must be satisfied if read operation is not performed prior to write operation.
In case $\overline{OE}$ is disabled after t_{OHCL} (Min), $\overline{WE}$ Low must be asserted after t_{RC} (Min) from $\overline{CE}$1r Low.
In other words, read operation is initiated if t_{OHCL} (Min) is not satisfied.
7. Applicable if $\overline{CE}$1r stays Low after read operation.
8. t_{CW} and t_{WP} are applicable if write operation is initiated by $\overline{CE}$1r and $\overline{WE}$, respectively.
9. t_{WRC} and t_{WR} are applicable if write operation is terminated by $\overline{CE}$1r and $\overline{WE}$, respectively.
The t_{WR} (Min) can be ignored if $\overline{CE}$1r is brought to High together or after $\overline{WE}$ is brought to High.
In such a case, the t_{CP} (Min) must be satisfied.

PSRAM POWER DOWN PARAMETERS

Parameter	Symbol	Value Min.	Value Max.	Unit
CE2r Low Setup Time for Power down Entry	t_{CSP}	10	—	ns
CE2r Low Hold Time after Power down Entry	t_{C2LP}	70	—	ns
$\overline{CE}$1r High Hold Time Following CE2r High after Power down Exit SLEEP Mode only	t_{CHH}	350	—	µs
$\overline{CE}$1r High Setup Time following CE2r High after Power down Exit (Except for SLEEP Mode)	t_{CHHN}	1	—	µs
$\overline{CE}$1r High Setup Time following CE2r High after Power down Exit	t_{CHS}	10	—	ns
$\overline{CE}$1r High to $\overline{PE}$ Low Setup Time (1)	t_{EPS}	70	—	ns
$\overline{PE}$ Power Down Program Pulse Width (1)	t_{EP}	70	—	ns
$\overline{PE}$ High to $\overline{CE}$1r Low Hold Time (1)	t_{EPH}	70	—	ns
Address Setup Time to $\overline{PE}$ High (1)	t_{EAS}	15	—	ns
Address Setup Time from $\overline{PE}$ High (1)	t_{EAH}	0	—	ns

Note:
1. Applies to Power Down Program.

PSRAM OTHER TIMING PARAMETERS

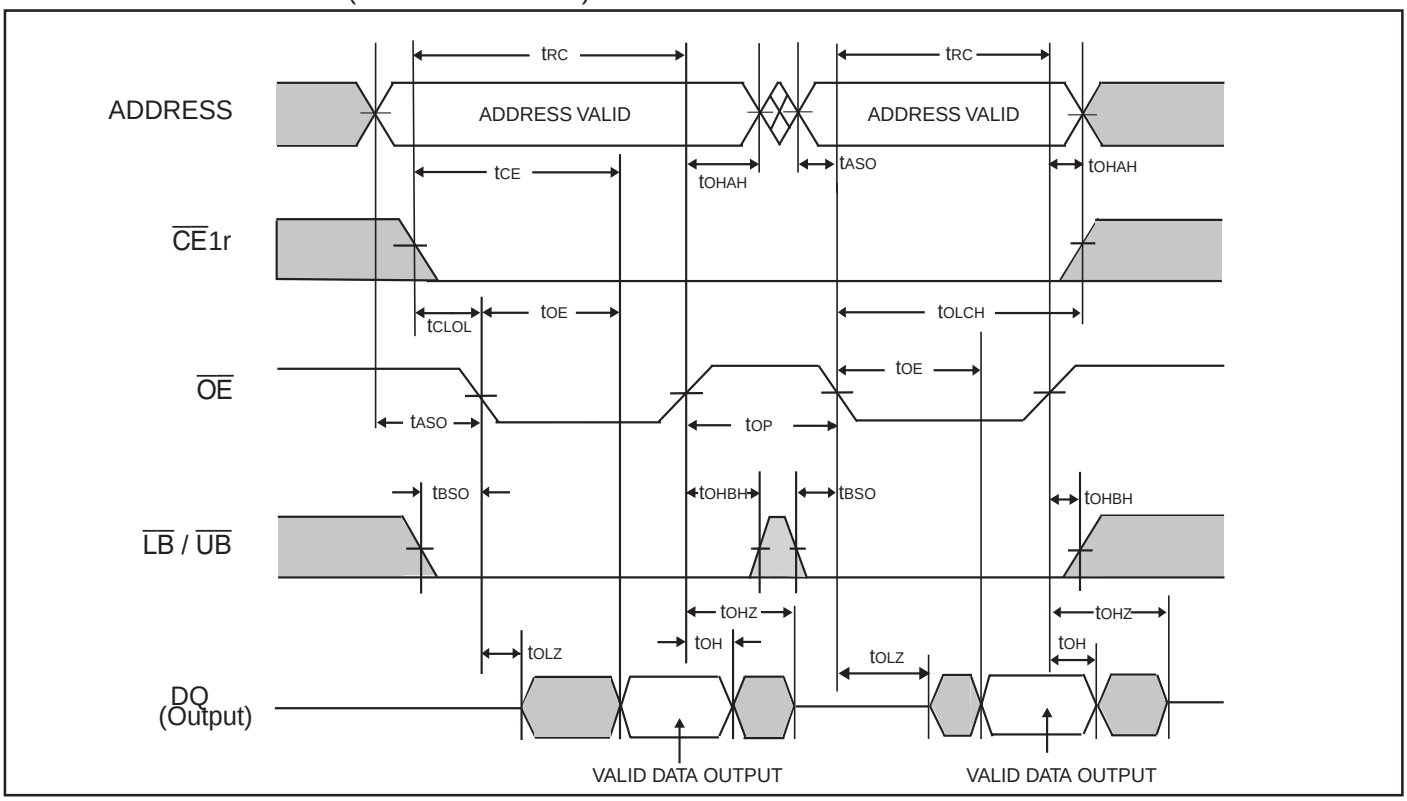
Parameter	Symbol	Value Min.	Value Max.	Unit
$\overline{CE}$1r High to $\overline{OE}$ Invalid for Standby Entry	t_{CHOX}	10	—	ns
$\overline{CE}$1r High to $\overline{WE}$ Invalid for Standby Entry(1)	t_{CHWX}	10	—	ns
CE2r Low Hold Time after Power-up(2)	t_{C2LH}	50	—	µs
CE2r High Hold Time after Power-up(3)	t_{C2HL}	50	—	µs
$\overline{CE}$1r High Hold Time Following CE2r High after Power-up(2)	t_{CHH}	350	—	µs
Input Transition Time(4)	t_T	1	25	ns

Notes:
1. Unintended data may be written into any address location if t_{CHWX} is not satisfied.
2. Must satisfy t_{CHH} (Min) after t_{C2LH} (Min) .
3. Requires Power Down mode entry and exit after t_{C2HL}.
4. Input Transition Time (t_T) at AC testing is 5 ns as shown below. If actual t_T is longer than 5 ns, it may violate some timing parameters.

PSRAM AC TEST CONDITIONS

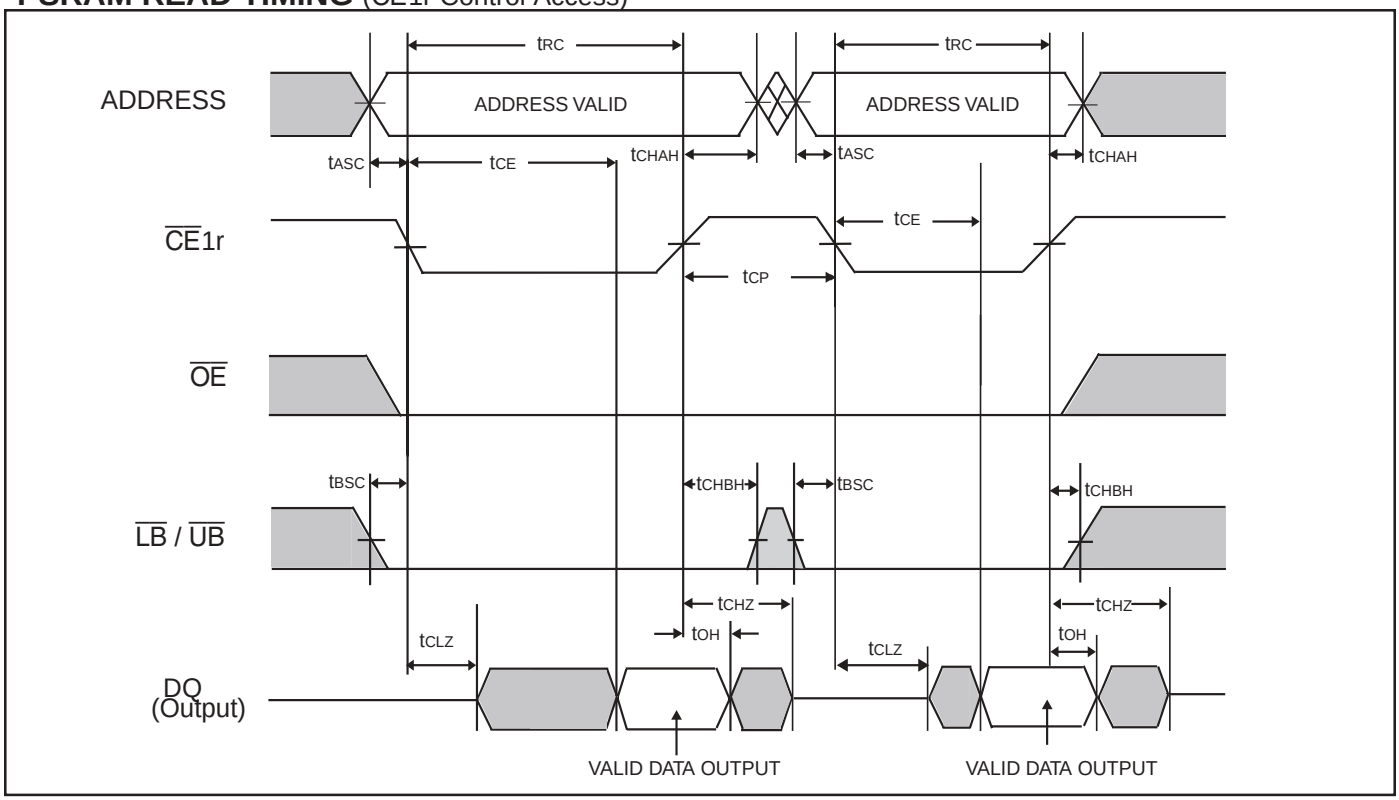
Parameter	Symbol	Condition	Value	Unit
Input High Level	V_{IH}	V_{CCr} = 2.7V to 3.3V	2.3	V
Input Low Level	V_{IL}	V_{CCr} = 2.7V to 3.3V	0.4	V
Input Timing Measurement Level	V_{REF}	V_{CCr} = 2.7V to 3.3V	1.3	V
Input Transition Time	t_T	Between V_{IL} and V_{IH}	5	ns

PSRAM READ TIMING ($\overline{OE}$ Control Access)



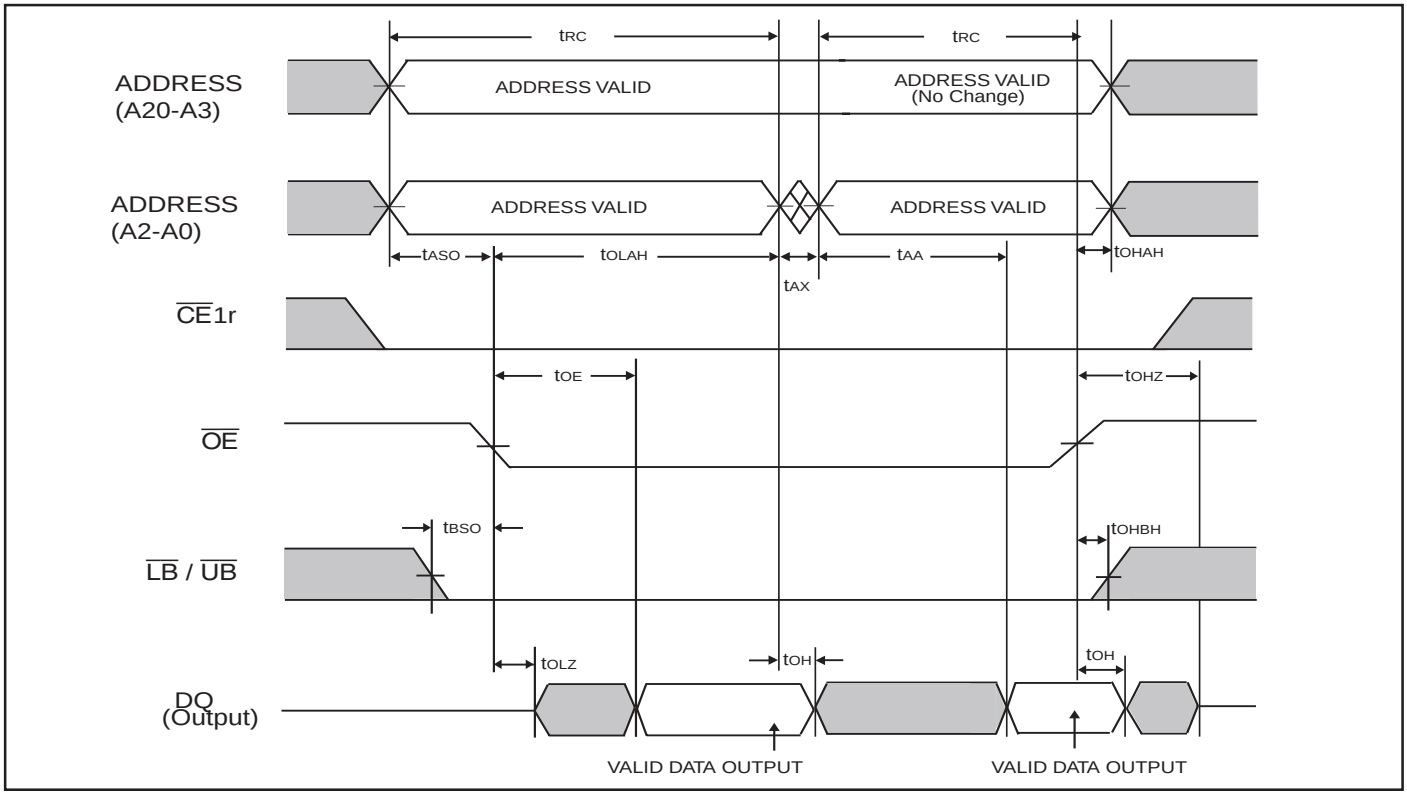
Note: CE2r, $\overline{PE}$ and $\overline{WE}$ must be High during read cycle. Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE}$1r and $\overline{OE}$ are Low.

PSRAM READ TIMING ($\overline{CE}$1r Control Access)



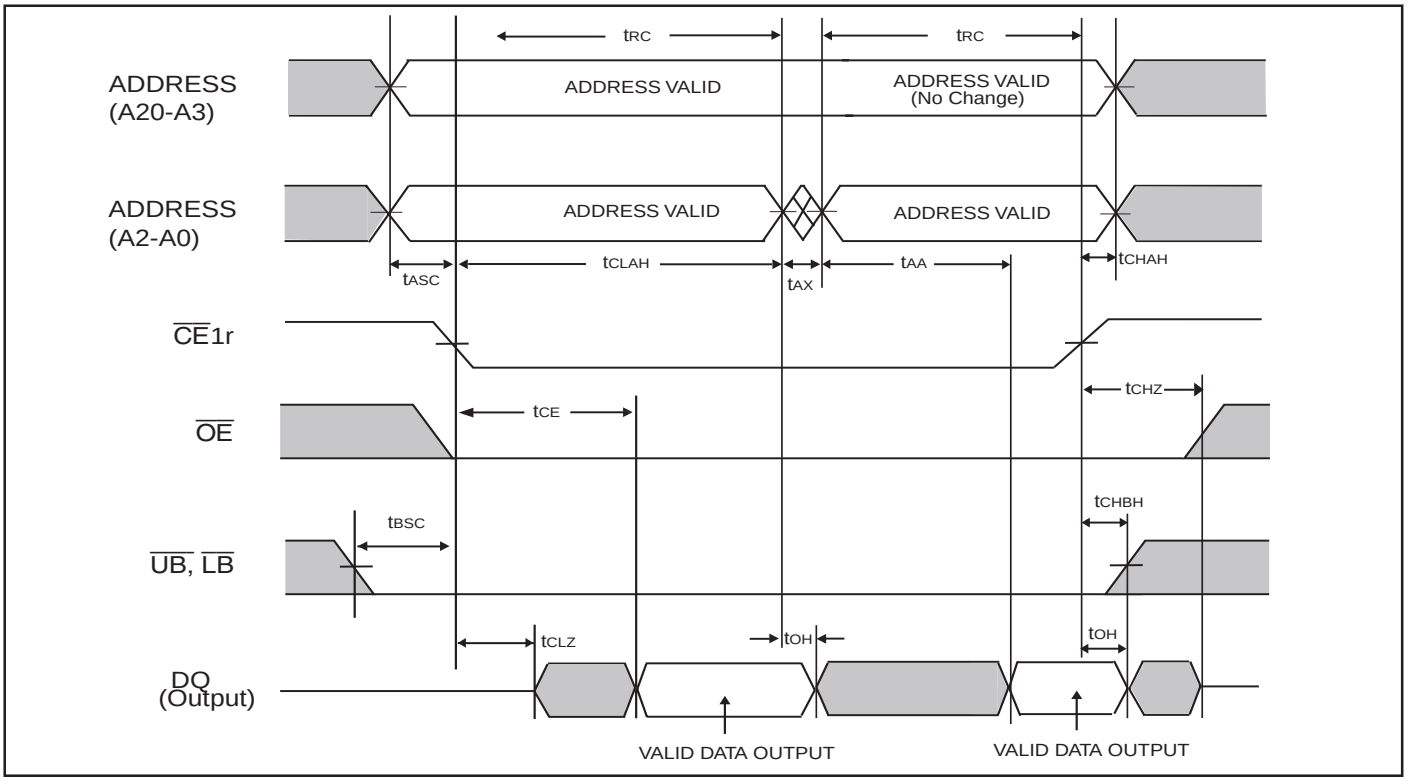
Note: CE2r, $\overline{PE}$ and $\overline{WE}$ must be High during read cycle. Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE}$1r and $\overline{OE}$ are Low.

PSRAM READ TIMING (Address Access after $\overline{OE}$ Control Access)



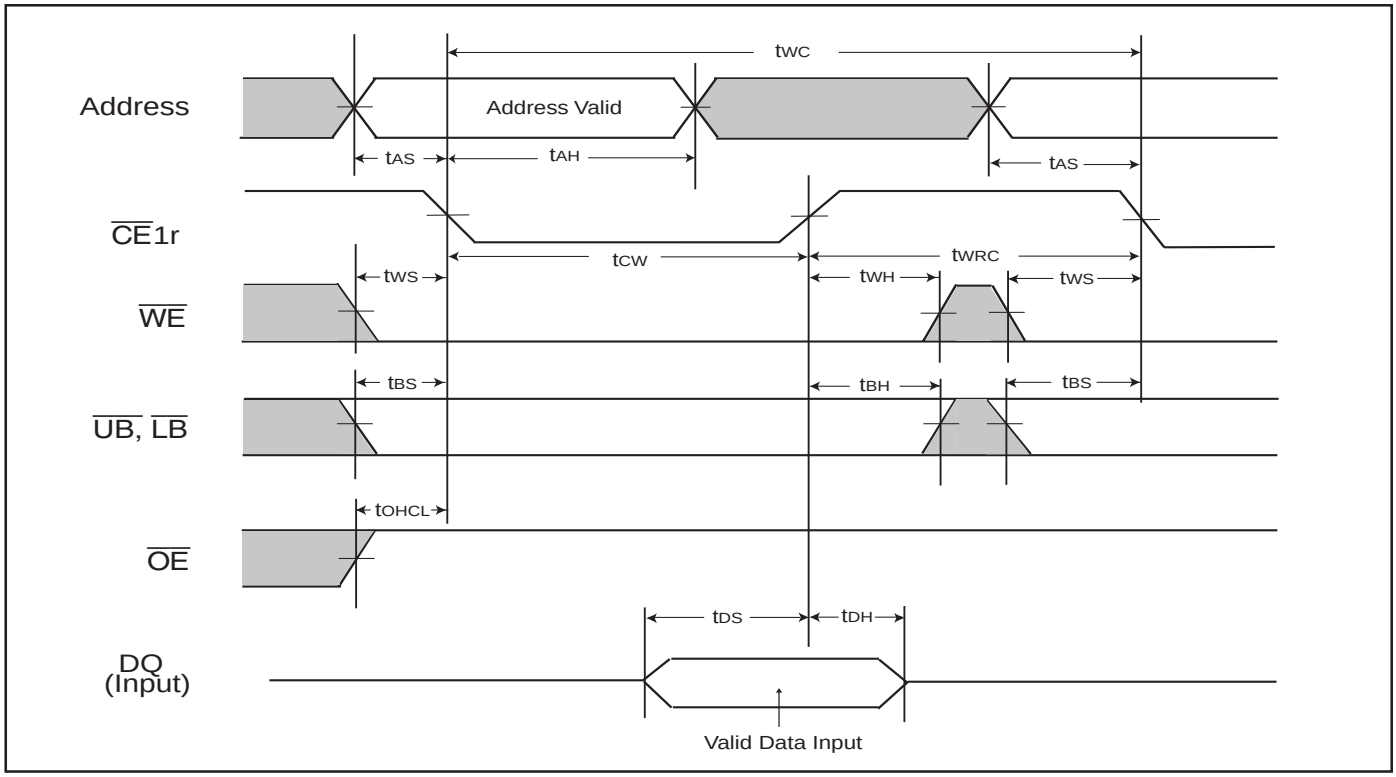
Note: CE2r, $\overline{PE}$ and $\overline{WE}$ must be High during read cycle. Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE}$1r and $\overline{OE}$ are Low.

PSRAM READ TIMING (Address Access after $\overline{CE}$1r Control Access)



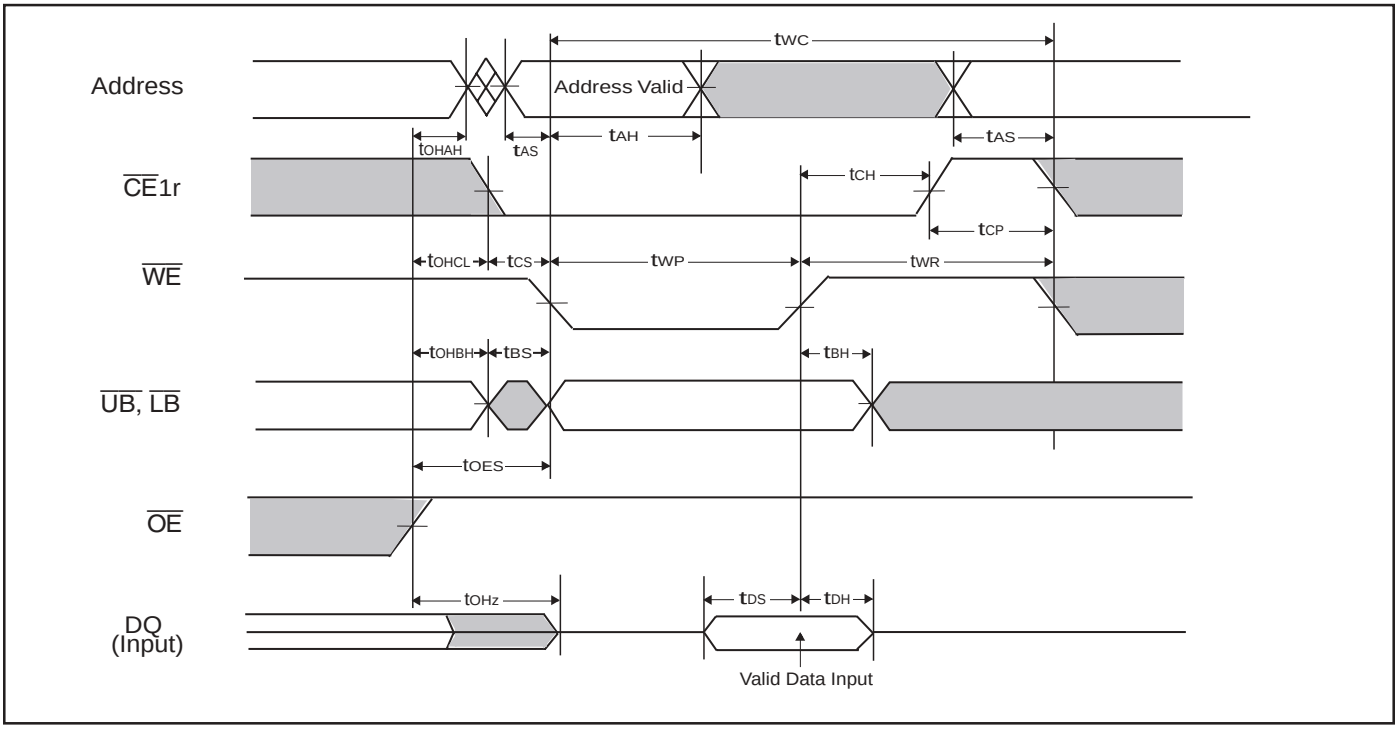
Note: CE2r, $\overline{PE}$ and $\overline{WE}$ must be High during read cycle. Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE}$1r and $\overline{OE}$ are Low.

PSRAM WRITE TIMING ($\overline{CE}$1r Control)



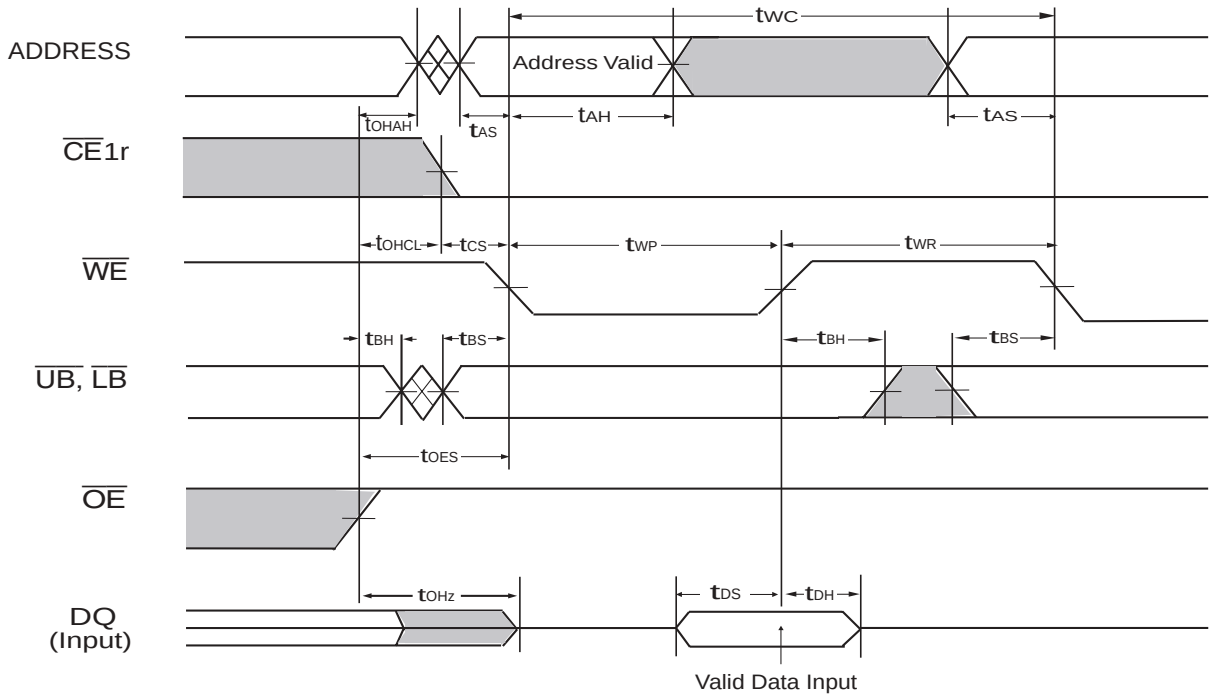
Note: CE2r and $\overline{PE}$ must be High during write cycle.

PSRAM WRITE TIMING ($\overline{WE}$ Control, Single Write Operation)



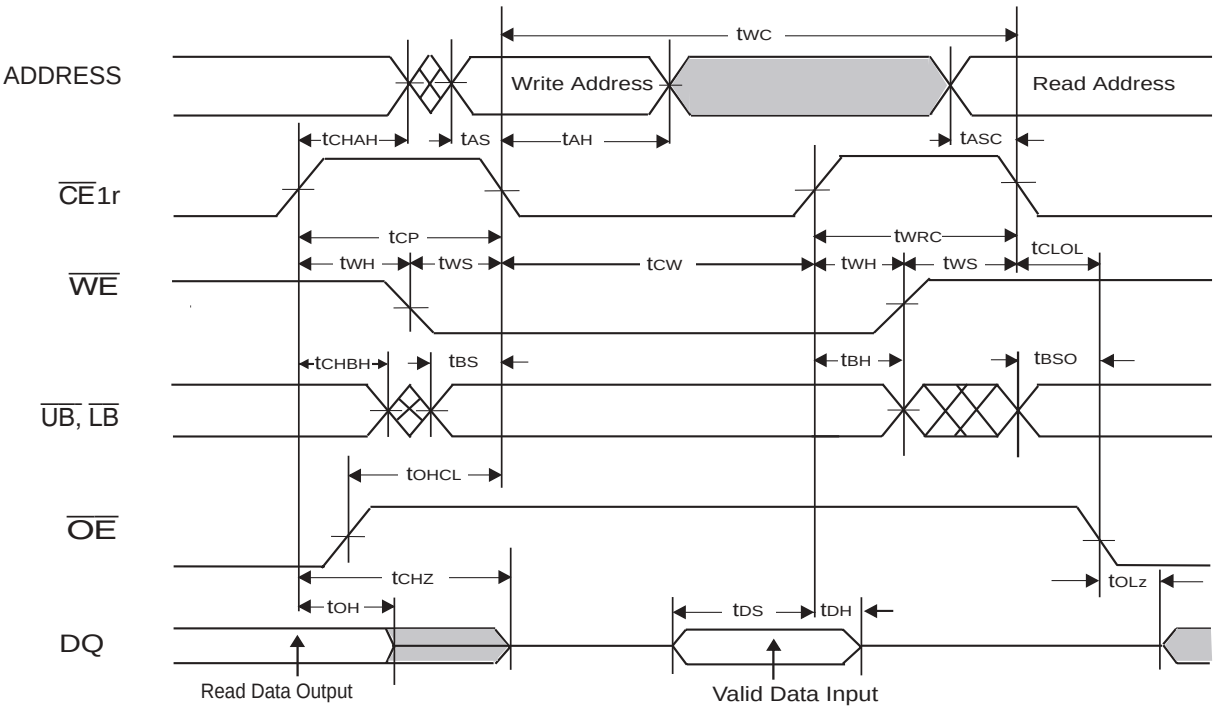
Note: CE2r and $\overline{PE}$ must be High during write cycle.

PSRAM WRITE TIMING ($\overline{WE}$ Control, Continuous Write Operation)



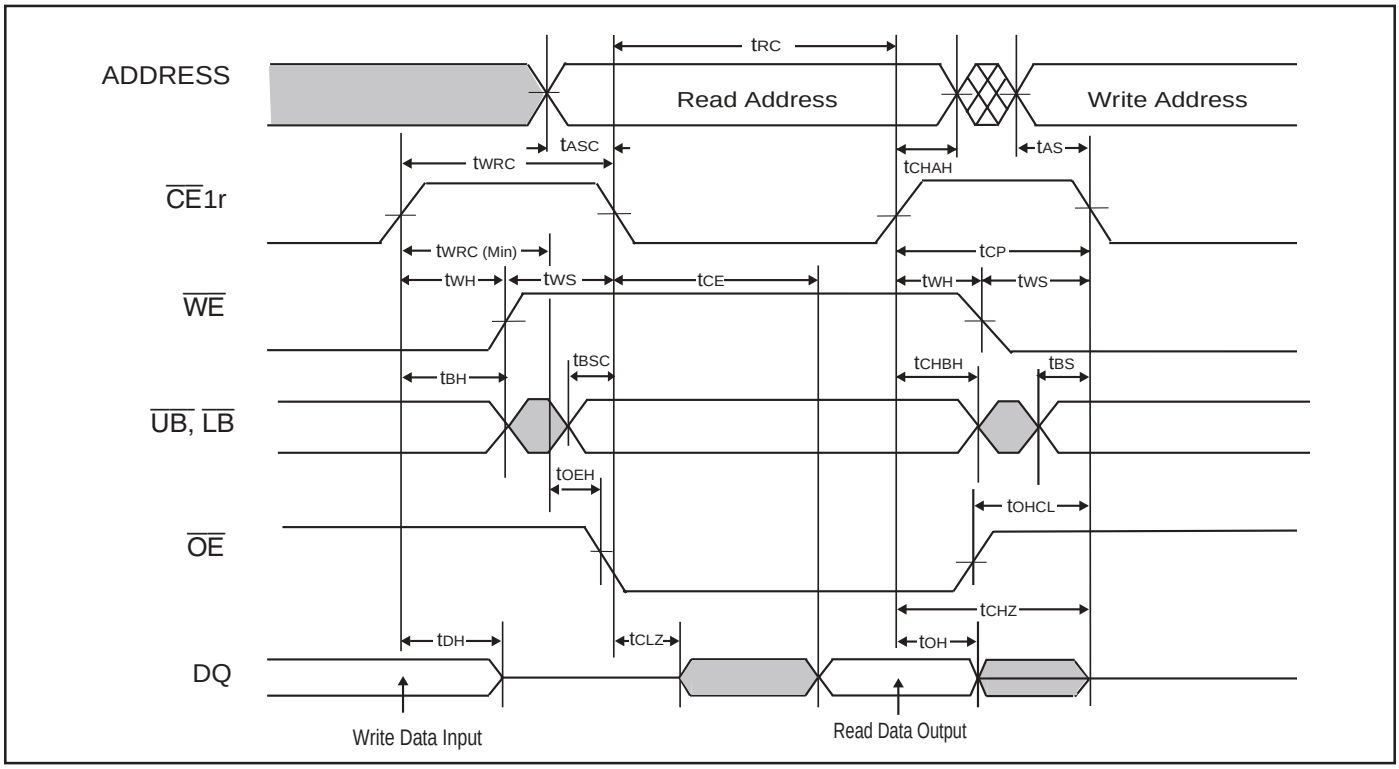
Note: CE2r and $\overline{PE}$ must be High during write cycle.

PSRAM READ / WRITE TIMING ($\overline{CE}$1r Control)



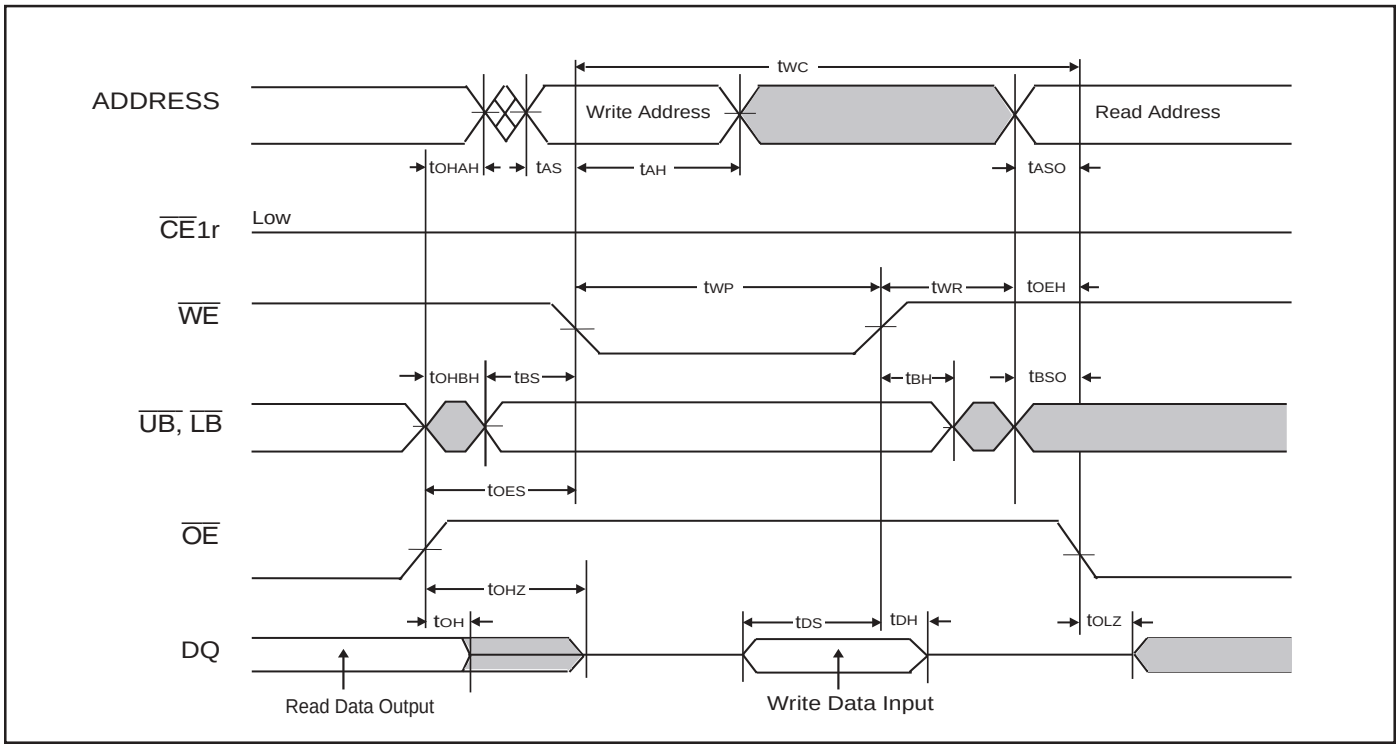
Note: Write address is valid from either $\overline{CE}$1r or $\overline{WE}$ of last falling edge.

PSRAM READ / WRITE TIMING ($\overline{CE}$1r Control)



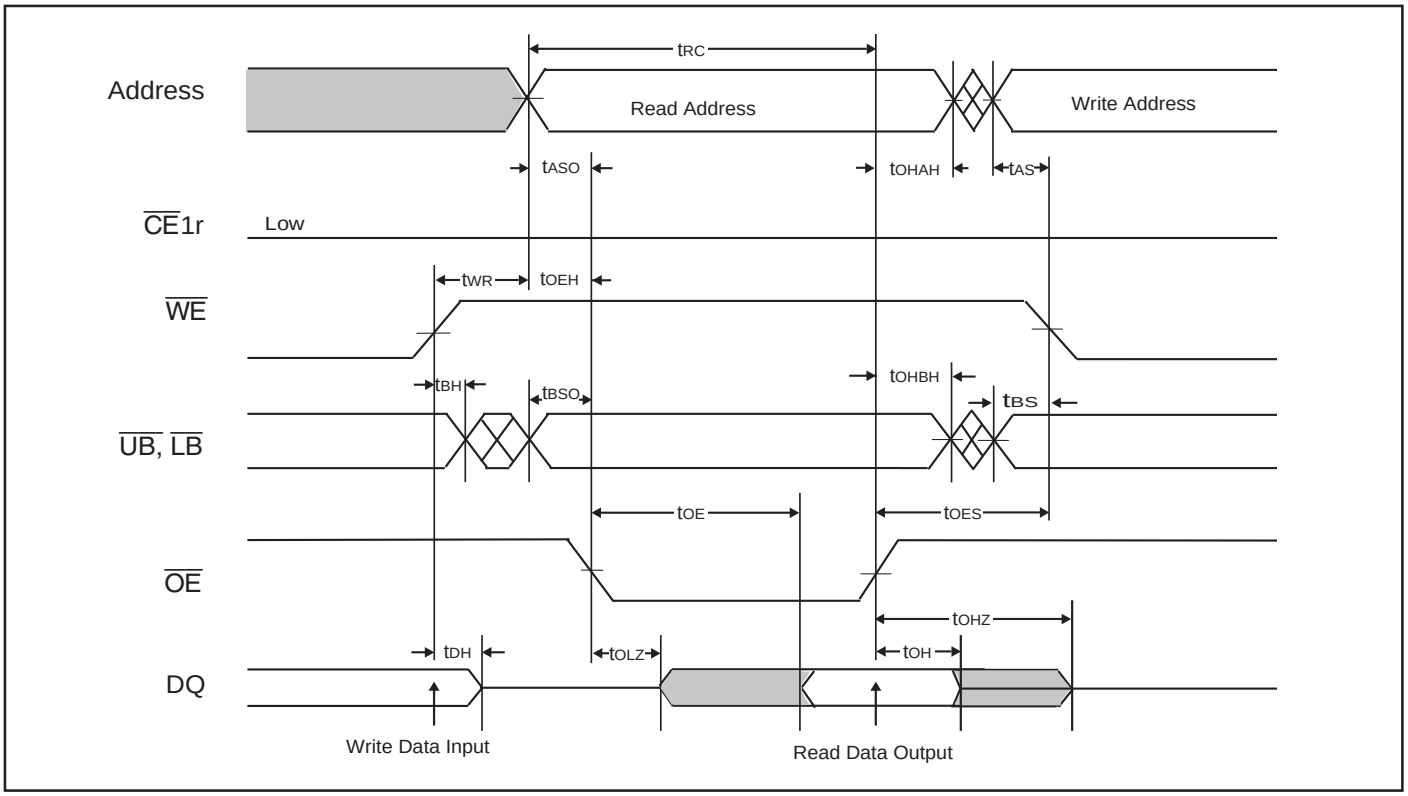
Note: The t_{OEH} is specified from the time satisfied oth t_{WRC} and t_{WR}(min).

PSRAM READ / WRITE TIMING (READ = $\overline{OE}$ Control, WRITE = $\overline{WE}$ Control)



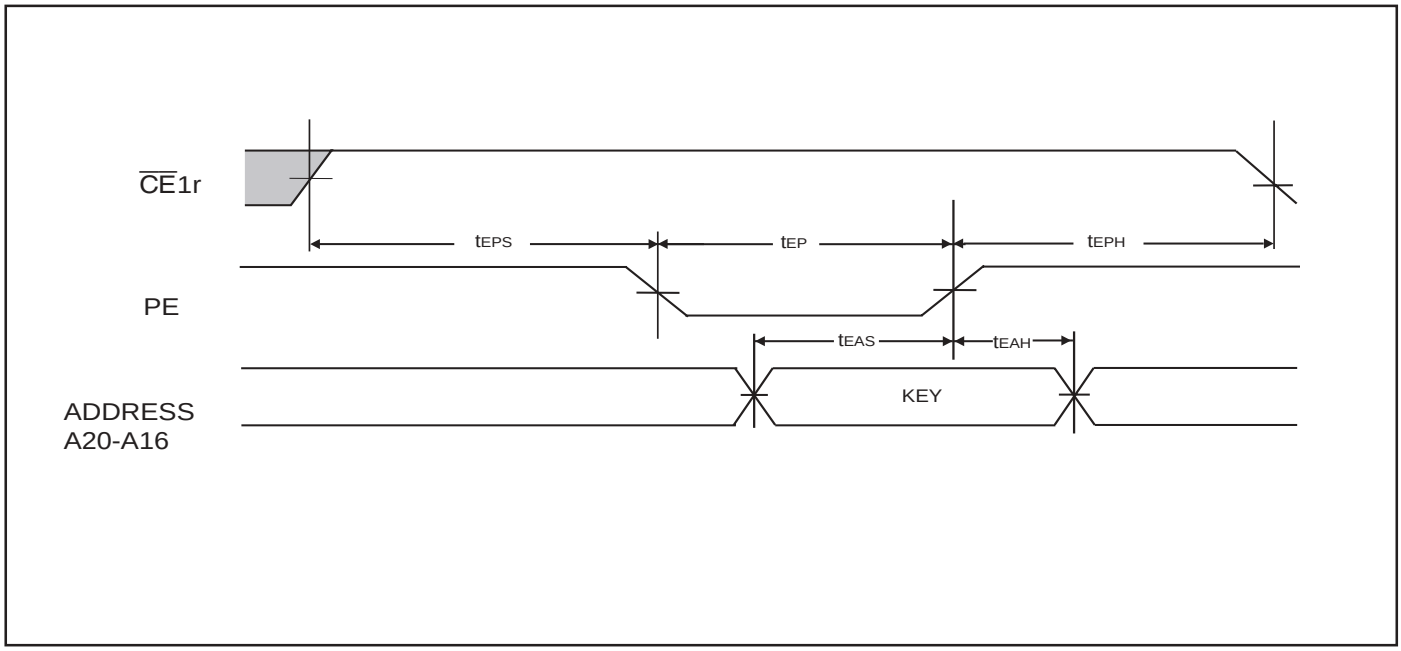
Note: $\overline{CE}$1r can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation. When $\overline{CE}$1r is tied to Low, output is exclusively controlled by $\overline{OE}$.

PSRAM READ / WRITE TIMING (READ = $\overline{OE}$ Control, WRITE = $\overline{WE}$ Control)



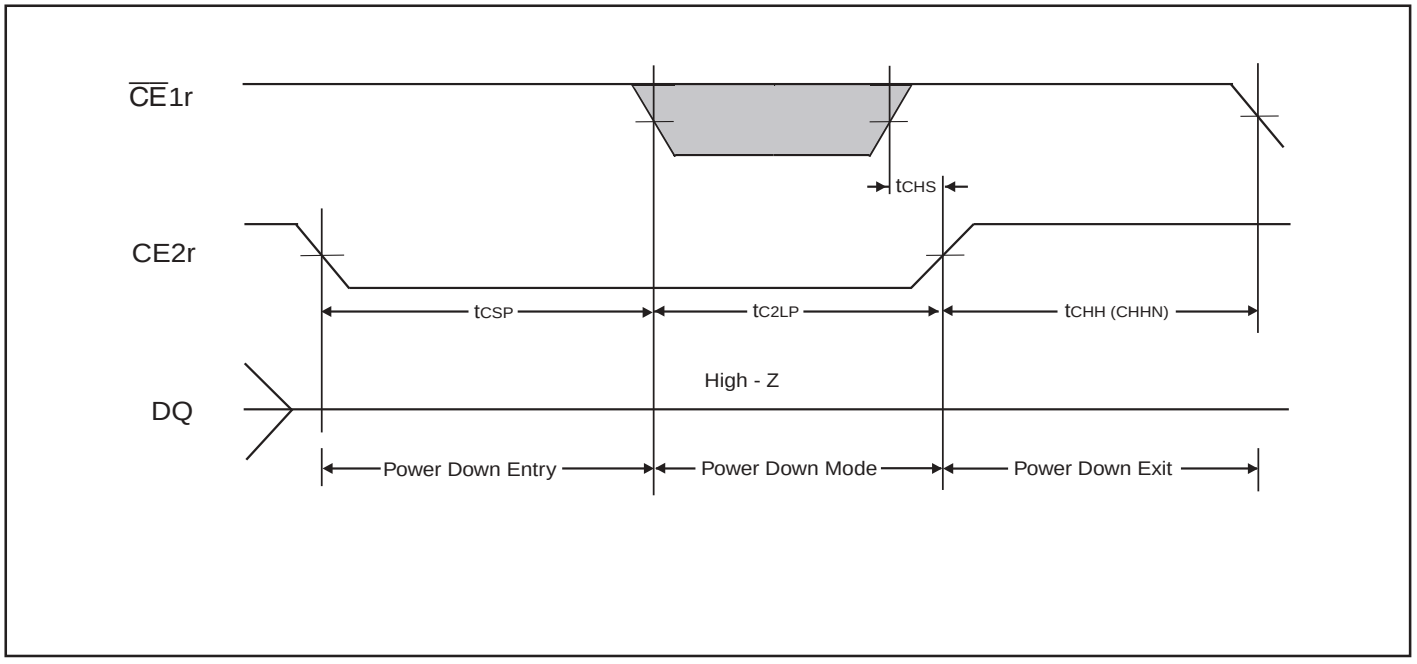
Note: $\overline{CE}$1r can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation. When $\overline{CE}$1r is tied to Low, output is exclusively controlled $\overline{OE}$.

PSRAM POWER DOWN TIMING



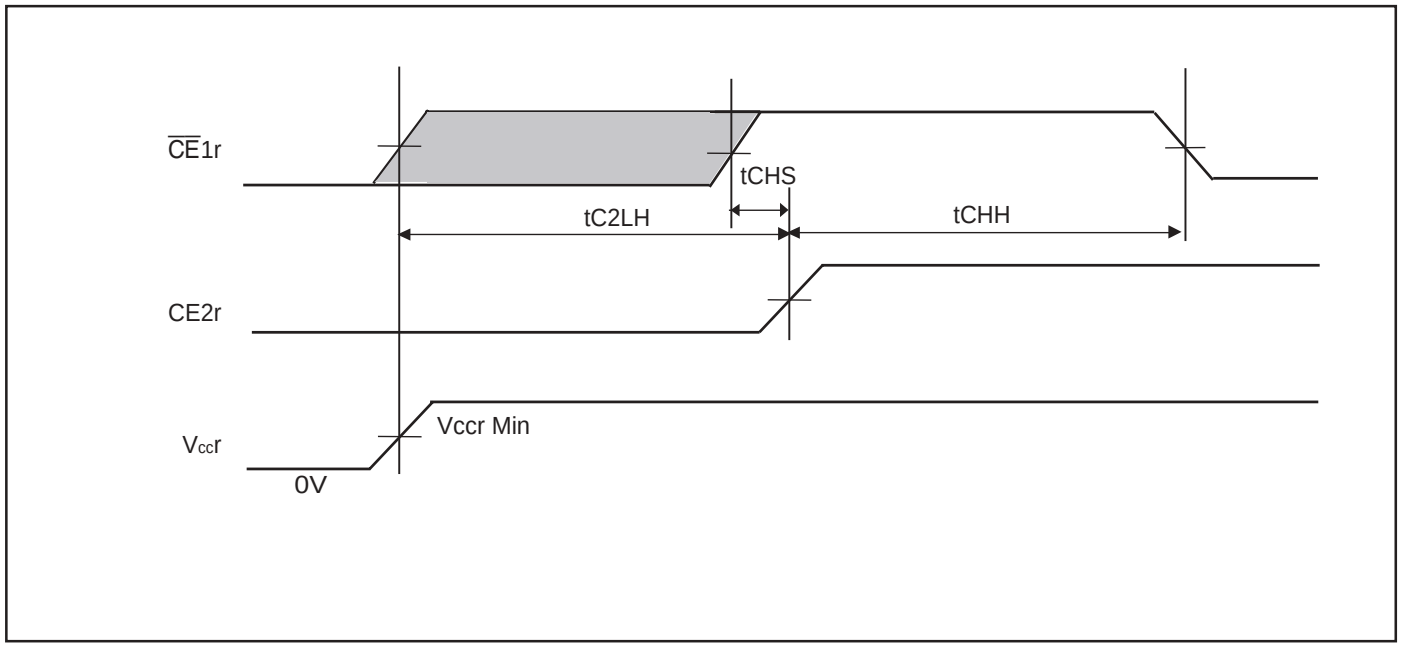
Note: CE2r must be High for Power Down Programming. Any other inputs not specified above can be either High or Low.

PSRAM STANDBY ENTRY and EXIT TIMING



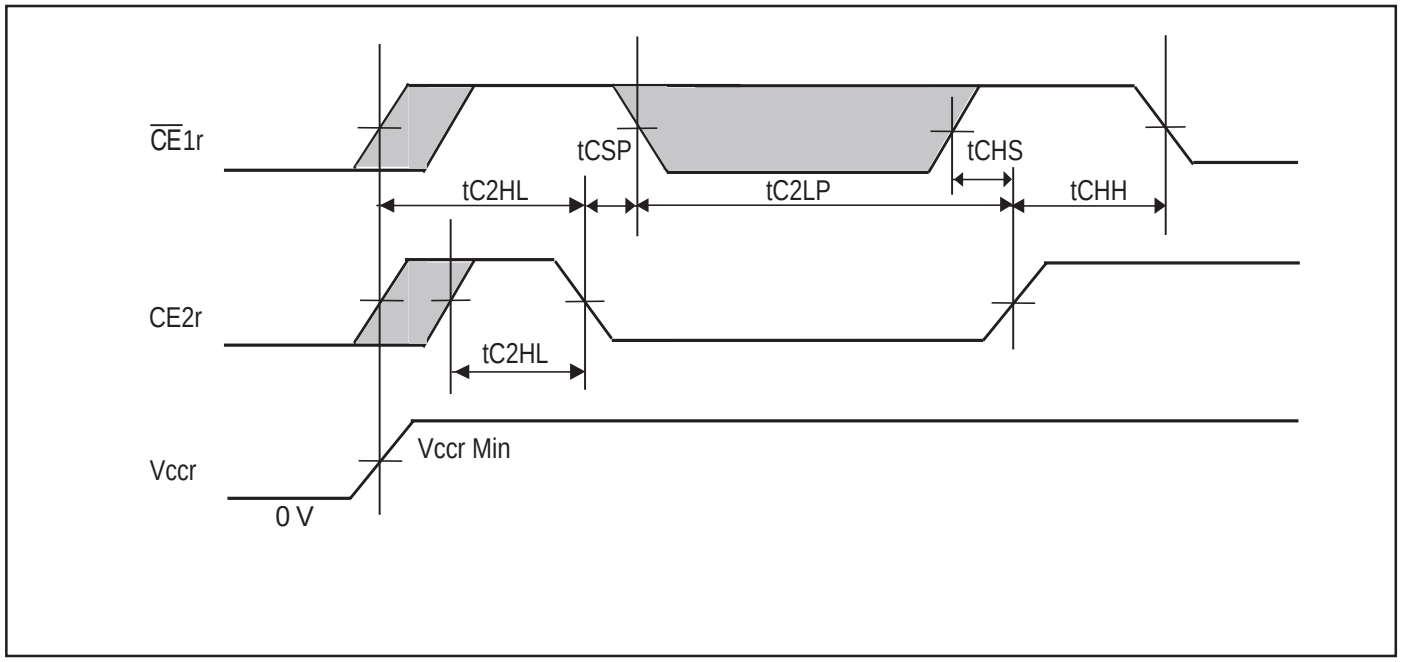
Note: This Power Down mode can be also used for Power-up Timing #2 except that t_{CHHN} can not be used at Power-up Timing.

PSRAM POWER UP TIMING 1



Note: The tC2LH specifies after Vccr reaches specfied minimum level.

PSRAM POWER UP TIMING 2



Note: The tC2HL specifies from CE2r Low to High transition after Vccr reaches specified minimum level. CE1r must be brought to High prior to or together with CE2r Low to High transition.

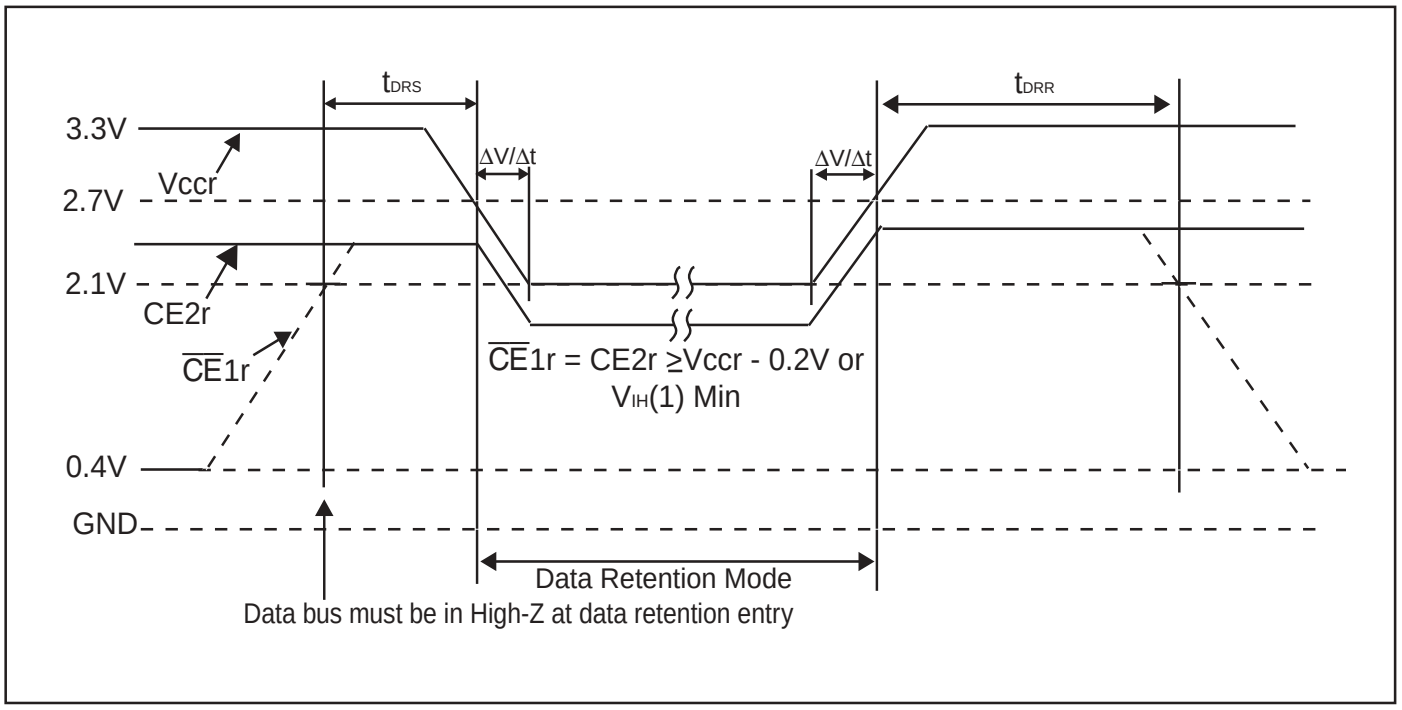
PSRAM DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{DR}	Vccr Data Retention Supply Voltage	$\overline{CE1}r = CE2r \geq V_{CCr} - 0.2V$ OR, $\overline{CE1}r = CE2r = V_{IH}$	2.1	3.3	V
I_{DR}	Vccr Data Retention Supply Current	2.1 V ≤ Vccr ≤ 2.7 V, $V_{IN} = V_{IH}$ (1) or V_{IL}, $\overline{CE1}r = CE2r = V_{IH}$ (1), I_{OUT} = 0 mA	—	1.5	mA
I_{DR1}	Vccr Data Retention Supply Current	2.1 V ≤Vccr ≤ 2.7 V, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CCr} - 0.2$ V, $\overline{CE1}r = CE2r \geq V_{CCr} - 0.2$ V, I_{OUT} = 0 mA	—	100	µA
t_{DRS}	Data Retention SetupTime	2.7 V ≤ Vccr ≤ 3.3 V, At Data Retention Entry	0	—	ns
t_{DRR}	Data Retention RecoveryTime	2.7 V ≤ Vccr ≤ 3.3 V, After Data Retention	200	—	ns
ΔV/Δt	V_{CCR} Voltage Transition Time	—	0.2	—	V/µs

Note:

1. 2.0 V ≤ V_{IN} ≤ V_{CCr} + 0.3

PSRAM DATA RETENTION TIMING



Note:

1. 2.0 V ≤ V_{IH} ≤ V_{CCr} + 0.3 V

PIN CAPACITANCE

Symbol	Parameter	Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	-	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	-	25	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0 V	-	25	pF

Notes:

1. Test conditions T_A = +25 °C, f = 1.0 MHz

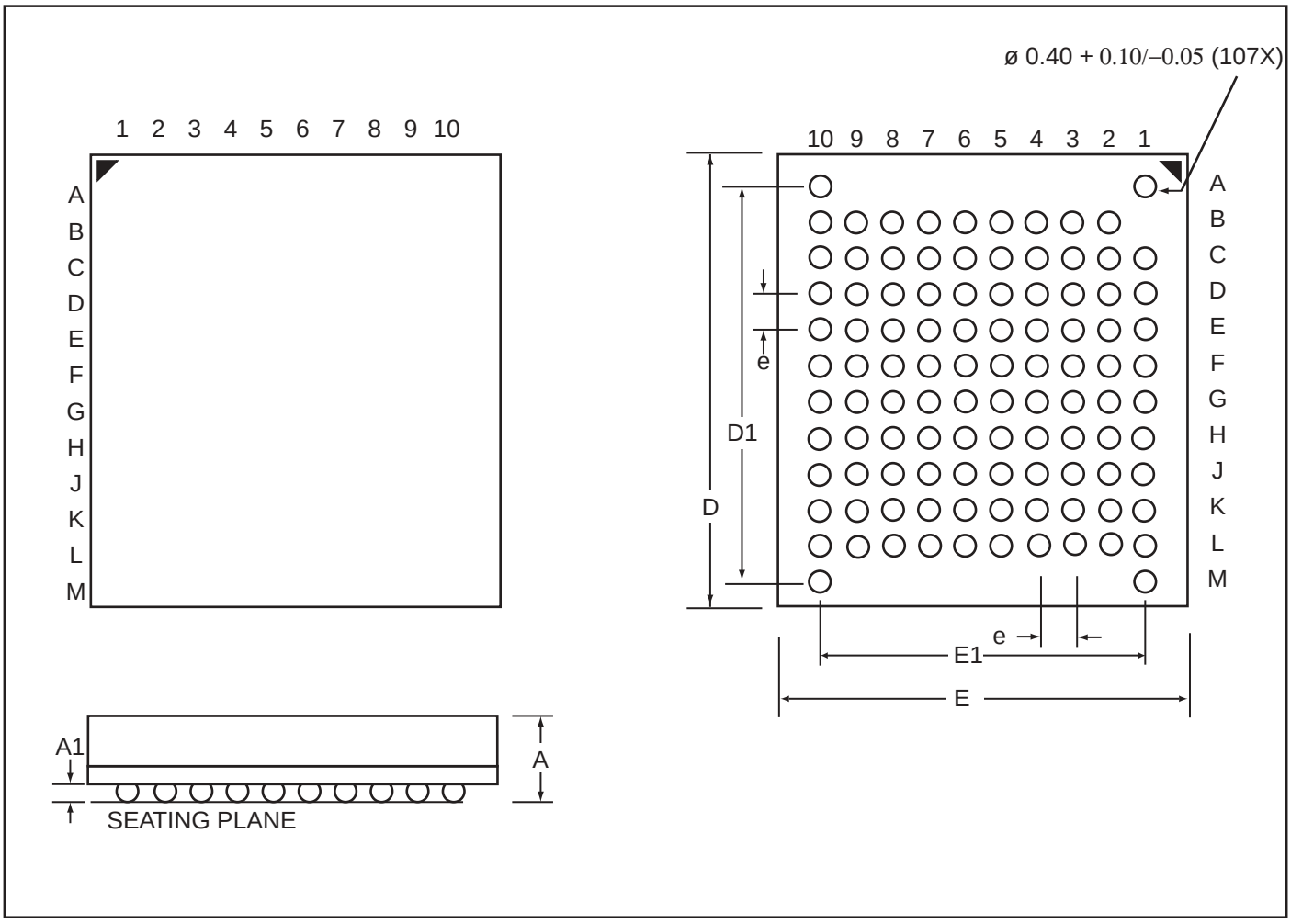
HANDLING OF PACKAGE:

Please handle this package carefully because the sides of the package have acute angles.

CAUTION:

1) The high voltage (VID) cannot be applied to address pins and control pins except RESET. Exception is when autoselect and sector group protection function are used. Then the high voltage (VID) can be applied to RESET.
2) Without the high voltage (VID) sector group protection can be achieved by using the “Extended Sector Group Protection” command.

MINI BALL GRID ARRAY – 107-Ball BGA
PACKAGE CODE: B (9.00 mm x 10.00 mm Body, 0.8 mm Ball Pitch)



Symbol	Min.	Typ.	Max.	Units
A	1.15	1.25	1.40	mm
A1	0.05	0.10	0.15	mm
D	9.90	10.00	10.10	mm
D1	—	8.80	—	mm
E	8.90	9.00	9.10	mm
E1	—	7.20	—	mm
e	—	0.80	—	mm

ORDERING INFORMATION

Industrial Range: -30°C to +85°C

Order Part No.	Flash Bank Organization	Flash Speed(ns)	PSRAM Speed(ns)	Package
IS75V16F128GS32-7065BI	User Configurable	70	65	107-ball BGA