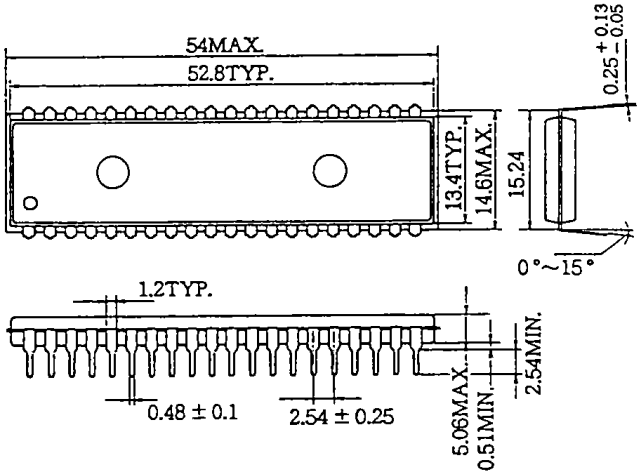
LSI designed specifically to offer a standardized interface bus meeting the
ing equipment interface on a single chip. The SM8530B executes 3-line
mands and bus line commands without software support. Standardized
ing with the IEC standard can be realized easily by adding several external
er/receiver.
pplicable to the IEEE-488, HP-IB and GP-IB.

require a microprocessor, hence:
nt is not necessary.
ng equipment can be used

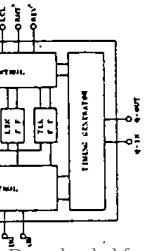
face function can be added easily
ring equipment.
ng to interface states (TLK, LSN,
are provided to facilitate opera-
se speed.
n realized by CMOS construction
h external switches
can be controlled only with the

CLK, etc.) for controlling external
ral circuits.

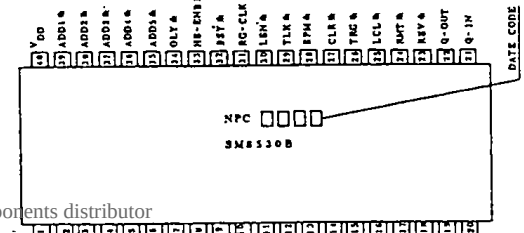
■ PACKAGE DIMENSIONS Unit: mm



40-pin plastic DIP



■ PINOUT TOP VIEW



CHARACTERISTICS

Ta = 25°C

	Symbol	Condition	Min	Typ	Min	Unit
	I_{DD}	V_{DD}=5.25V fosc=4MHz All input pins GND			8.0	mA
	V_{DD}	Q_{in} = 4 MHz or less	4.75	5.0	5.25	V
ns)	V_{IH}	V_{DD}=5.25V	3.0		5.25	V
ns)	V_{IL}	V_{DD}=5.25V	0		0.8	V
	V_{IH} ADD-1	V_{DD}=5.25V	4.9		5.25	V
	V_{IL} ADD-1	V_{DD}=5.25V	0		0.4	V
	V_{IH} Q_{in}	V_{DD}=5.25V	4.0		5.25	V
	V_{IL}•Q_{in}	V_{DD}=5.25V	0		0.8	V
s except Q_{OUT}	V_{OH}	V_{DD}=4.75V, I_{OH}=10μA	2.4		4.75	V
in	V_{OH}•Q_{out}	V_{DD}=4.75V, I_{OH}=10μA	2.4		4.75	V
s except Q_{OUT}	V_{OL}	V_{DD}=5.25V,I_{OL}=3.2mA	0		0.4	V
in	V_{OL}•Q_{out}	V_{DD}=5.25V, I_{OL}=10μA	0		0.4	V

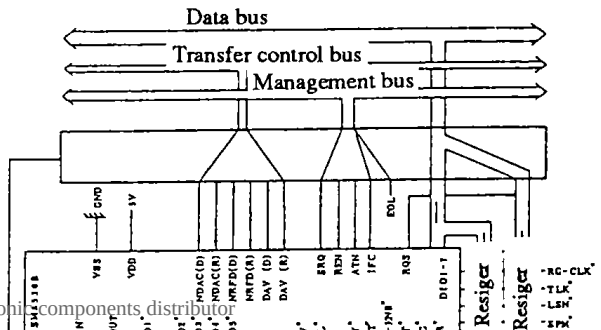
ct the ADD1 pin to V_{DD} or V_{SS} via a 1 KΩ (or less) resistor to set [H][L].
H] to V_{DD} via a 1 MΩ (or more) resistor. To pull up the ADD2 to ADD5
ect them via 2.2 KΩ (or less) resistors for stable operation.

ICTION

cutes the following five

(T)
on (L)
ice request function (SRQ)
RL)
DC, DT)
ts the levels of functions that
the SM8530B in relation to

■ SYSTEM CONFIGURATION



* mark indicates negative logic)

on		No.	Pin name	Function	
		28	SPM*	Pin for outputting signal that indicates system is in serial poll mode. L to Serial poll mode H to Other mode	SPMS
ut pins for data bus s not used.)		29	TLK*	Pin for outputting talker specified signal. L to Specified as talker. H to Not specified as talker.	TADSVTACS
N signal input	ATN	30	LSN*	Pin for outputting listener specified signal. L to Specified as listener. H to Not specified as listener.	LADSVLACS
I signal input	REN				
signal input	IFC				
Q signal output	SRQS	31	RG-CLK*	External register clock signal output. 1 pulse is output when the BSY signal is output.	
	NRFD				
	AIDSVACRS				
	NDAC	32	BSY*	Pin for outputting signal that indicates the execution of 3-line handshaking. L to 3-line handshaking being executed H to Other state Use of this signal is explained later. Data and status must be transmitted/ received while this signal is L.	(i) Transmission (SDYSVSTRS) ∧ TACSVSPAS) (ii) Receiption ACDS ∧ LACS
	AIDSVAWNS				
	DAV				
	STRS				
r status byte)	APRS				
rcuit to idle state.	Pon				
nection pin. in.		33	HS-ENB*	Pin for inputting signal that starts transmission/reception of data and status. Use of this signal is explained later.	(i) Transmis-sion - nba (ii) Receiption, rdy
pin					
quest (i.e., SRQ controller) is		34	OLY*	Input signal for identifying only mode/ address mode of measuring equipment L to Only mode pin 35: L to Talker only H to Listener only H to Address mode	(i) Talker ton (ii) Listener l on
g signal output. equipment to	REMS VRWLS				
equipment to local		35	ADD5*	Pin for specifying address bit 5. Talker/listener is specified in the only mode.	
l that sets back to local state. local lock-out.	rt l	36	ADD4*- ADD2*	Address bits 2 to 4 (See the Address Code Table.)	
nal that starts operation.	DTAS	38	ADD1*	Pin for specifying address bit 1. Connect a 1 MΩ (or more) pull-up resistor for dual address, which validates only the high-order 4 bits of the address converter.	
nal that sets to initial state					
		39	VDD	Ground	

S AND SPECIFIED ■ INTERFACE COMMAND EXECUTED BY THE SM8530B

OF 3-LINE HANDS-
A RECEPTION

DAV and NDAC signals
nd transmission (D) pins,
gic. As all signals have
dard bus line, the logic
me of input to or output

blished (TLK* = L) first.
e
ys set when pins 34 and 35
level.

8 goes H with pin 34
en H, the talker is set by

smitted, a measuring
S-ENB* signal for the
(active) level to control 3-
concept of this operation is
the time chart in Figure 2.
quipment is in the data
tate, make the HS-ENB*
The following condition is
ng.
SY* = H)
the SM8530B senses the
signal. It outputs the
0 ns after NRFD (R) goes
to transmit 1 byte if this
open the gate and output
the register to the bus. The

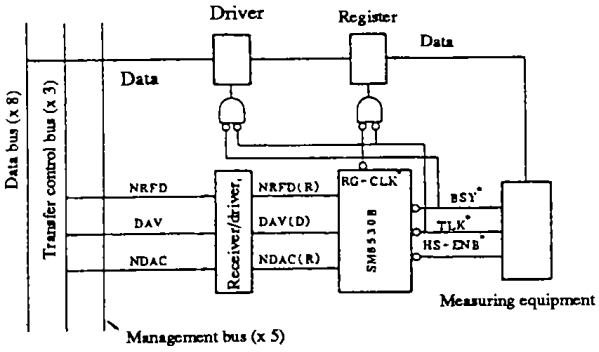
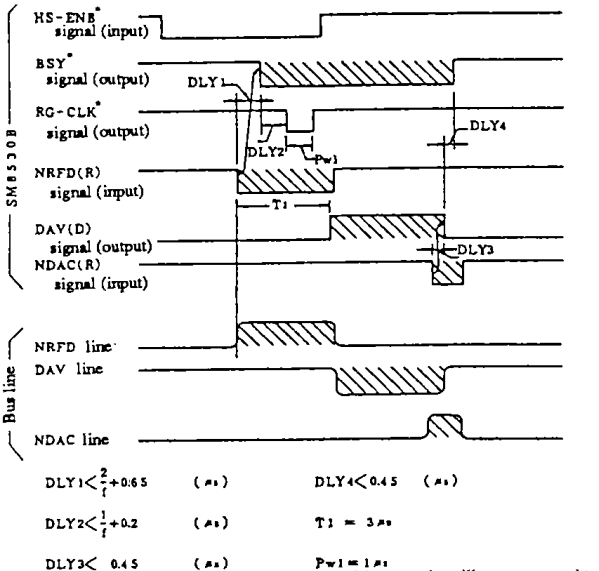


Figure 1 Schematic drawing of a talker



"f" is the oscillation frequency of the crystal oscillator connected to pins 21 and 22 of the SM8530B (example 4 MHz).

Figure 2 Talker handshaking

ss mode)
ollowing five cases:

t
ne listener by MLA
y mode is specified by

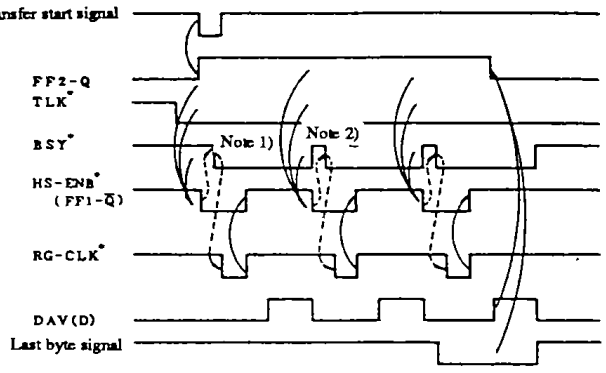
nples of the data trans-
ng. Figures 3 and 4 show
e HS-ENB* signal byte
show an example of
uccession.
ner
olished first (LSN* = L).

ys established when pin
and pin 35 is on the H

e
goes H with pin 34
n H, the listener is set by

nent becomes ready to
0B changes the HS-ENB*
arts 3-line handshaking.
is necessary for this

Y* = H)
natic drawing of data
s timing chart. Refer to
s way of thinking.
oulled H at the end of
owing condition is



→ LSI internal operation
Note 1) In this period, establish DI0 line data. Do not change the data.
Note 2) In this period, change the data to be sent to the DI0 line.
(It is recommended that data be changed at the rising edge of BSY*.)

Figure 4 Timing chart of circuit in Figure 3

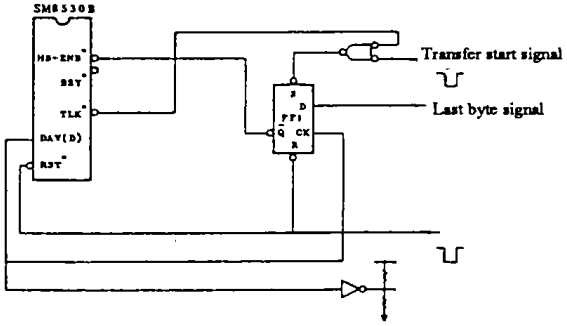
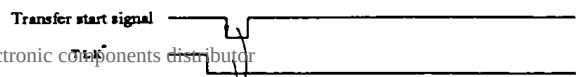


Figure 5 Talker circuit example (II)



received (ATN = H),
uted regardless of the state
nal. The BSY* signal and
l are not output at this
ws the timing chart of this

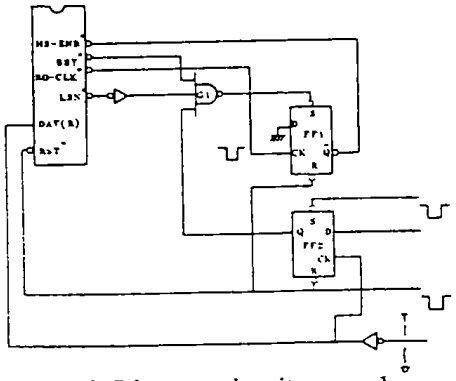
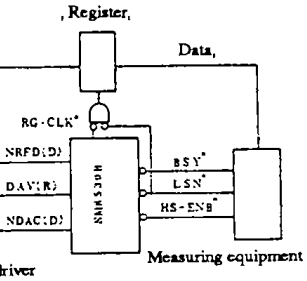
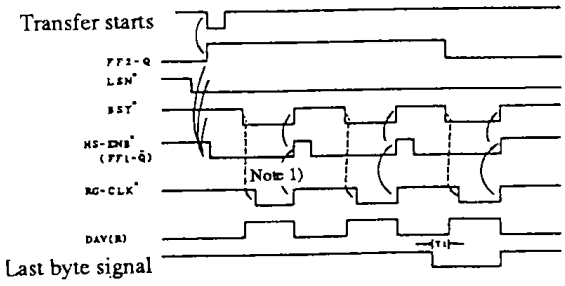


Figure 9 Listener circuit example



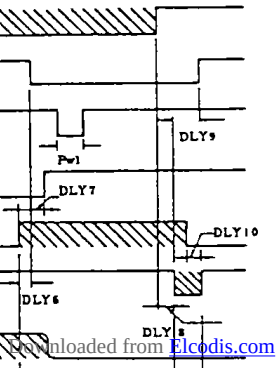
5)

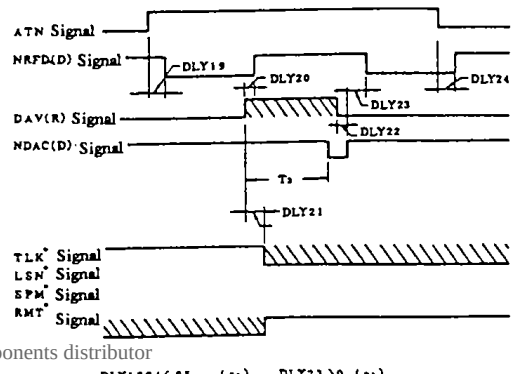
nception



→ LSI internal operation
Note 1) DI0 line data must be stored in the register at the rising edge of RG CLK.

Figure 10 Timing chart of circuit in Fugure 9





VITCHING

zation) after power-on, the SM8530B sets RMT* at pin 24 to the H level
nt to the local state.

receives MLA with REN = H, the RMT* signal goes L to establish the

state
be reset by the following three methods:
sets the local state (in this case, all the equipment in the system is set to the

the listener mode sets the local state.
signal Low with a control switch etc. of a measuring equipment sets the
ning is shown in Figure 12. This method can set a measuring equipment in
pendent of the controller state. This, however, may cause trouble in some
input can be invalidated by the LLO (local lock-out) command input in
ntroller to the SM8530B.
state cannot be reset by the IFC command.
* signal is H (i.e., local state), no limitations are placed on the SM8530B
interface control is performed normally.

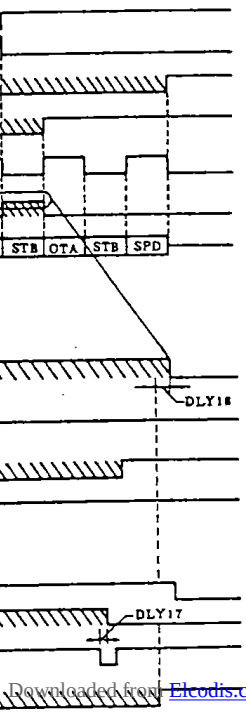
T (interrupt processing)
ends the RSV* signal to the SM8530B to make a service request.
* signal, the SM8530B outputs the H-level SRQ signal to the management
ice request to the controller (logic of the SRQ signal is inverted to L in the

e controller calls the interrupt processing subroutine.
able only to serial-polling systems. Figure 13 shows a service request
e shows an example of the 3-line handshaking timing for status byte (STB)

other measuring equipment in the system
ment in the listener period) to receive the requester's status.
he controller calls the talker by serial polling, a special command (Serial
able) must be sent in advance to distinguish it from the ordinary talker

d listener configurations made with the SM8530B are shown below.
ker for reading A/D converter data, and Figure 16 a listener for controlling

or
roprocessor, the SM8530B can be used to create even more sophisticated
ase, the SM8530B carries out the handshake operation for sending/receiv-
As transmission/reception data can be sent to the microprocessor for
versatile system configurations are possible. Using a microprocessor also
ications to be designed. In this case, the SM8530B performs only the
o the ATN, IFC, REN, SRQ and EOI control signals are processed directly
/OUT commands. In this case, it is effective to use the SM8530B in the
shows the schematic drawing of the former case, and Figure 18 the latter



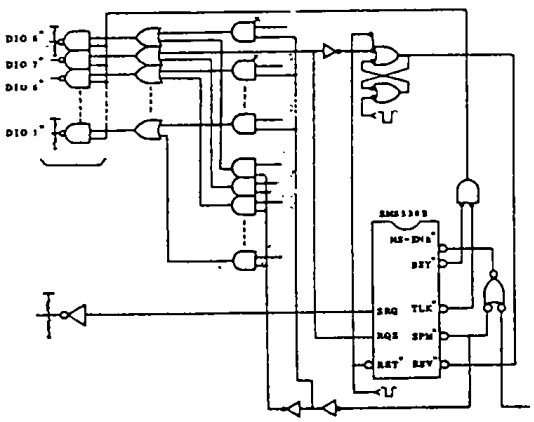


Figure 14 Service request circuit example

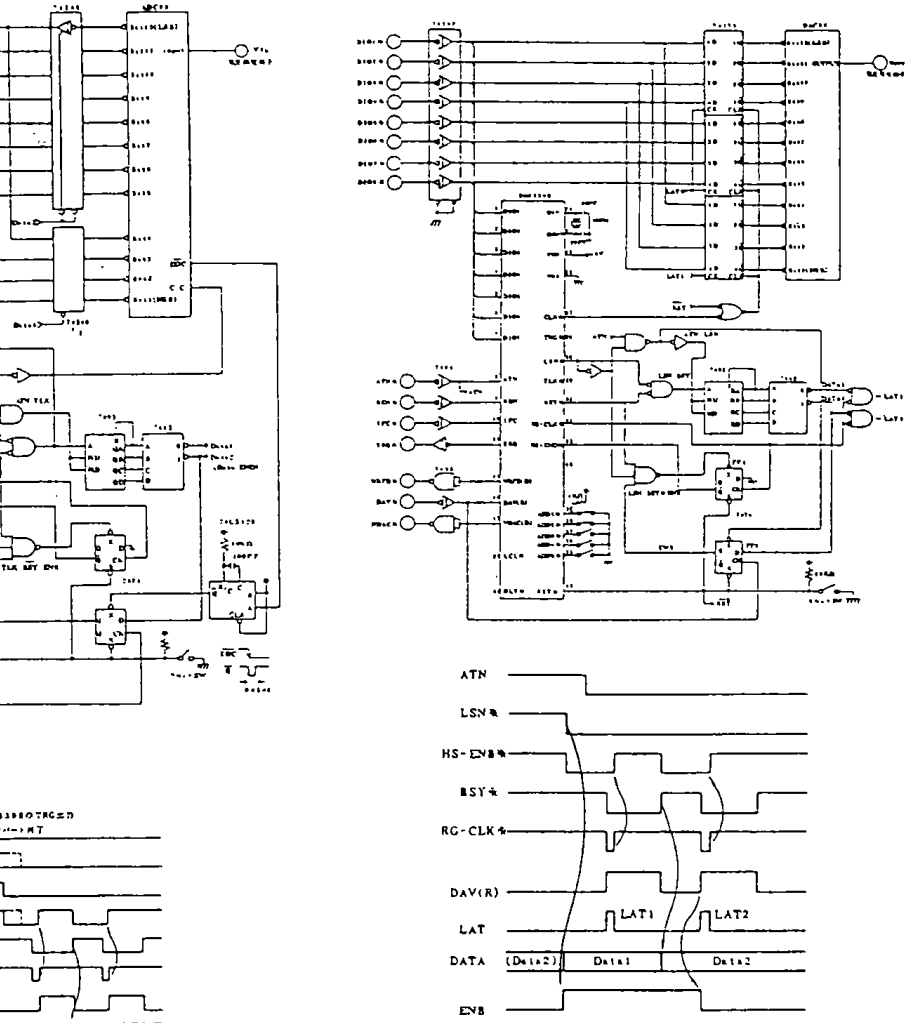


Figure 16 Listener application (DA converter control)

ation (AD converter control)