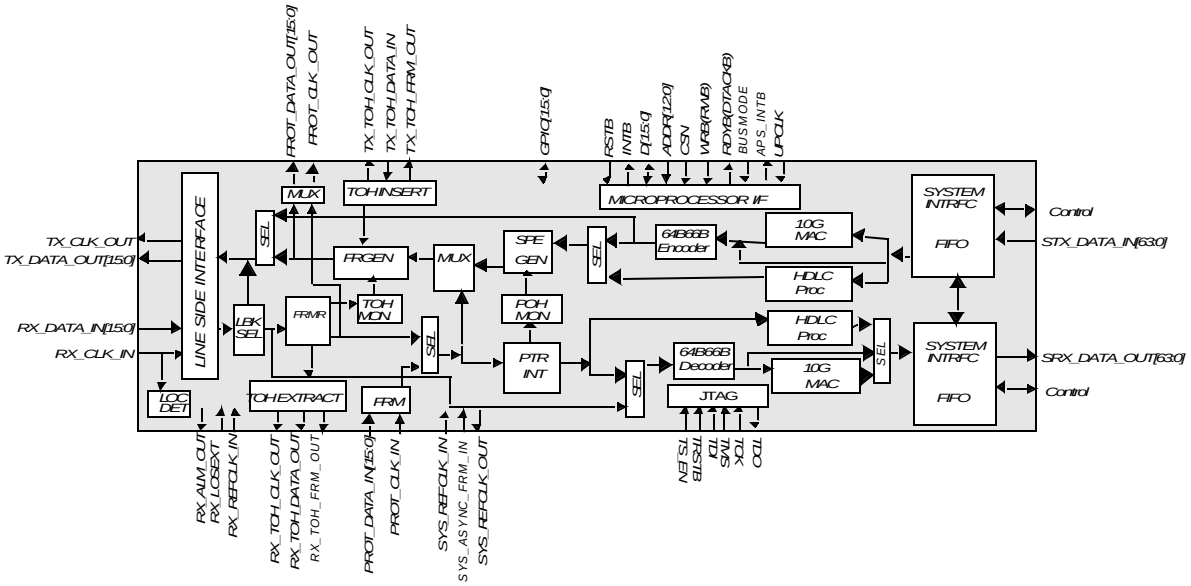
Features

- Single STS-192c/STM-64 framer/mapper device to support 10 Gigabit Ethernet (10GbE) serial WAN, serial LAN and STS-192c/ AU-4-64c POS applications.
- Supports full duplex mapping of Ethernet frames into a single SONET/SDH STS-192c/AU-4-64c (WIS functionality) in compliance with IEEE P802.3ae / D2.0 proposed baseline specification for 10GbE over the WAN.
- SONET/SDH section/line/path processing compliant with Telcordia GR-253, ANSI T1.105 and T1.416, and ITU G.751, G.783 and G.804. Provides a subset of the full SONET/SDH processing which implements the P802.3ae / D2.0 defined 10GbE WAN Interface Sublayer (WIS).
- Performs 10GbE MAC processing, compliant with IEEE P802.3ae / D2.0.
- Performs 64B/66B encoding in the TX direction and 64B/66B decoding in the RX direction when operating in 10GbE mode.
- A WIS bypass mode is provided, to support 10GbE serial LAN applications.
- Supports external MAC implementations.
- Alternatively, supports full-duplex mapping of packets in a single SONET/SDH STS-192c/AU-4-64c per IETF 2615 (POS).
- SONET/SDH processing includes termination and generation of section, line, & path layers, with transport/section and path overhead interfaces in both transmit and receive directions.
- POS processing includes HDLC framing, payload scrambling (x^{43} + 1) and transparency processing.
- 10GbE MAC transmit processing includes frame assembly, pad insertion, and CRC generation.
- 10GbE MAC receive processing includes Ethernet framing, CRC checking, and frame size monitoring.
- Supports 802.3x PAUSE flow control.
- Provides counters to support implementation of RMON, 802.3 MIBs.
- Provides a 622.08 MHz 16-bit bus interface on the line side in both the TX and RX directions (SFI-4/XSBI compliant).
- Provides a 644 MHz 16-bit LVDS interface on the line side in both TX and RX directions for LAN PHY applications (XSBI).
- Provides a 64-bit, 200 MHz FlexBus-4™ system interface (SPI-4 Phase 1 compliant).
- Direct Map Mode for mapping of any traffic type in SONET/SDH STS-192c/AU-4-64c payloads
- 16-bit synchronous microprocessor interface for configuration, control, and status monitoring.
- Provides a 622.08 MHz 16-bit line bus to support Automatic Protection Switching (APS) configurations.
- Packaged in a 624-pin CBGA.
- Implemented in .18 micron CMOS, 1.8V and 2.5V technology.

Figure 1: Block Diagram



FInal Production Release Information - The information contained in this document is about a product in its fully tested and characterized stage. All features described herein are supported. Contact AMCC for updates to this document and the latest product status.

Overview and Applications

The S19205 is a dense VLSI device that integrates a 10GbE MAC, a 64B/66B Physical Coding Sublayer (PCS) and a WAN Interface Sublayer (WIS) as baselined by the IEEE P802.3ae task force. Optionally, it can be configured to perform full-duplex mapping of packets into SONET/SDH payloads at OC-192c rate (POS). When configured for SONET/SDH operation, the S19205 supports Automatic Protection Switching (APS) as required in carrier-class equipment.

SONET/SDH Processing (WIS)

The S19205 implements SONET/SDH processing functions for a single STS-192/STM-64 data stream. The S19205 performs full section, line, and path overhead processing of all defined TOH/POH bytes, including framing, scrambling/descrambling, alarm signal (AIS) insertion/detection, remote failure insertion/detection (REI/RDI), section/path trace insertion/capture (J0/J1) and bit interleaved parity (B1/B2/B3) processing. The S19205 provides programmable Signal Fail (SF) and Signal Degrade (SD) thresholds for B2 and B3 monitoring.

The S19205 is SONET and SDH standards compliant with Telcordia GR-253, GR-499 and GR-1377, and ANSI T1. 105-1995, and ITU G.707 and G.783.

POS HDLC Processing

The S19205 can be configured for HDLC processing for STS-192c/AU-4-64c POS applications. When configured for POS HDLC processing, the S19205's transmit HDLC processor will provide the insertion of HDLC framed packets into the STS SPE. It will perform packet framing, provide interframe fill and TX FIFO error recovery. In addition, it optionally performs payload scrambling ($x^{43} + 1$), performs transparency processing as required by RFC 2615 and will optionally generate a 32 bit CRC.

The receive HDLC processor provides for the extraction of HDLC frames, transparency removal, de-scrambling (if enabled), FCS error checking and optionally deletes the HDLC address and control fields. The S19205 also provides a robust set of counters and status/control registers for performance monitoring via the microprocessor.

It is SONET/SDH standards compliant IETF RFC 1662 and RFC 2615.

10 Gigabit Ethernet MAC Processing

The 10GbE Medium Access Control block supports full-duplex traffic at 10Gbps rates. In the transmit direction, it performs encapsulation of packets received through the system interface into Ethernet frames. It provides pad insertion to insure a minimum frame length, as well as CRC generation. The MAC processing block also provides for preamble, SFD and IFG generation.

In the receive direction, the MAC processing consists of Ethernet framing and CRC validation, as well as monitoring of the size of the received frame.

The MAC block also integrates an extensive set of counters for network statistics collection in support of RMON and IETF standard MIBs.

The MAC supports flow control for both serial LAN (10Gbps) or WAN (9.95Gbps) applications through the 802.3x MAC 'PAUSE' functionality.

64B/66B Encoder / Decoder

When configured for Ethernet operation, the PCS sublayer performs frame scrambling and bit ordering before passing data to the WAN Interface Sublayer or to the XSBI interface. 64B/66B block coding is used to guarantee run length, transition density and DC balance of the serial data stream. Data frames are delineated using "01" sync header. Control frames are identified with a "10" sync header.

Line-side Interface

In 10GbE WAN PHY and OC-192c POS mode, the line-side interface supports a 16-bit parallel bus operating at 622.08 MHz, compliant with the OIF SFI-4 and the proposed IEEE P802.3ae XSBI interfaces. In 10GbE LAN PHY mode, the line side interface operates as a XSBI-compliant 16-bit LVDS parallel interface operating at 644.53MHz.

System Interface

A 64-bit, 200MHz FlexBus-4™ interface is used for transferring packets on the system side. FlexBus-4™ is compliant to the OIF SPI-4 Phase 1 Specification.

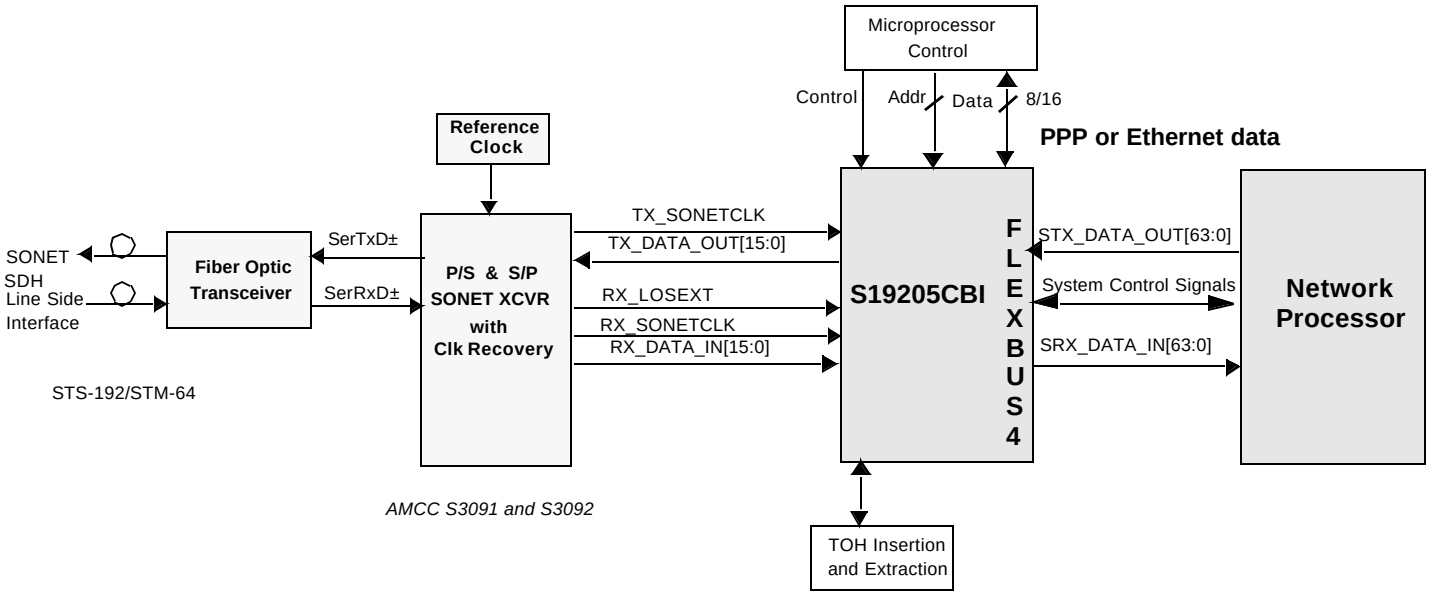
Microprocessor Interface

The user of the S19205 can select between an 8-bit asynchronous or a 16-bit synchronous microprocessor interface for device control and monitoring. The interface supports both Intel and Motorola type microprocessors, and is capable of operating in either an interrupt driven or polled-mode configurations.

Applications

- Core switches/routers
- Multi-service switches
- MAN switches
- Direct Mapping of any traffic type in SONET/SDH STS-192c/AU-4-64c payloads

Figure 2: Typical Application



200 Minuteman Road • Andover, MA 01810 • Tel: 978-247-8000 • Fax: 978-623-0024 • http://www.amcc.com